MRF Timing System

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Timing Workshop CERN
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Micro-Research Finland Oy

- Founded in 1985
- Timing System development initiated in 1999 by the design of the timing system for SLS (series 100)
- References:
  - SLS, Paul-Scherrer Institute, Switzerland
  - Diamond Light Source Ltd., U.K.
  - ASP, Australia
  - BEPCII, Insitute for High Energy Physics, Beijing, China
  - LCLS, Stanford Linear Accelerator Center, USA
  - SNS, Oak Ridge National Laboratory, USA
  - SSRF, Shanghai, China
  - Elettra, Trieste, Italy
  - ALBA, Spain
  - And others...

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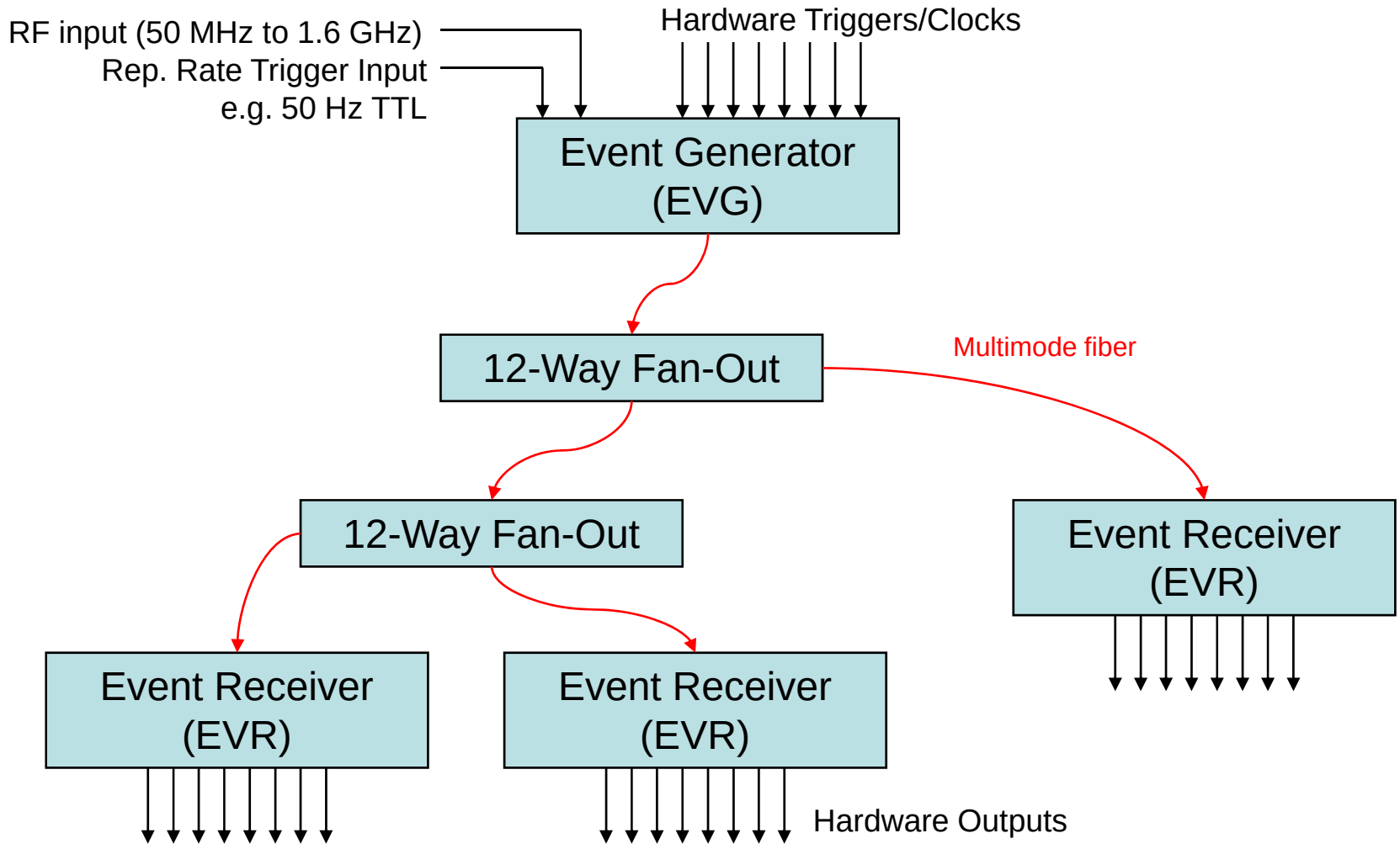
Timing System Overview



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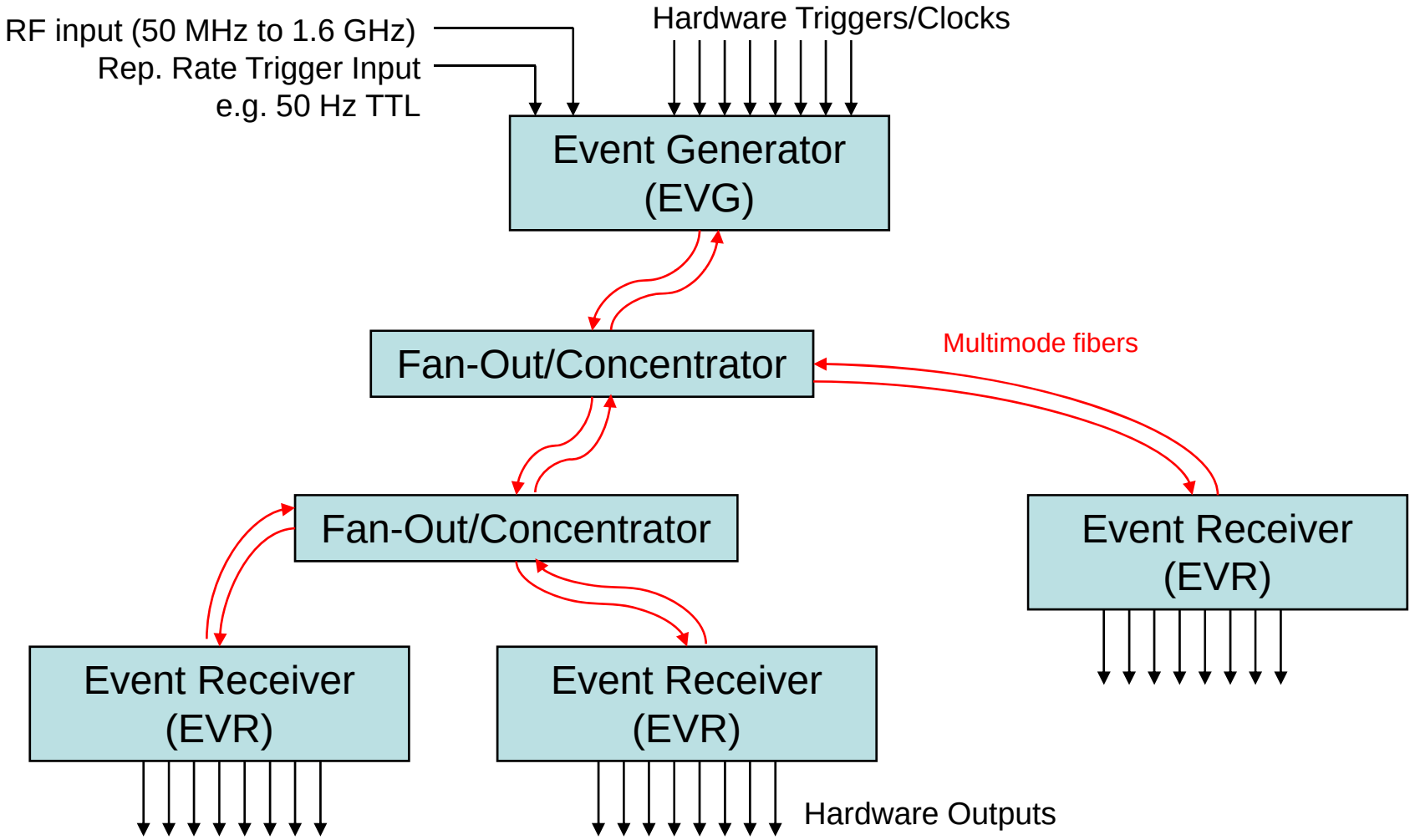
Timing System with Upstream



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Timing System Features

- Event driven system, 255 event codes
- Events are sent out with the event clock rate which is derived from an external RF reference
- Event clock rate 50 to 125 MHz
- Events generated
  - From external HW inputs
  - Two sequencers (up to 2048 events/sequencer)
  - Multiplexed counters
  - Software
- Eight distributed bus signals, updated simultaneously at the event clock rate, no interference with events
- Event Generators may be cascaded
  - EVGs synchronized to different clocks

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Timing System Features (cont.)

- Event Receivers lock to the EVG event clock and generate
  - pulse outputs with programmable delay and width
  - level outputs
  - Software interrupts
  - Synchronous clocks
  - RF recovery (VME-EVR-230RF only)
- Support for Timestamping/distribution of time
- Timestamping of external events
- Data transfer support with predictable timing
  - Up to 2 kbyte buffer
  - Max. 62.5 Mbytes/s
- SFP transceivers, multi-mode fiber

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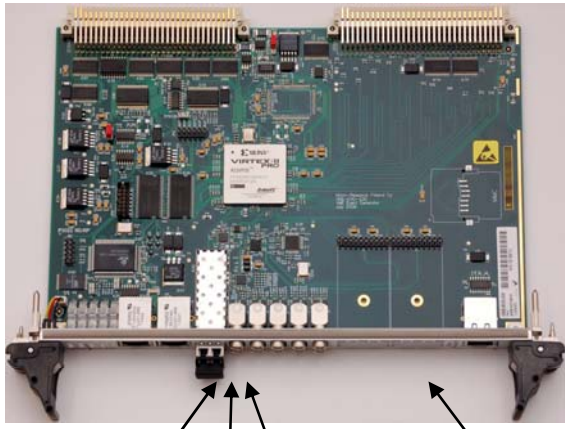
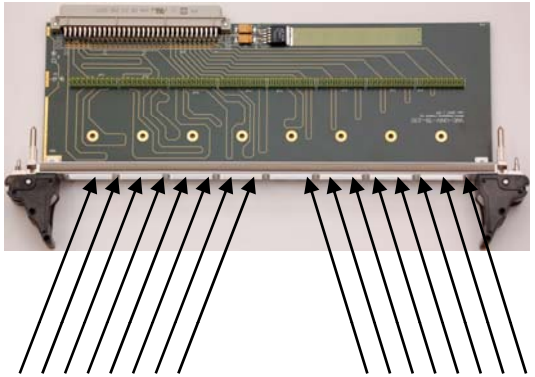
Event Generator (VME-EVG-230)





Distributed bus inputs

External trigger inputs

Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

SFP transceiver
• Optical signal to EVRs (fan-outs)
• Upstream EVG

RF input
• Event clock divided from RF /1, /2, ... , /32
• Event clock 50 – 125 MHz

Line syncronisation input
e.g. 50 Hz / 60 Hz TTL level

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Event Generator (cPCI-EVG-220/230)

Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

Line syncronisation input
e.g. 50 Hz / 60 Hz TTL level

RF input
• Event clock divided from RF
• /1, /2, ... , /32
• Event clock 50 to 100/125 MHz

SFP transceiver
• Optical signal to EVRs (fan-outs)
• Upstream EVG

Optional side-by-side I/O extension module for three Universal I/O slots, providing up to six I/O signals

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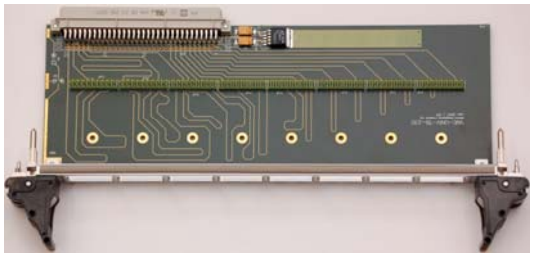
VME Event Receiver (VME-EVR-230)



Eight Universal I/O slots
• Up to sixteen programmable I/O, TTL/NIM/Optical

SFP transceiver
• Optical signal from EVG (or fan-out)

Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

Programmable outputs
• 8 TTL level
• External trigger input

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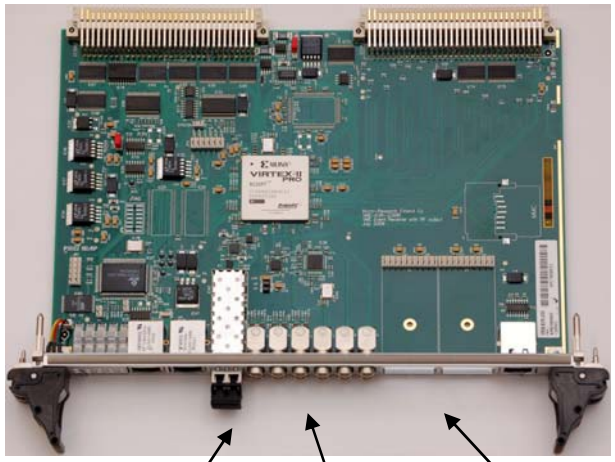
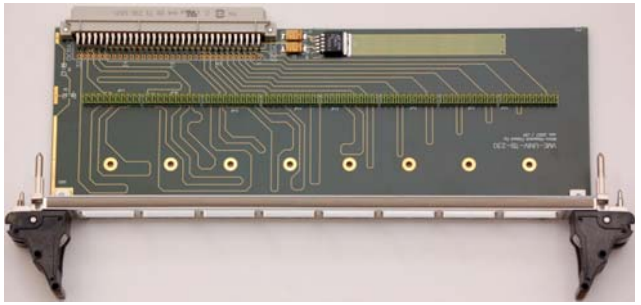
VME Event Receiver with RF output (VME-EVR-230RF)





Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

SFP transceiver
• Optical signal from EVG (or fan-out)

Programmable outputs
• 4 TTL level
• External trigger input
• External inhibit input

• 3 Differential CML RF/pattern outputs with 1/20th event cycle resolution (400 ps @ 8 ns event clock cycle)

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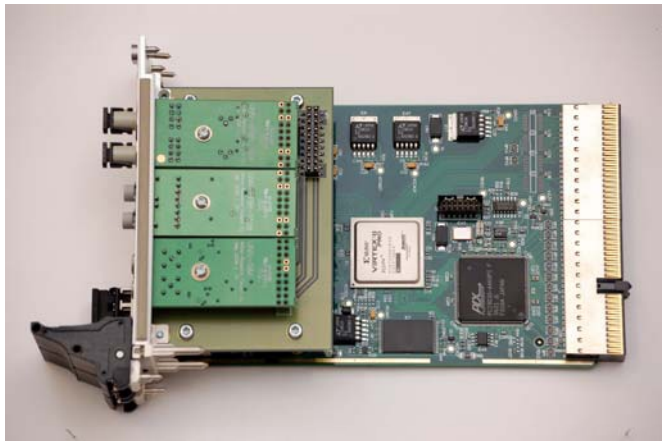
CompactPCI Event Receiver (cPCI-EVR-220/230)

Two Universal I/O slots
- Up to four programmable I/O, TTL/NIM/Optical

- External trigger input
- External inhibit input

SFP transceiver
- Optical signal from EVG (or fan-out)

Optional side-by-side I/O extension module for three Universal I/O slots, providing up to six I/O
TTL/NIM/Optical



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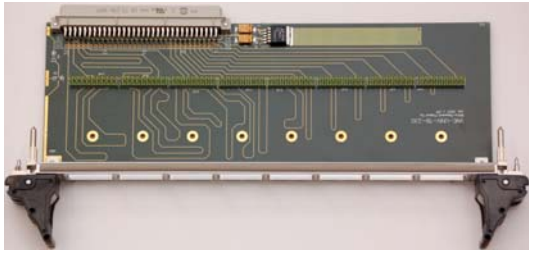
PMC Event Receiver (PMC-EVR-230)

- SFP Transceiver
- External trigger input
- Three TTL outputs

Transition Board I/O through VME P2



Eight Universal I/O slots
- Up to sixteen programmable I/O, TTL/NIM/Optical

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Event Receiver Performance

Module	Resolution	Jitter typ.
VME-EVR-230	8 ns min. *)	< 25 ps RMS
VME-EVR-230RF (standard outputs)	8 ns min. *)	< 15 ps RMS
VME-EVR-230RF (CML outputs)	400 ps (8 ns / 20)	< 5 ps RMS
cPCI-EVR-220	10 ns min.	< 25 ps RMS
cPCI-EVR-230 PMC-EVR-230	8 ns min. *)	< 25 ps RMS

*) 10 ps with UNIV-LVPECL-DLY module

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Universal I/O Modules

- 25.4 mm x 52 plug-in units
- two outputs or inputs each
- can be fitted on VME-EVG-230 and VME-EVR-230(RF), VME-UNIV-TB, CompactPCI EVG/EVR, CompactPCI side-by-side module
- Module specification available on-line for custom module development

Optical HFBR-1414	Optical HFBR-1528	NIM Output	TTL Output	TTL Input	LVPECL Output	LVPECL Output
						
820 nm	650 nm 1 mm POF					10 ps step Delay tuning

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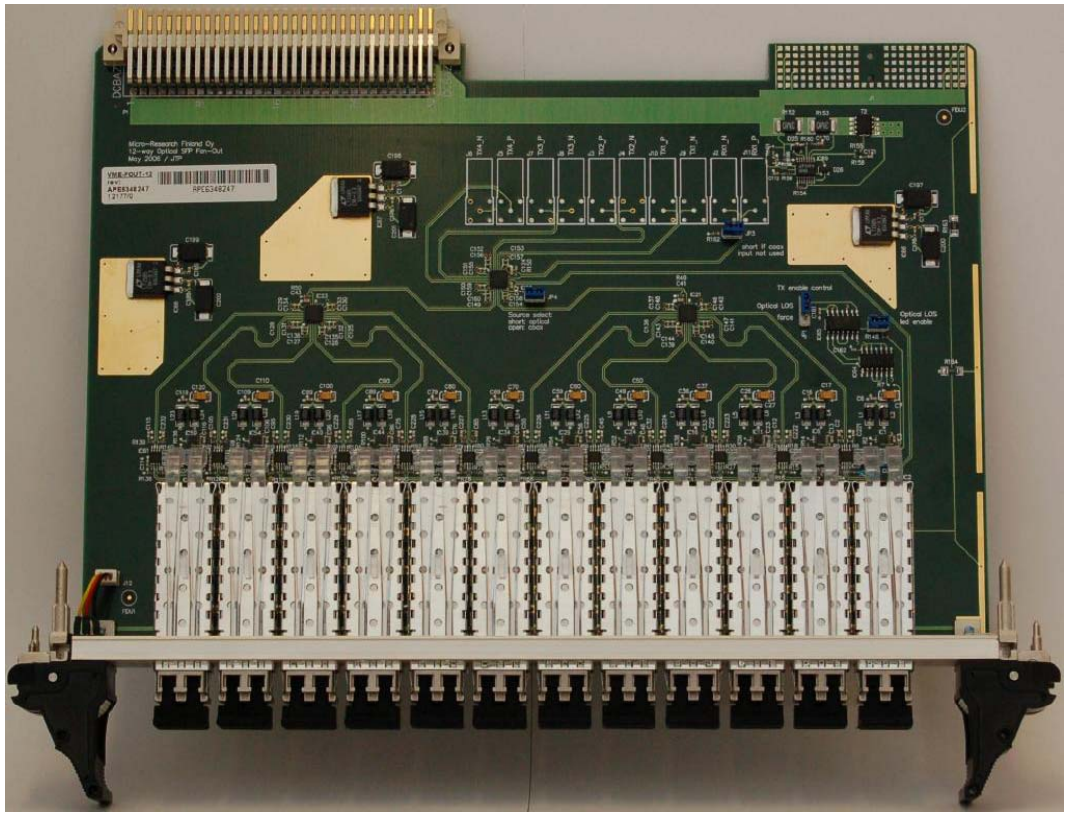
Fan-Out Modules (VME/cPCI-FOUT-12)



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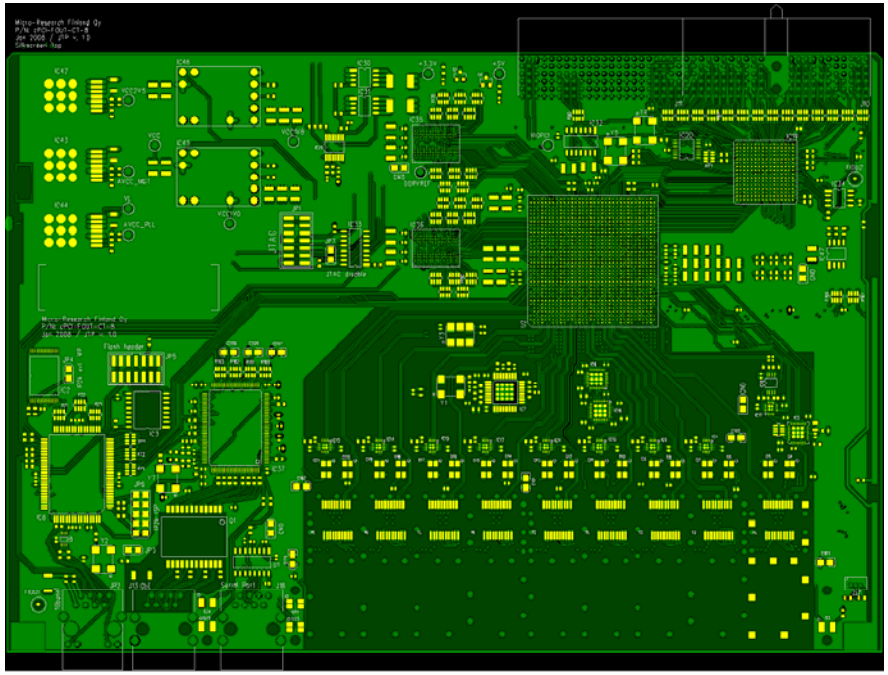
Fan-Out Concentrator Module (cPCI-FOUT-CT-8)



- Upstream events
- Upstream distributed bus
- Upstream data transfer
- Fiber length measurement

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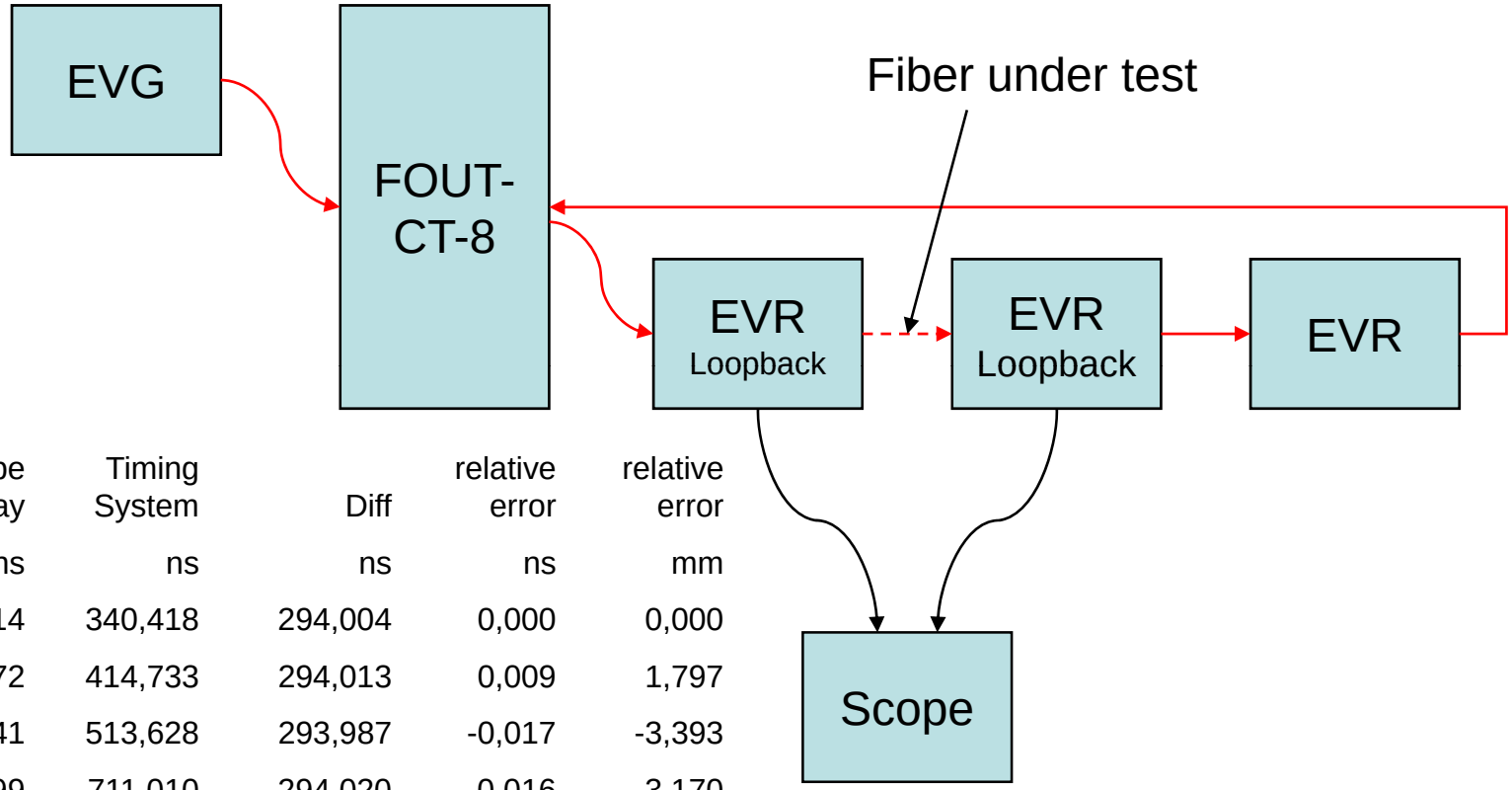
Fiber Delay Measurement Setup



Fiber length	Scope Delay	Timing System	Diff	relative error	relative error
m	ns	ns	ns	ns	mm
9	46,414	340,418	294,004	0,000	0,000
24	120,72	414,733	294,013	0,009	1,797
44	219,641	513,628	293,987	-0,017	-3,393
84	416,99	711,010	294,020	0,016	3,170
164	812,625	1106,629	294,004	-0,001	-0,105
294	1455,446	1749,457	294,011	0,007	1,340
554	2741,692	3035,692	294,000	-0,005	-0,930

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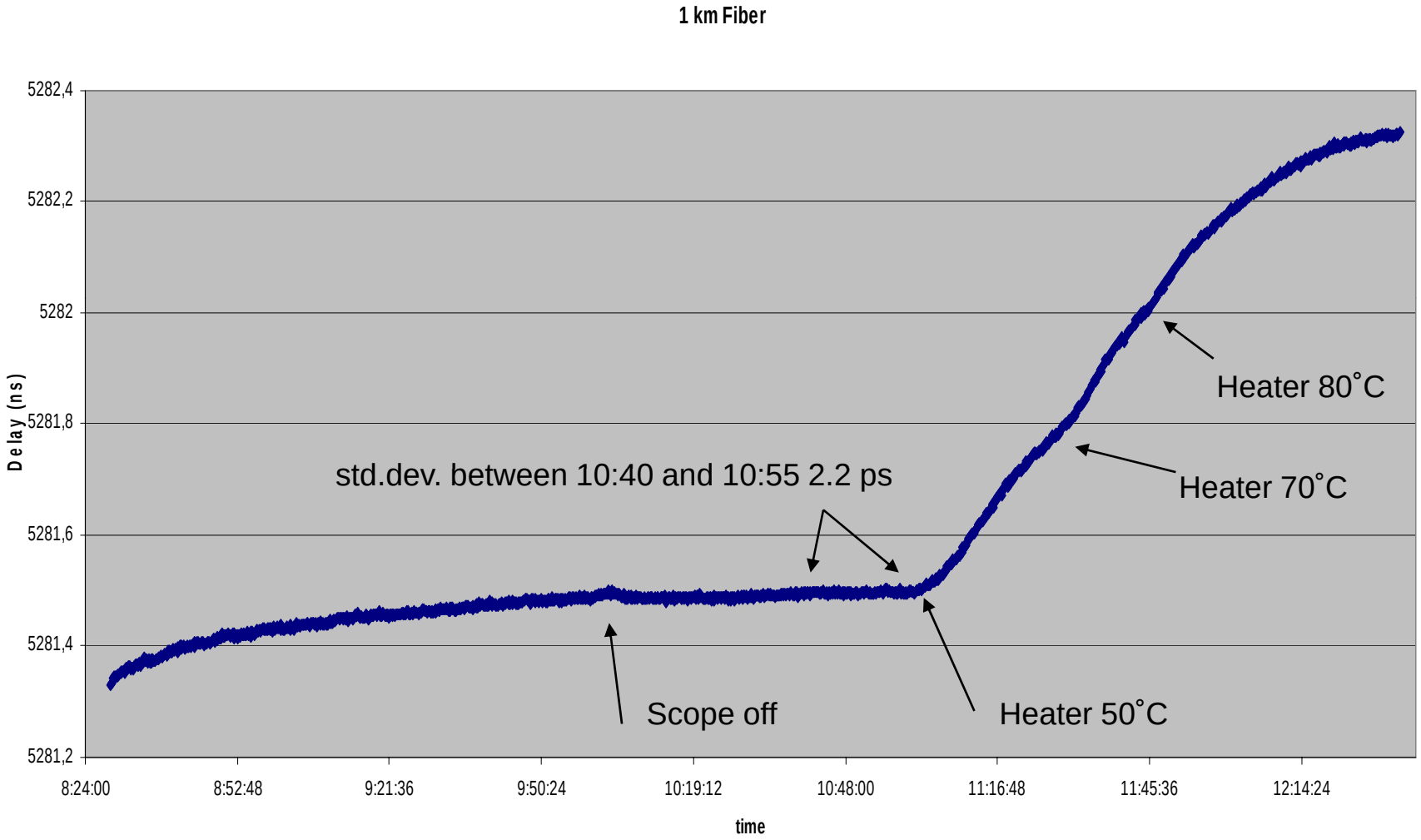
Fiber Delay Measurement



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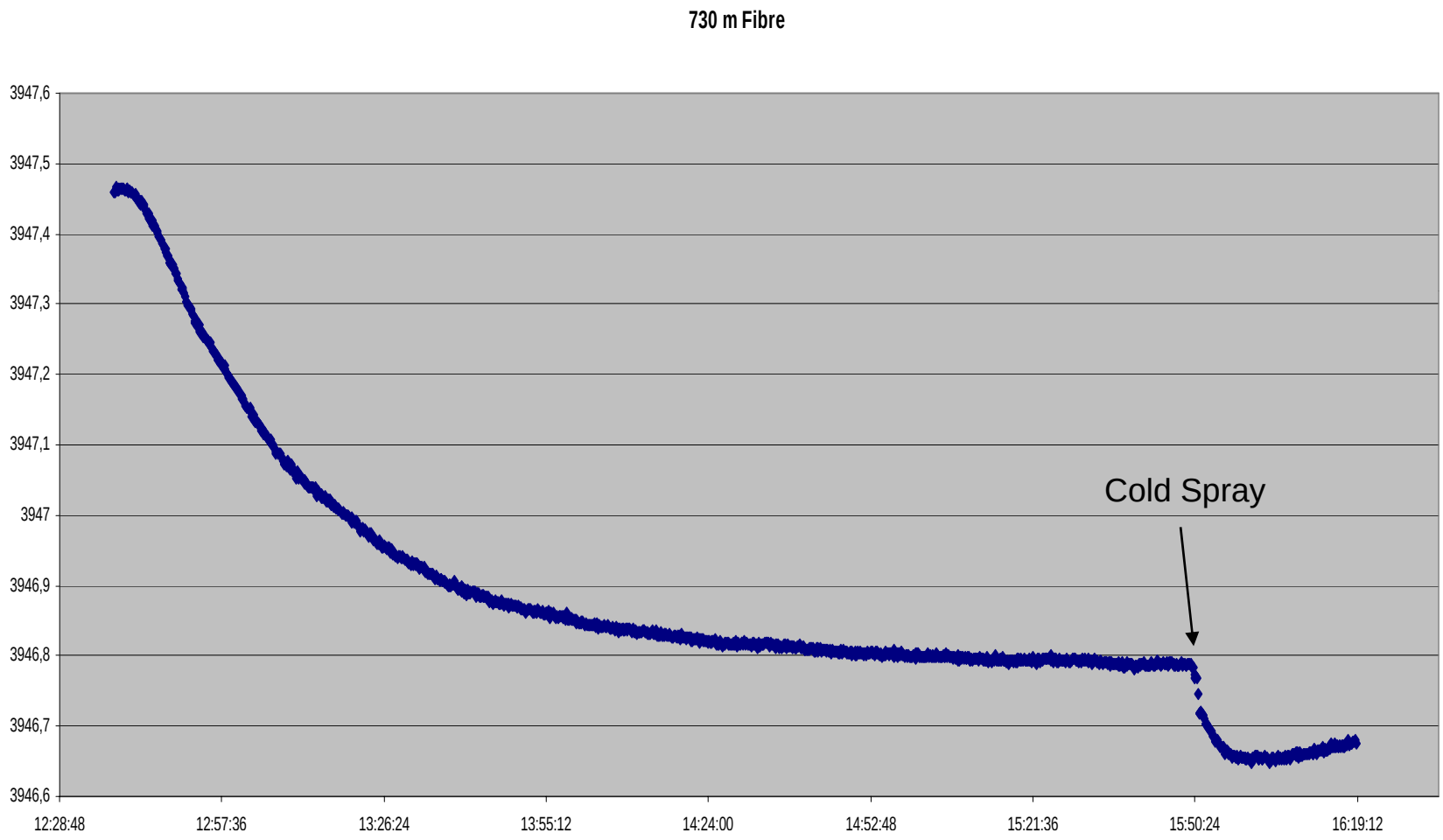
Fiber Delay Measurement



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VME-ADC-200 4 x 1 Gsps ADC Prototype

- Designed to be used for filling pattern feedback at SLS
- Two Atmel AT84AD001B Dual 8-bit 1 Gsps ADCs
  - 2 Gsps in interleaved mode
  - 500 mVpp Differential Analog Input
  - 1.5 GHz Full Power Input Bandwidth (-3 dB)
  - Sample clock can be shifted in 10 ps steps
- Integrated Event Receiver
  - Production version will recover RF (ADC conversion clock) from event system
  - Timing/triggering from event system

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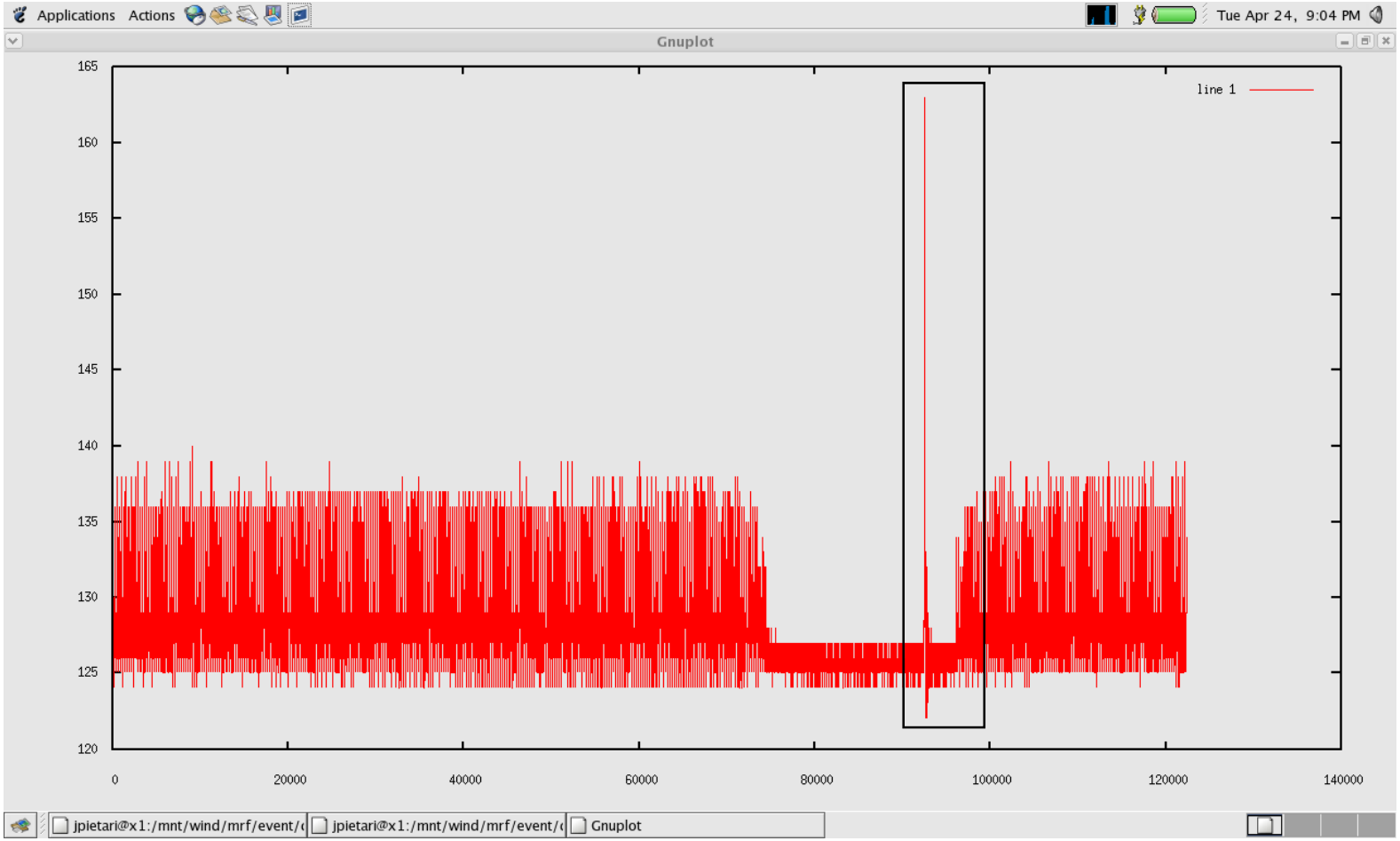
SLS filling pattern sample with VME-ADC-200 prototype



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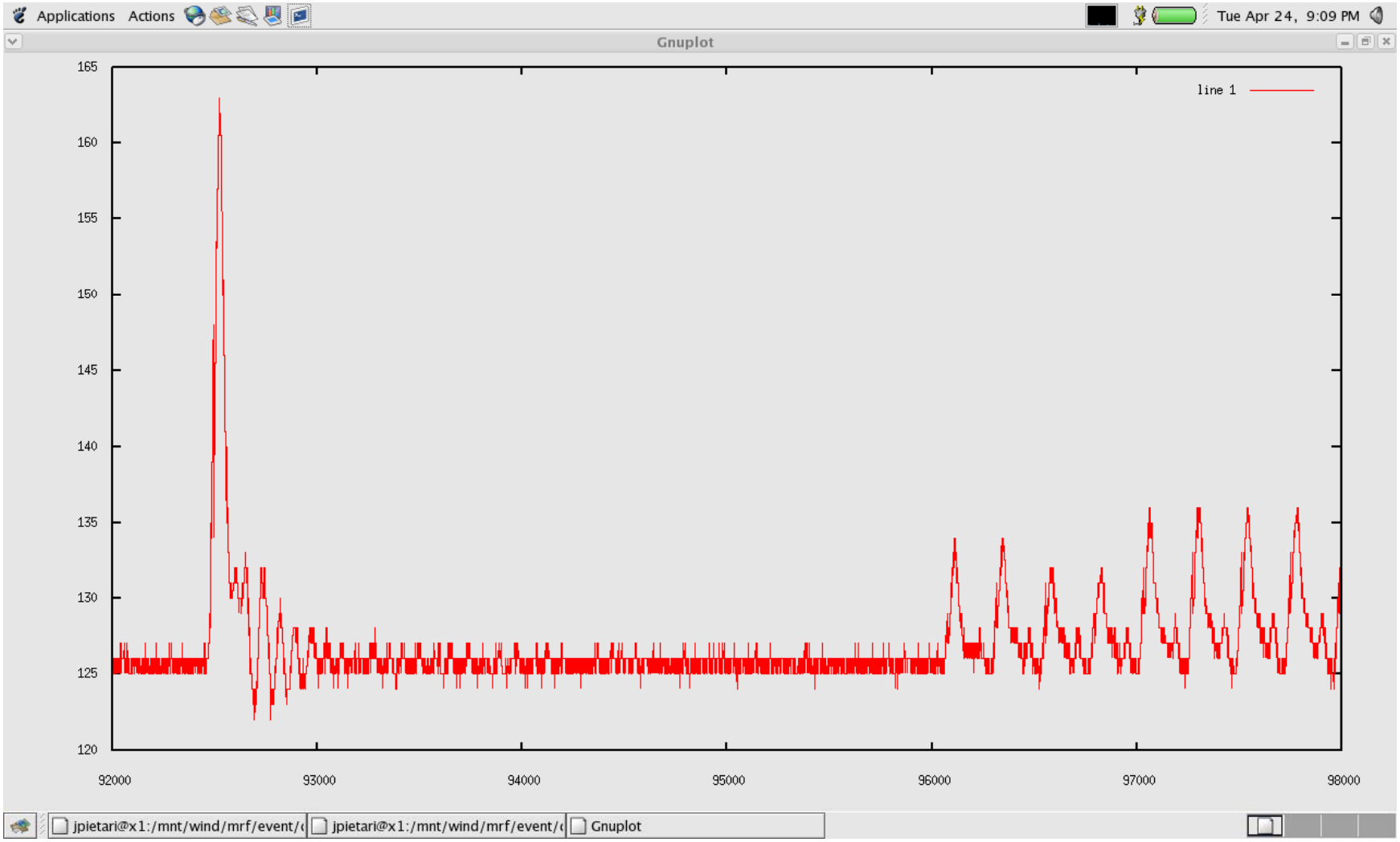
SLS filling pattern sample with VME-ADC-200 prototype



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Other products

- Electron Gun Triggering
  - Transmitter module EGUN-TX
  - Receiver module at high voltage EGUN-RX

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Future Interests

- EPIC form factor EVR prototype (see http://www.pc104.org)
  - Integrated CPU (either soft-CPU inside FPGA or Freescale Coldfire)
  - Integrated EVR
  - PC104 bus / PCI bus
- Event Receiver for CompactRIO (National Instruments)
  - Feasibility? cRIO interface not very suitable for timing receiver

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