AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

AIDA IP blocks activities at AGH-UST

Marek Idzik AGH-UST

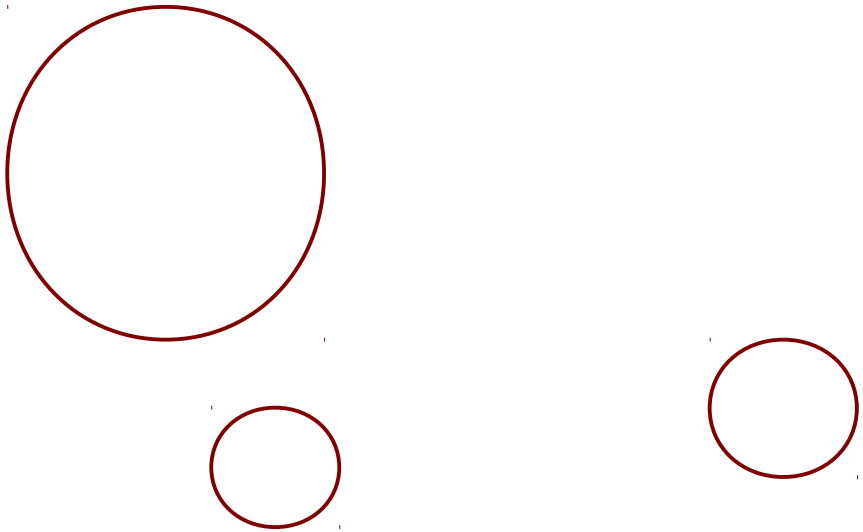
Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

AIDA 3rd Annual Meeting, Vienna 26-28 March 2014

Outline and Status of IP blocks at AGH-UST

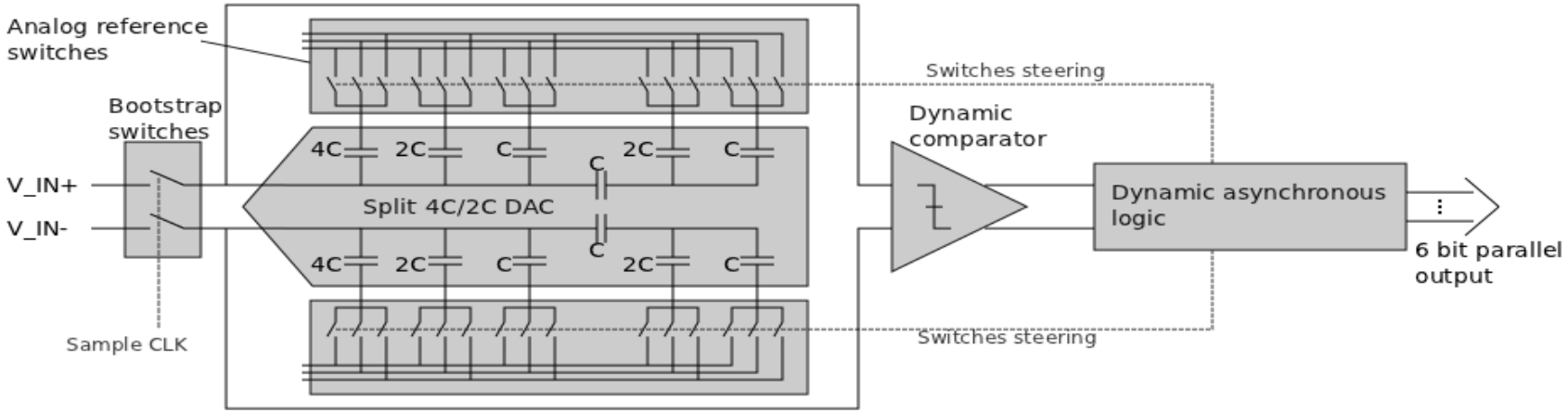
- Design Kit for 65 nm not yet released by CERN
  - We are still waiting to start design in 65 nm. We hope for submission this year...
- At the beginning of AIDA AGH-UST proposed to develop some blocks in IBM 130 nm
  - Fast (>40 Msps) 6-bit
  - Fast 10-bit SAR ADC
  - Variable frequency PLL
  - SLVS interface
- All above blocks were designed in IBM 130 nm, 1st prototypes were produced, the result are summarized in next slides...

IP blocks needed for multichannel readout
Example: SALT chip architecture



- Readout of silicon strip detectors in LHCb Upgrade or LumiCal detector in future ILC will contain front-end and ADC in each channel, and fast serialization of output data.
- Among the key blocks in these readouts, which can be also used as IP cores, are ADC, PLL, SLVS
- First prototypes of these blocks are available – the performed measurements are discussed in this talk

6-bit SAR ADC for SALT chip in LHCb Upgrade Architecture&Design considerations



Architecture of ADC:

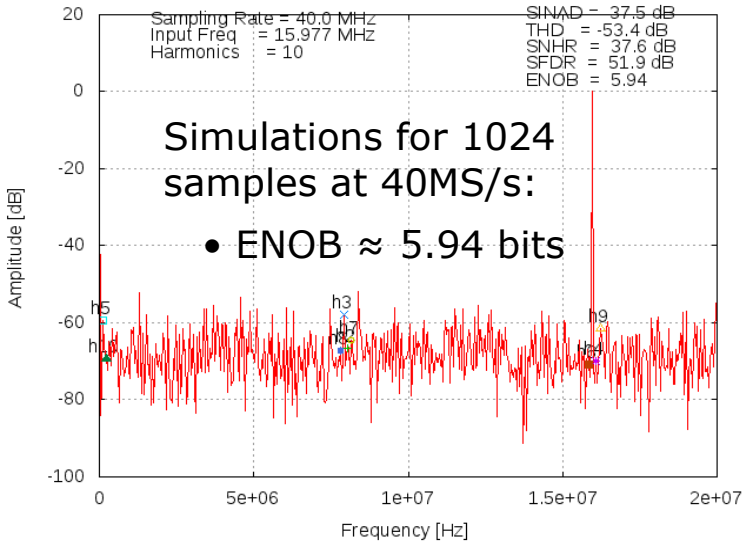
- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

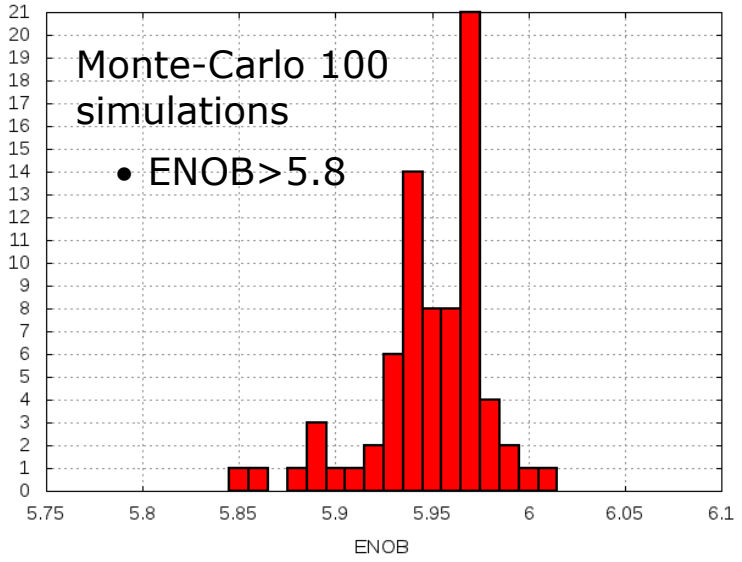
Design considerations:

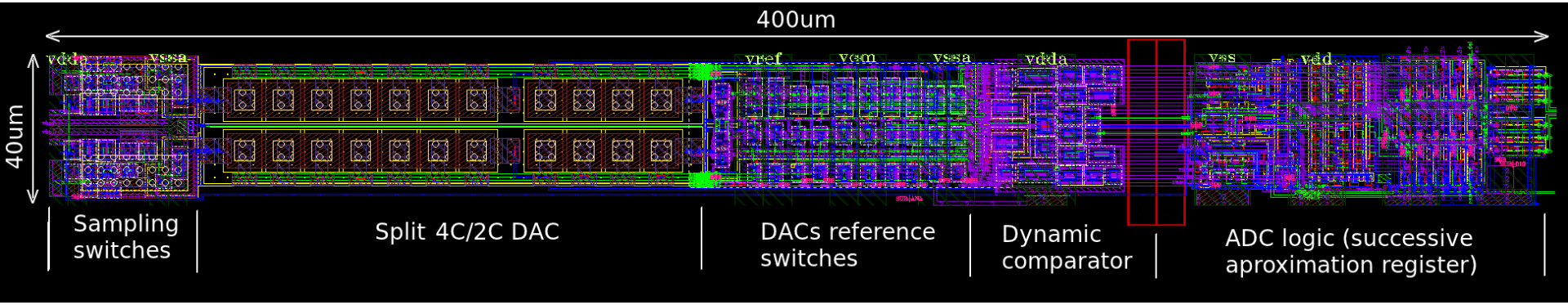
- Resolution 6 bits
- Variable sampling frequency up to ~80 MS/s
- Power consumption at 40 MS/s 0.35 mW
- pitch, ready for multichannel integration 40 µm

K. Świentek, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, T. Szumlak "SALT – new silicon strip readout chip for the LHCb Upgrade", TWEPP2013 23-27 September 2013, Perugia Italy

6-bit SAR ADC
Post-layout simulations

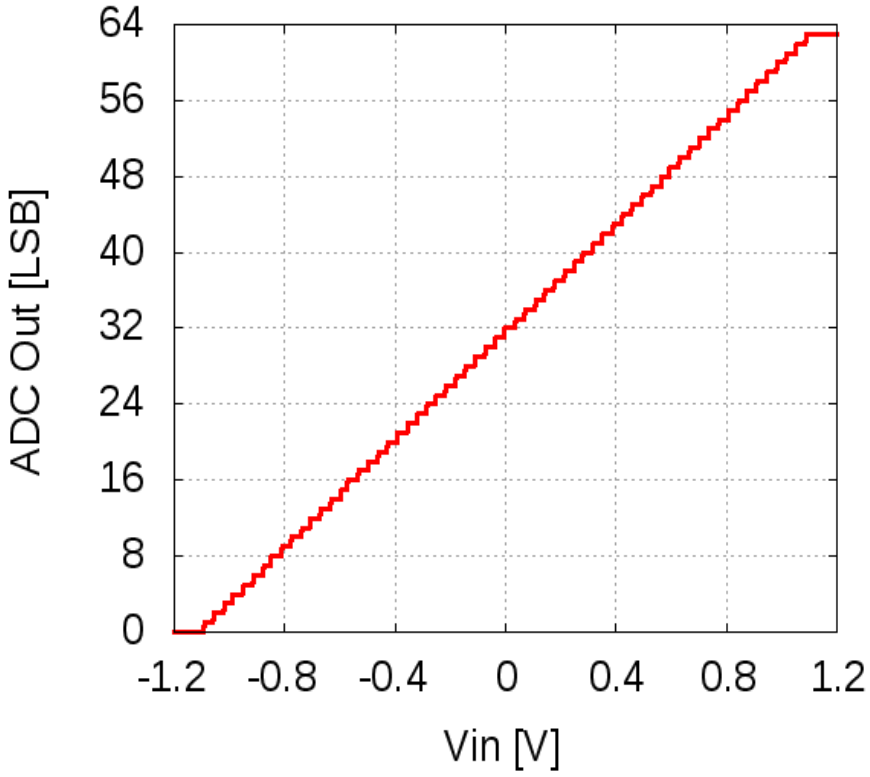




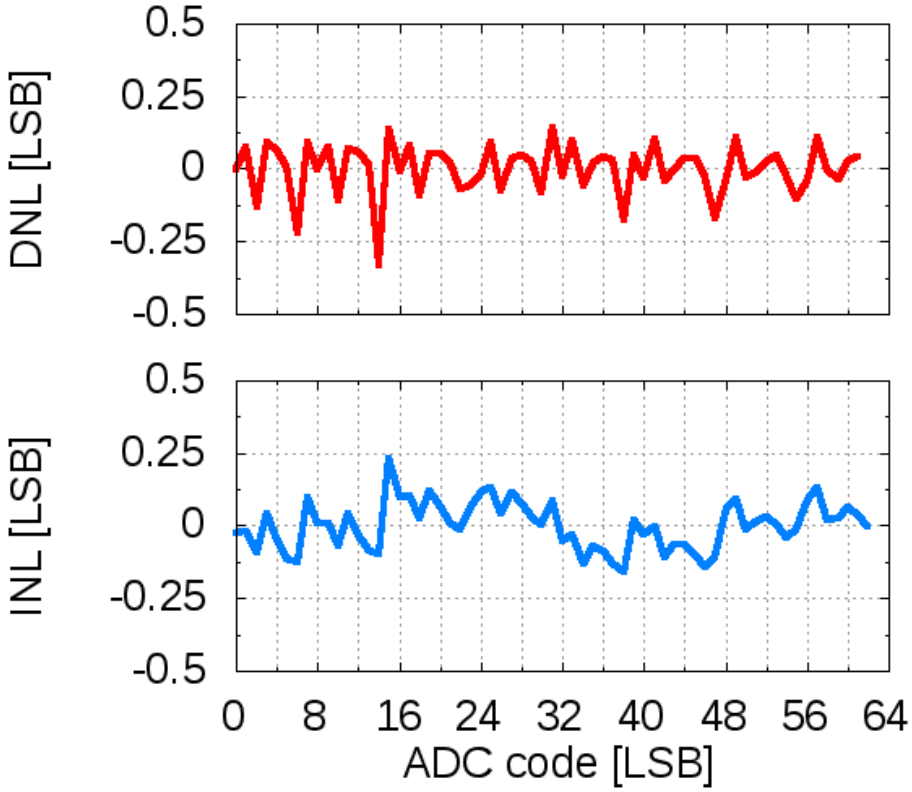


6-bit SAR ADC
Static tests – linearity (@50 MS/s)

Transfer function



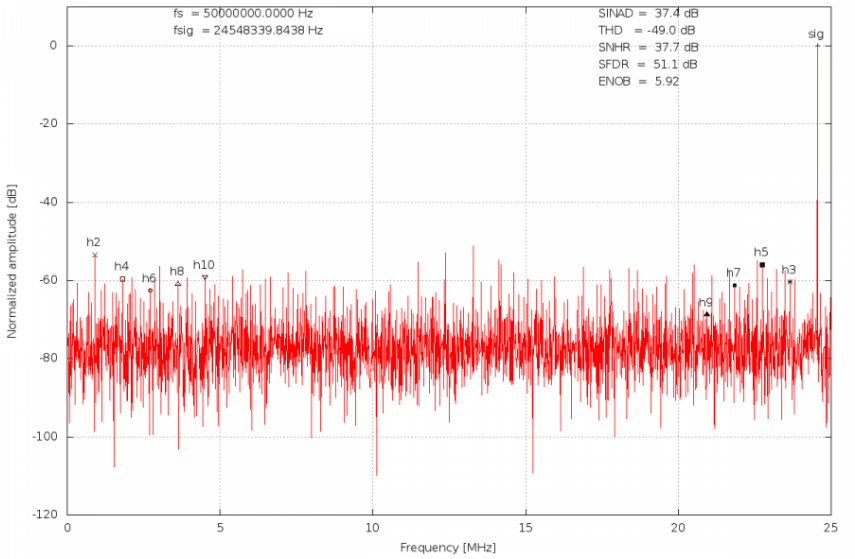
INL/DNL measurements



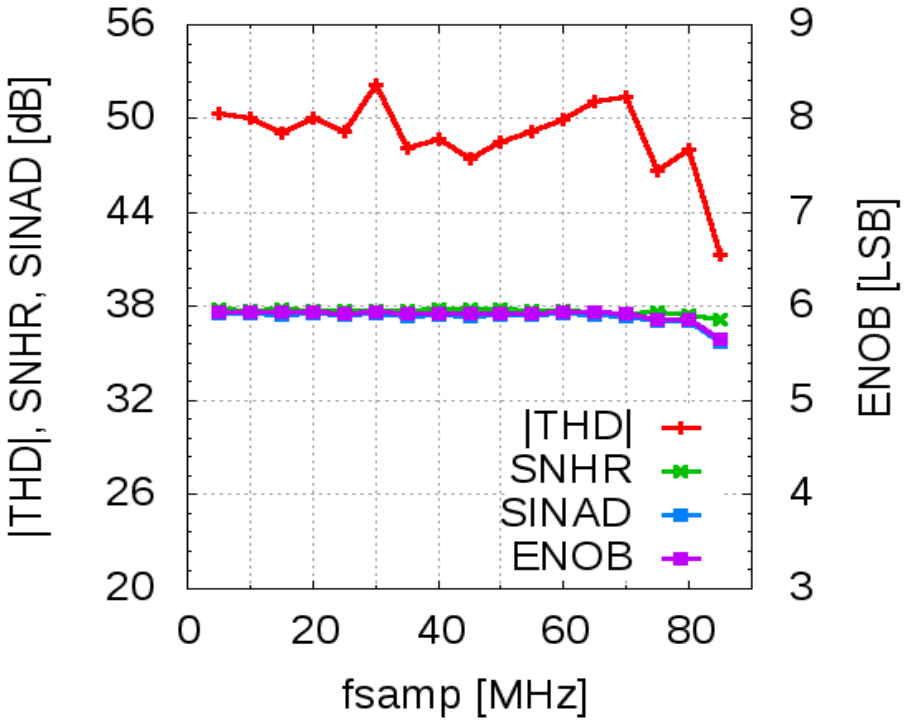
- Measurements show that ADC works very well
- At 50MHz sampling frequency good linearity INL, DNL < 0.4 is seen

6-bit SAR ADC
Dynamic tests – ENOB effective resolution

Example DFT Spectrum @50MS/s

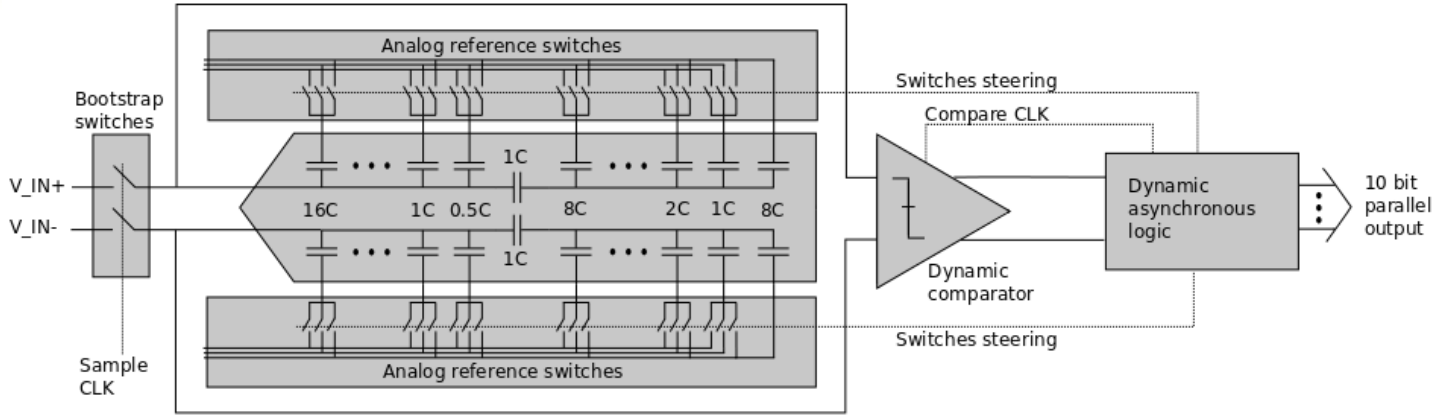


Sampling frequency sweep



- Measurements show very good dynamic behaviour.
- Measured ENOB is between 5.7 – 5.9 bits
- ADC works well for sampling frequencies beyond 80 MHz

10-bit SAR ADC for LumiCal at ILC
Architecture&Design considerations



Architecture of ADC:

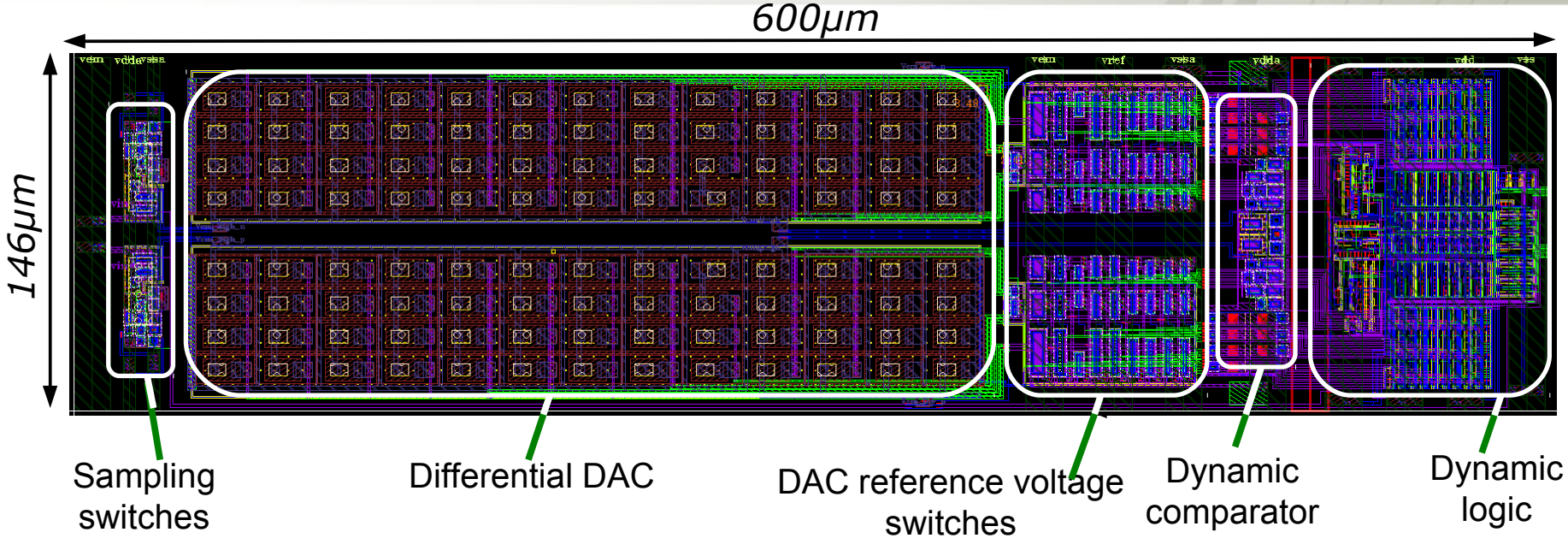
- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

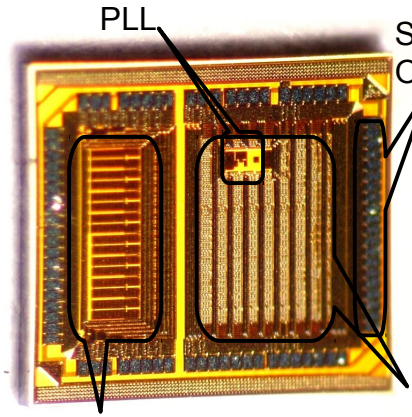
Design considerations:

- Resolution 10 bits
- Variable sampling frequency up to ~50 MS/s
- Power consumption at 40 MS/s ~1 mW
- pitch, ready for multichannel integration 146 µm

J. Moron, M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, K. Swientek. "Development of variable sampling rate low power 10-bit SAR ADC in IBM 130 nm technology", TWEPP2013 23-27 September 2013, Perugia Italy

10-bit SAR ADC for Lumical



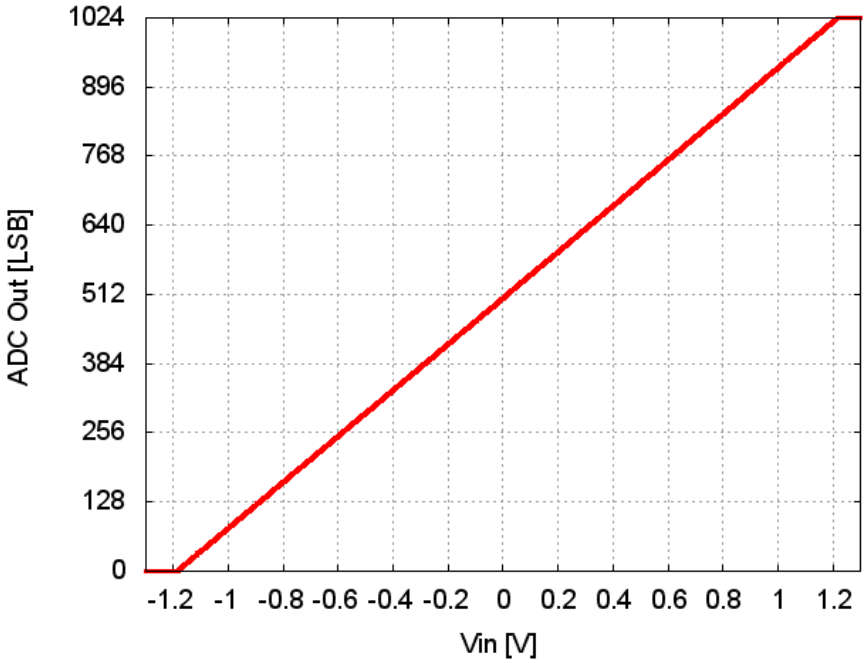


Simulated performance of 10 bit ADC:

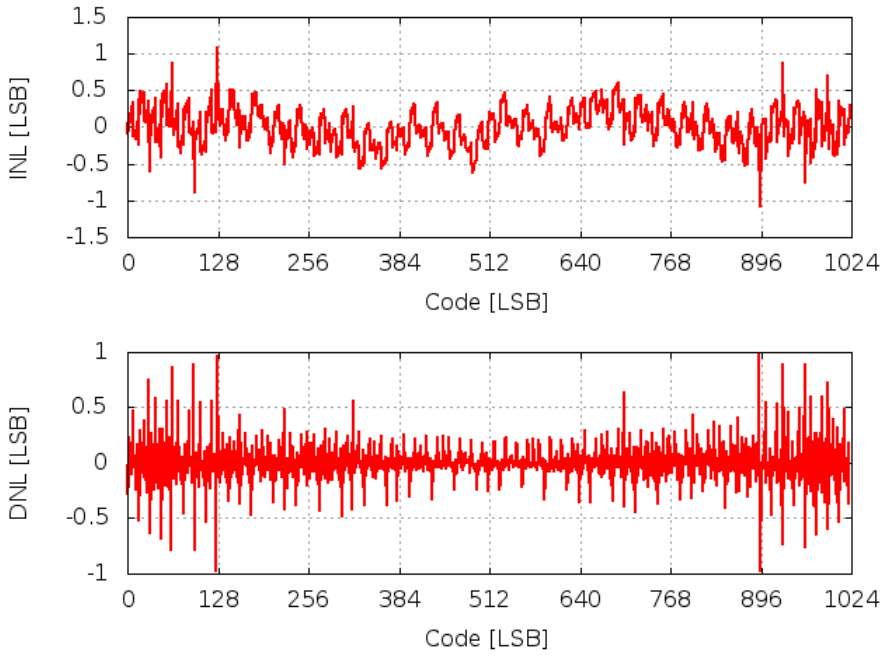
- Simulated ENOB ~ **9.5-9.7 bits**
- Maximum sampling rate **~50 MS/s**
- Power consumption ~ **1mW @ 40 MS/s**

10-bit SAR ADC for LumiCal
Static measurement results

Transfer function



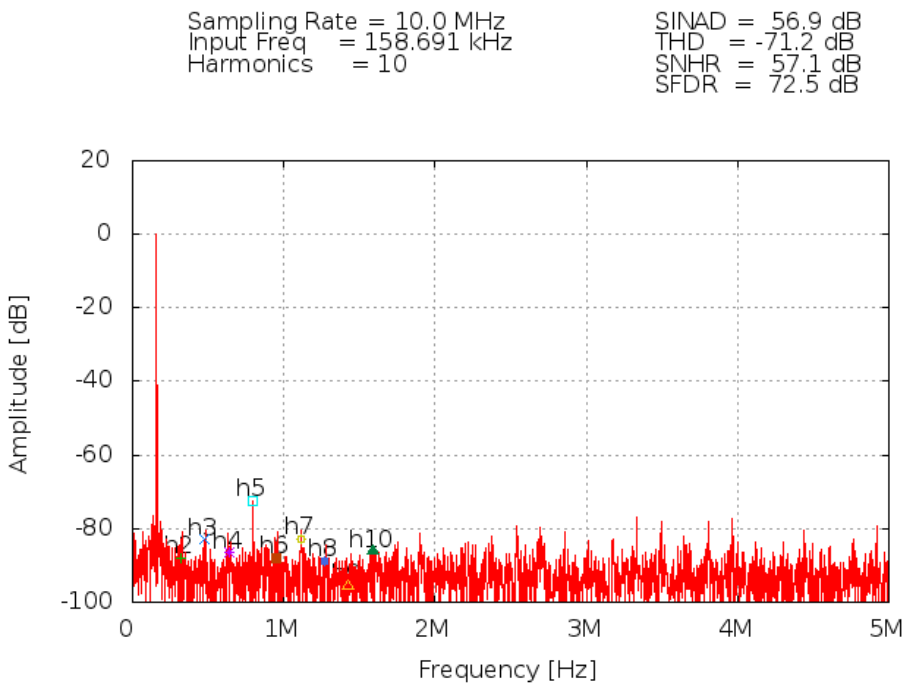
INL/DNL measurements



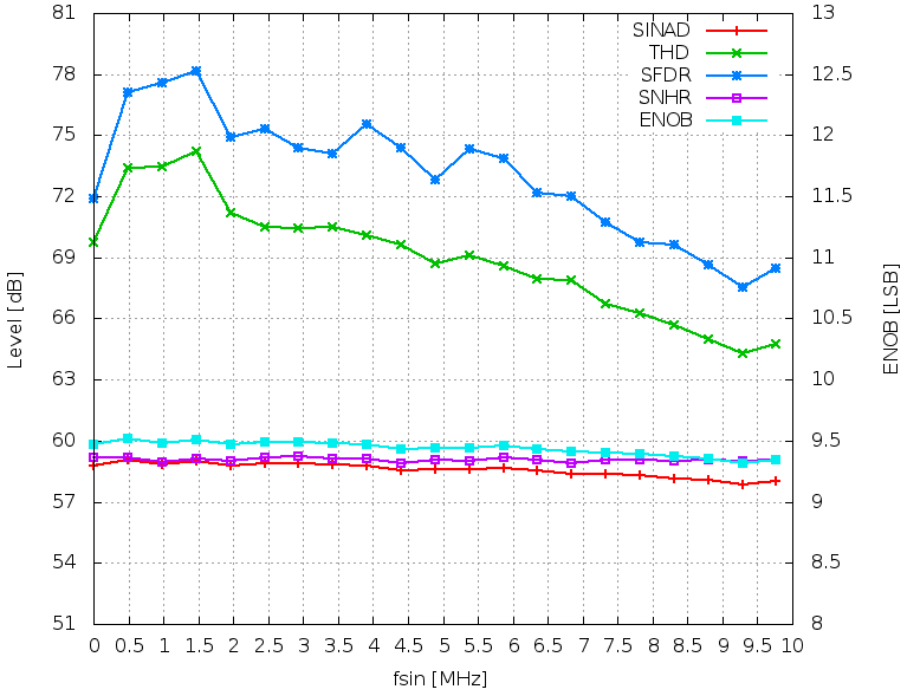
- ADC works well in the whole input signal range
- Generally, good linearity is measured, although for a few codes improvement is still needed

10-bit SAR ADC for LumiCal
Dynamic measurement results (@20 MS/s)

Example DFT Spectrum



Input frequency sweep



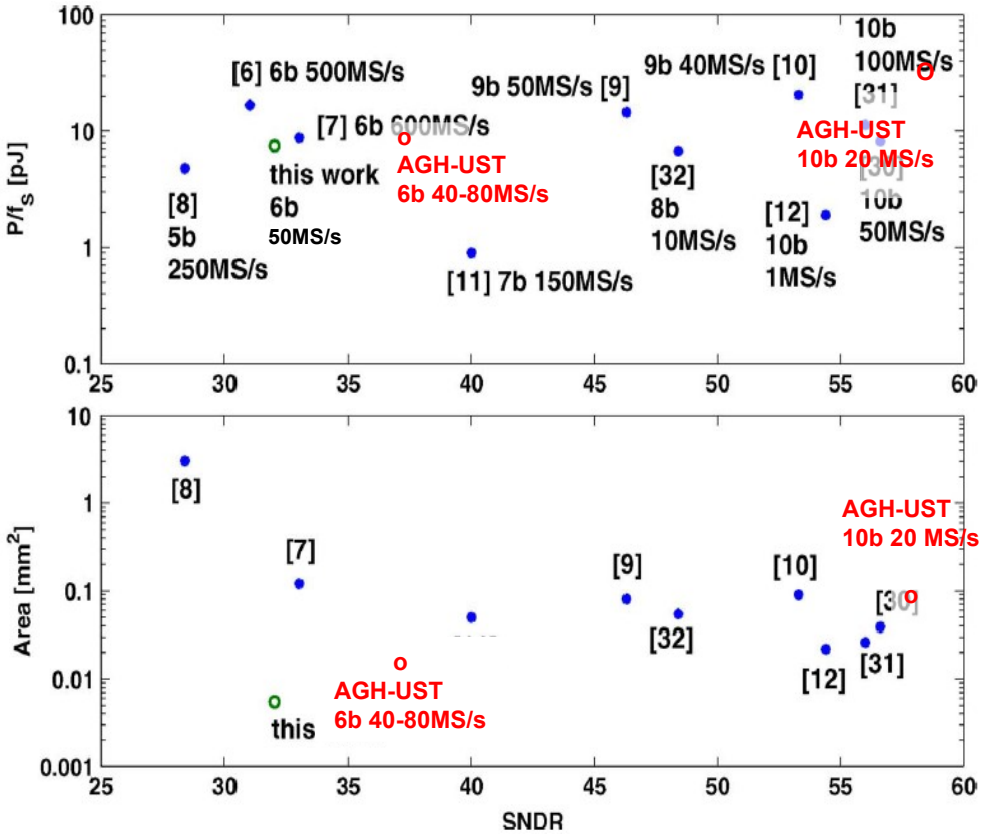
ENOB~9.3 up to Nyquist input frequency for f_{sample} ~20MHz

ADC works for f_{sample} beyond 40 MS/s, but above 20 MS/s ENOB start to decrease.
Problem with jitter above 20 MS/s found..., will be fixed in next submission.

Prototypes of SAR ADC vs State-of-the-Art
Performance of first prototypes

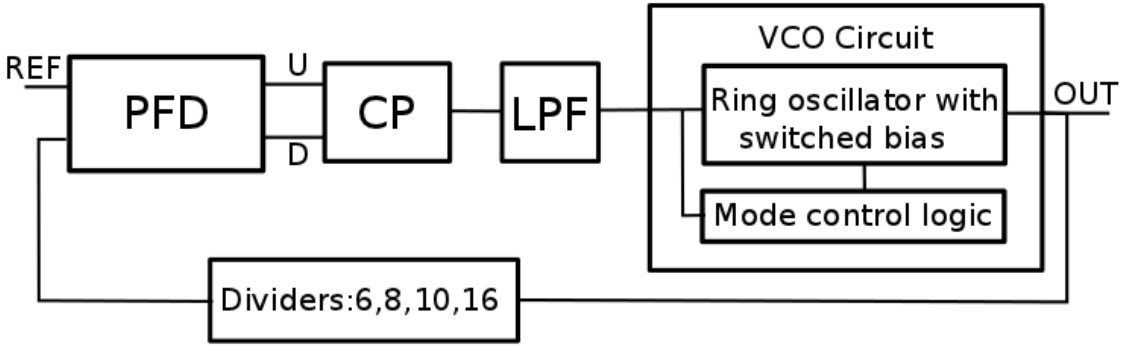
Main features:	LHCb	LumiCal
• Resolution [bits]	6	10
• Sampling frequency [MS/s]	>80	20 (50*)
• Power cons. [mW] @ 40 MS/s	0.35	1
• Size [mm^2] Dim. [µm]	0.016 40 x 400	0.087 146x600
• DNL/INL [LSB]	<0.4	~1.0
• SINAD@40MS/s [dB] ENOB [bits]	37.5 5.8	>56 9.3
• FOM [fJ/conv]	~150	~50

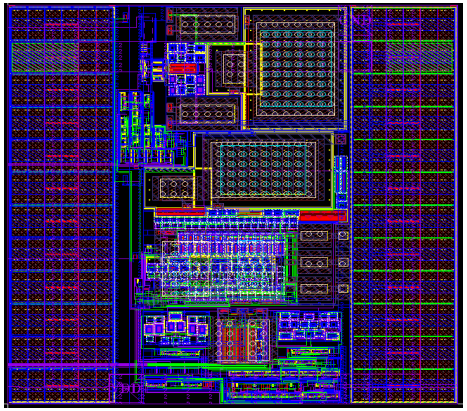
Performance of **our ADCs** is similar to **State-of-the-Art designs**



AGH-UST data were added to Table taken from "this work" :
P.Nuzzo, C. Nani, at el.,*"A 6-Bit 50-MS/s Threshold Configuring SAR ADC in 90-nm Digital CMOS"*,
IEEE Trans. On Circuits and Systems I vol.59 pp.80-92 January 2012

Low power PLL in 130 nm CMOS Architecture and specifications





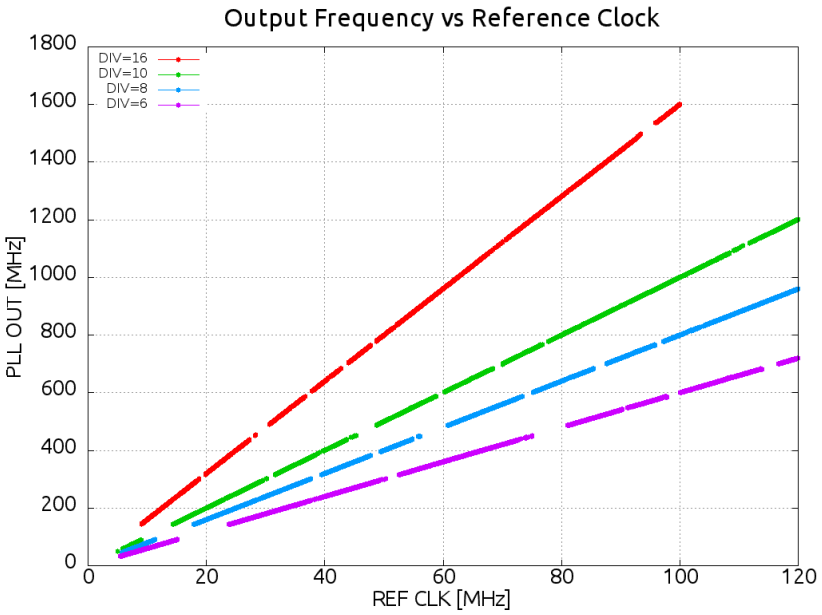
300 x 300 um

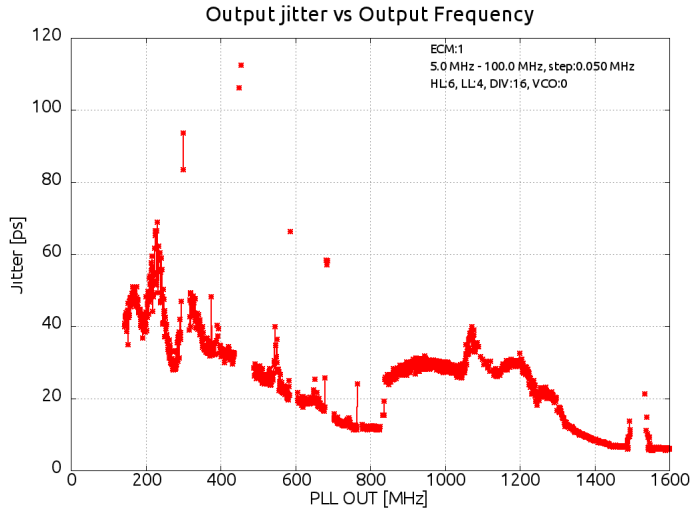
PLL features:

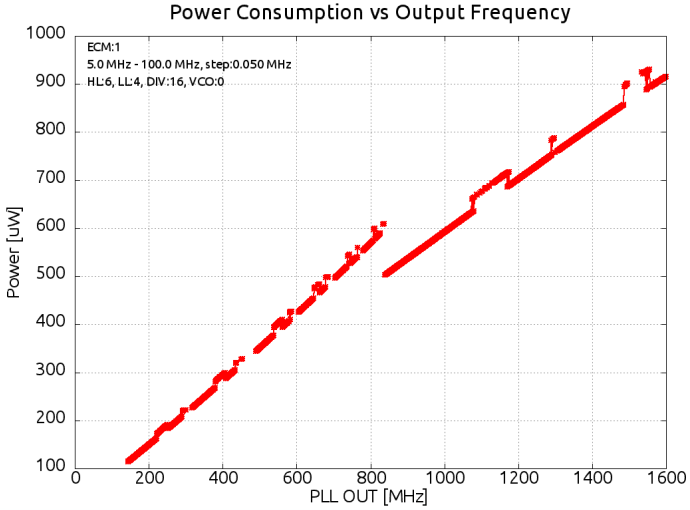
- General purpose PLL block
- Very wide output frequency range (10MHz – 3.5GHz)
- 16 VCO modes - Automatically (or manually) changed
- Power consumption ~0.6mW@1GHz
- Different loop division factors: 6,8,10 and 16

M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Swientek, "Development of scalable frequency and power Phase-Locked Loop (PLL) in 130nm CMOS technology", TWEPP2013 23-27 September 2013, Perugia Italy

Low power PLL in 130 nm CMOS Measurements







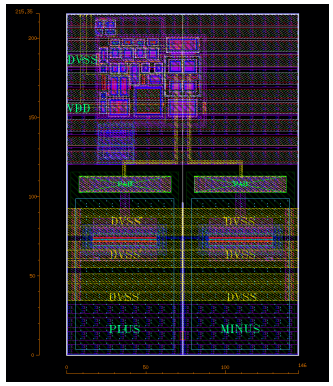
- Measurements confirm proper circuit operation in frequency range 20MHz-1.6GHz
- All four division factors work properly
- Power consumption scales linearly with PLL clock frequency (two rings → two curves)
- Gaps in frequency and Jitter need to be improved

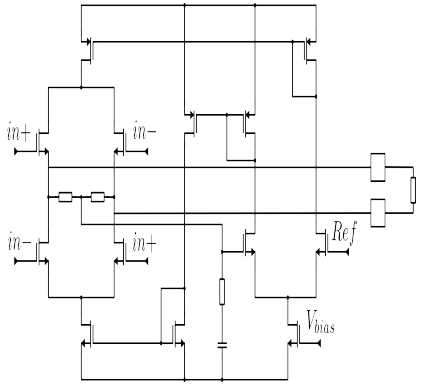
Multichannel ADC aspects
Design of SLVS interface

Specifications:

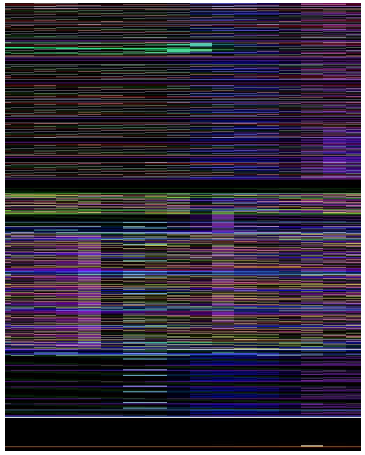
- Architecture
  - Driver – based on Boni paper
  - Receiver – based on self-biased amplifier (Bazes paper)
- Technology – CMOS 130 nm
- Maximum frequency ~1GHz
- Pitch matched to pads. Driver/receiver integrated with 2 pads (146um pitch)

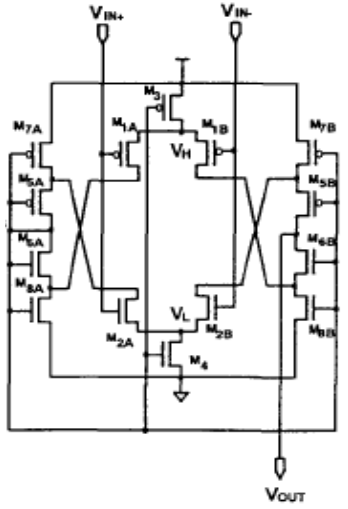
Driver





Receiver





Functionality verified during ADC and PLL test up to ~1.5 GHz. Dedicated quantitative tests not yet done (waiting in line...)

Summary

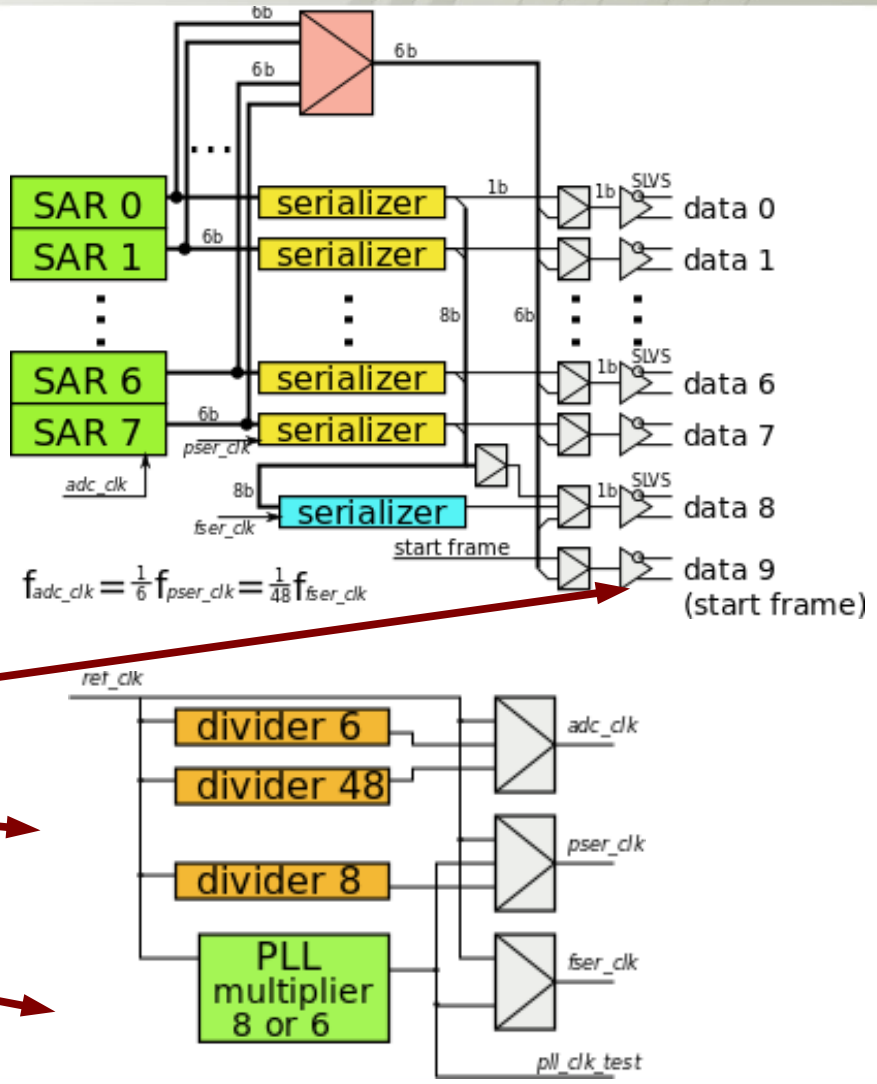
- Two low power ADCs (6-bit, 10-bit), general purpose PLL and SLVS interface were designed in 130 nm, fabricated and tested.
- All blocks are fully functional, quantitative tests show excellent results for 6-bit ADC and good results for 10-bit ADC and PLL.
- Improved versions were submitted in February 2014

Thank you for attention

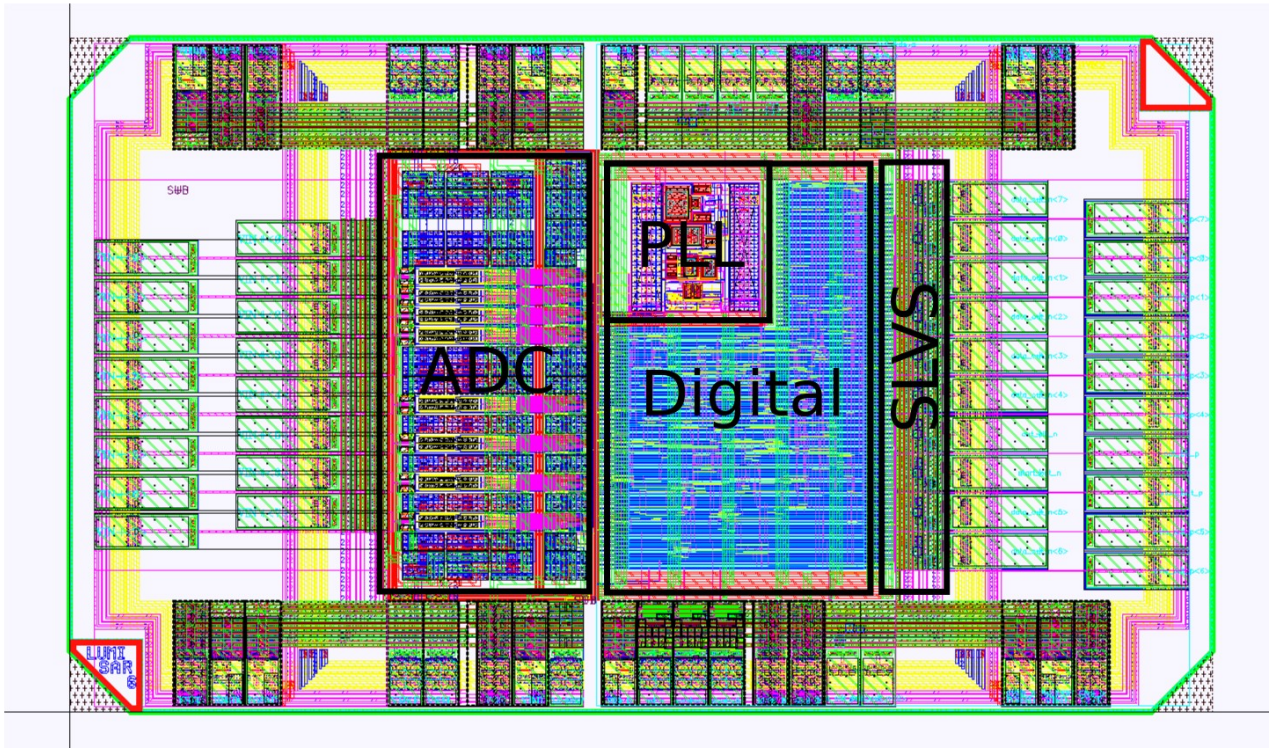
Multichannel SAR ADC with serialization Architecture

Specifications & implementation issues:

- 8 channels of 6-bit SAR ADC
- Technology 130 nm CMOS
- Multimode digital multiplexer/serializer:
  - Full serialization: one data link per all channels (external clk division or PLL clk generation)
  - Partial serialization: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channel output (max fsmp ~50 Msps)
- High speed SLVS interface (>1GHz)
- Multiple clock generation schemes (with or without PLL)
- PLL for data serialization
- Power pulsing



6-bit SAR ADC
Layout of prototype ASIC



2340um x 1380um

ADC prototype contains:
- 8 channels of 6-bit SAR ADC in 40um pitch
- Multiplexing&Serialization circuitry
- PLL prototype (discussed later...)
- SLVS I/O circuitry (discussed later...)
- Staggered pads

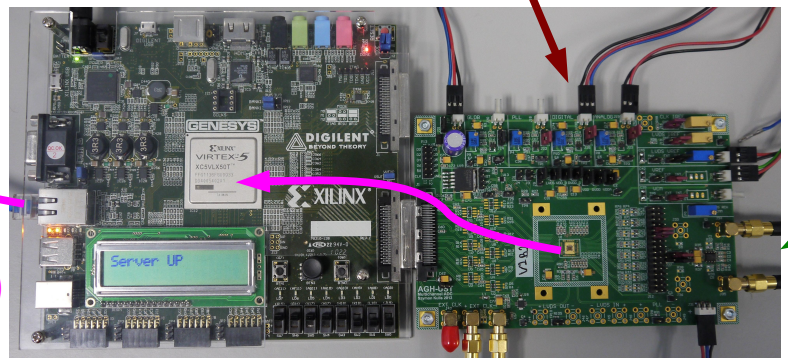
Prototypes were fabricated in 2012. FPGA based test setup was developed.
Measurements of ADC performance have been completed...

ADC testing
Measurement setup

DFT and data analysis – custom software

Power supply

Differential function generator – Agilent 81160A

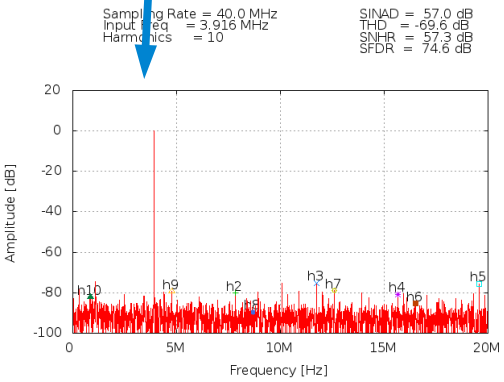


Input sine

Sample clock

Results

Sampled data (**low bitrate**)



Sampled data (**high bitrate**)

DAQ – receives fast transmission from ADC (up to 500 Mb/s), captures the data and sends to PC via Ethernet for offline analysis