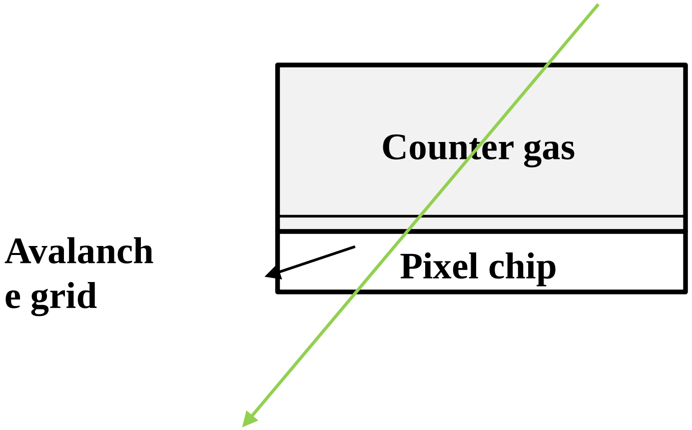
SPIDR, a readout for Timepix3

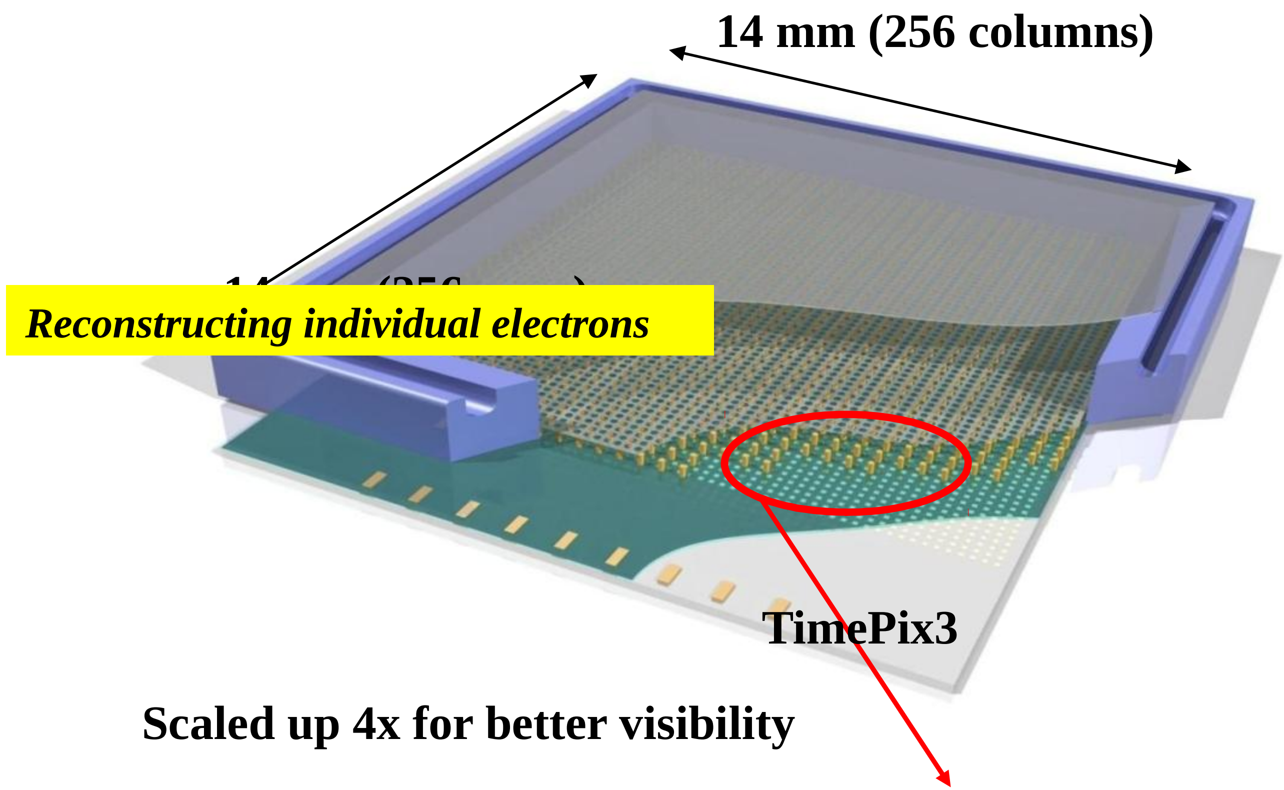
AIDA 3rd annual meeting
26 March 2014

Bas van der Heijden, Frans Schreuder, Henk Boterenbrood, Vladimir Gromov, Harry van der graaf, Fred Hartjes, Martin van Beuzekom, Nigel Hessey, Szymon Kulis, Joop Roeverkamp, Jan Visser
And the Medipix3 collaboration + Bonn university

Gridpix: gaseous pixel detector

- Interaction volume (gas)
- Amplification grid for avalanche
- High granularity pixel ASIC (55 μm)





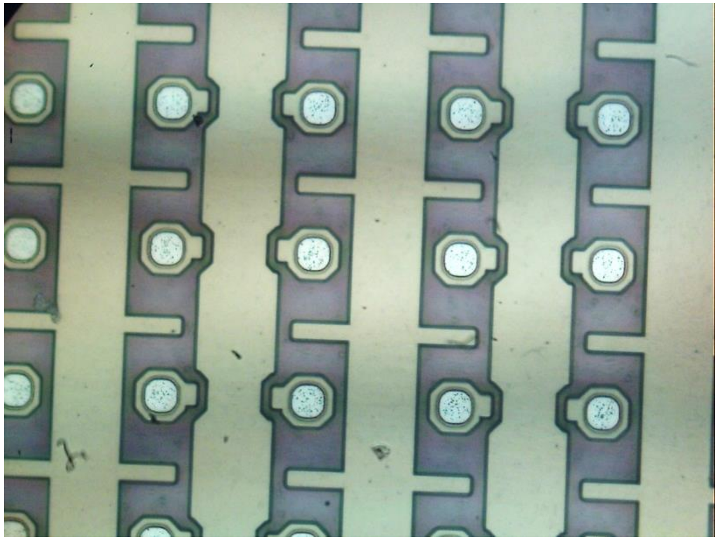
Scaled up 4x for better visibility

Timepix3

- Developed by CERN Medipix3 group, Nikhef and Bonn university
- Follow up of Timepix
- Same geometry, 256x256 pixels, 55 μm pitch, 1.4x1.4 cm2

New features:

- Faster front-end
- Simultaneous time and charge measurement
  - Time of Arrival (ToA) with 1.56 ns resolution, range 409.6 μs
  - Charge via Time over Threshold (ToT)
- Zero suppressed readout
- Data driven, max 40 Mhits/cm2/s
  - Shutter based readout still possible



Timepix3 versus Timepix

	Timepix (2006)	Timepix3 (2013)
Pixel arrangement	256 x 256	
Pixel size	55 x 55 μm²	
Technology	250nm CMOS - 6Metals	130nm CMOS - 8Metals
Acquisition modes	1) Charge (iTOT) 2) Time (TOA) 3) Event counting (PC)	1) Time (TOA) AND Charge (TOT) 2) Time (TOA) 3) Event counting (PC) AND integral charge (iTOT)
Readout Type	1) Full-Frame	1) Data driven (DD) 2) Frame (FB)
Zero suppressed readout	NO	YES
Dead time per pixel	> 300μs readout time of one frame	> 475ns **~600x** Pulse measurement time + packet transfer time
Minimum timing resolution	10ns	1.562ns **6.4x**
On-chip Power pulsing (PP)	NO	YES
Minimum detectable charge	~750e-	>500e- **1.5x**
Output bandwidth	1 LVDS ≤200Mbps 32 CMOS ≤3.2Gbps	1 to 8 SLVS @640Mbps DDR ≤5.2Gbps **1.6x**

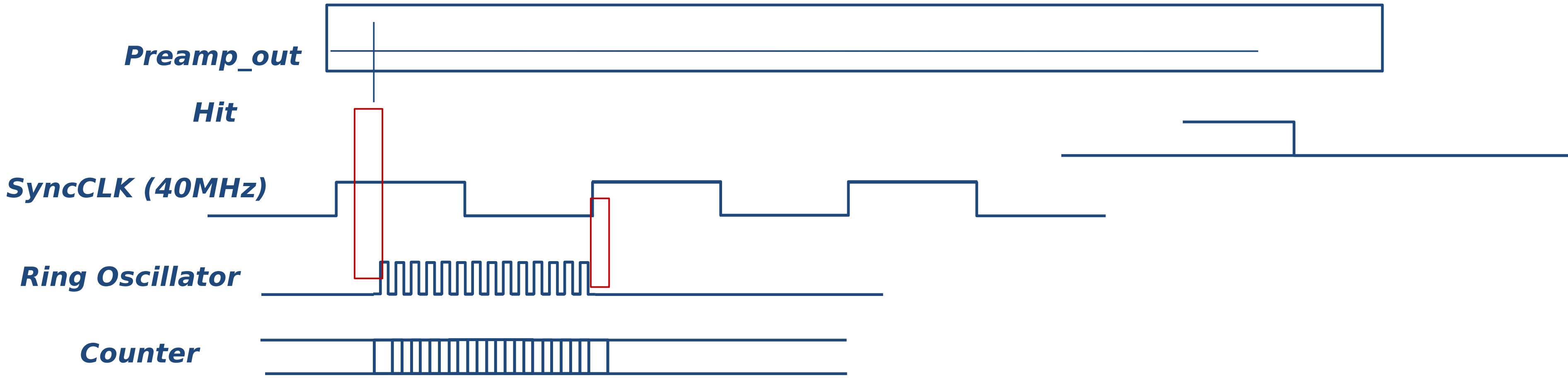
frame based (>> 100x for tracking)

Timepix3 has many modes / features

Timepix (2006)

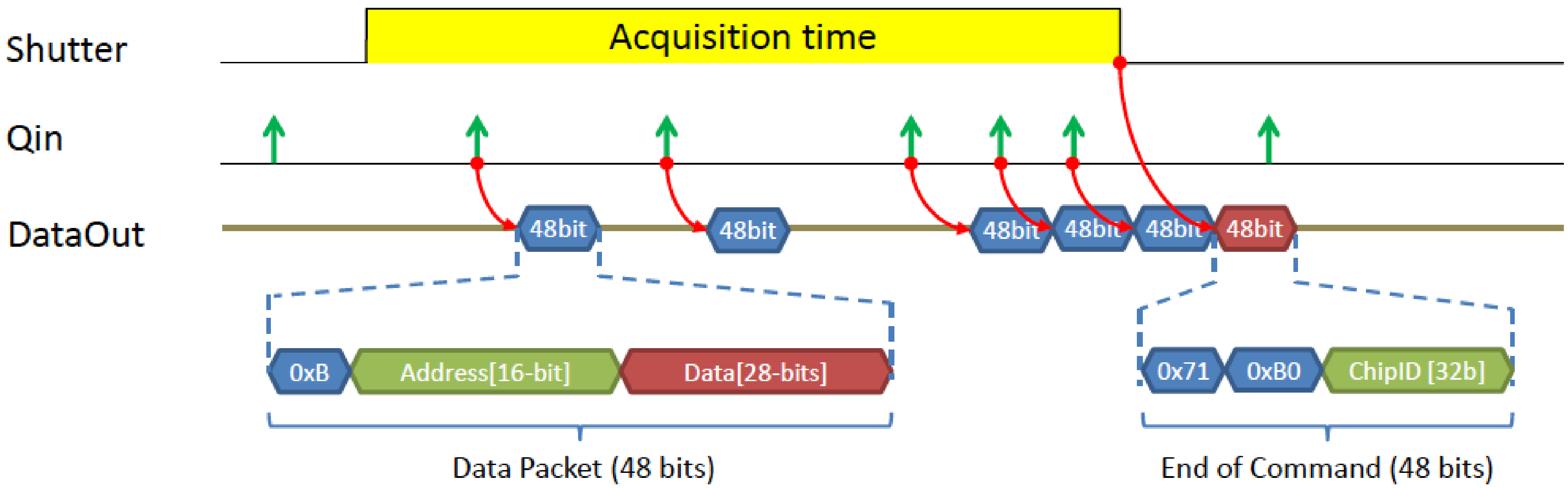
Timepix3 (2013)

Time measurement



- **4-bit fast time measurement till first clock edge of 40 MHz clock**
- **+ 14 bit ToA counter at 40 MHz**
  - **range 409 μs**
- **ToT counter at 40 MHz**
  - **10 bit range**
  - **Preamp discharge rate configurable**

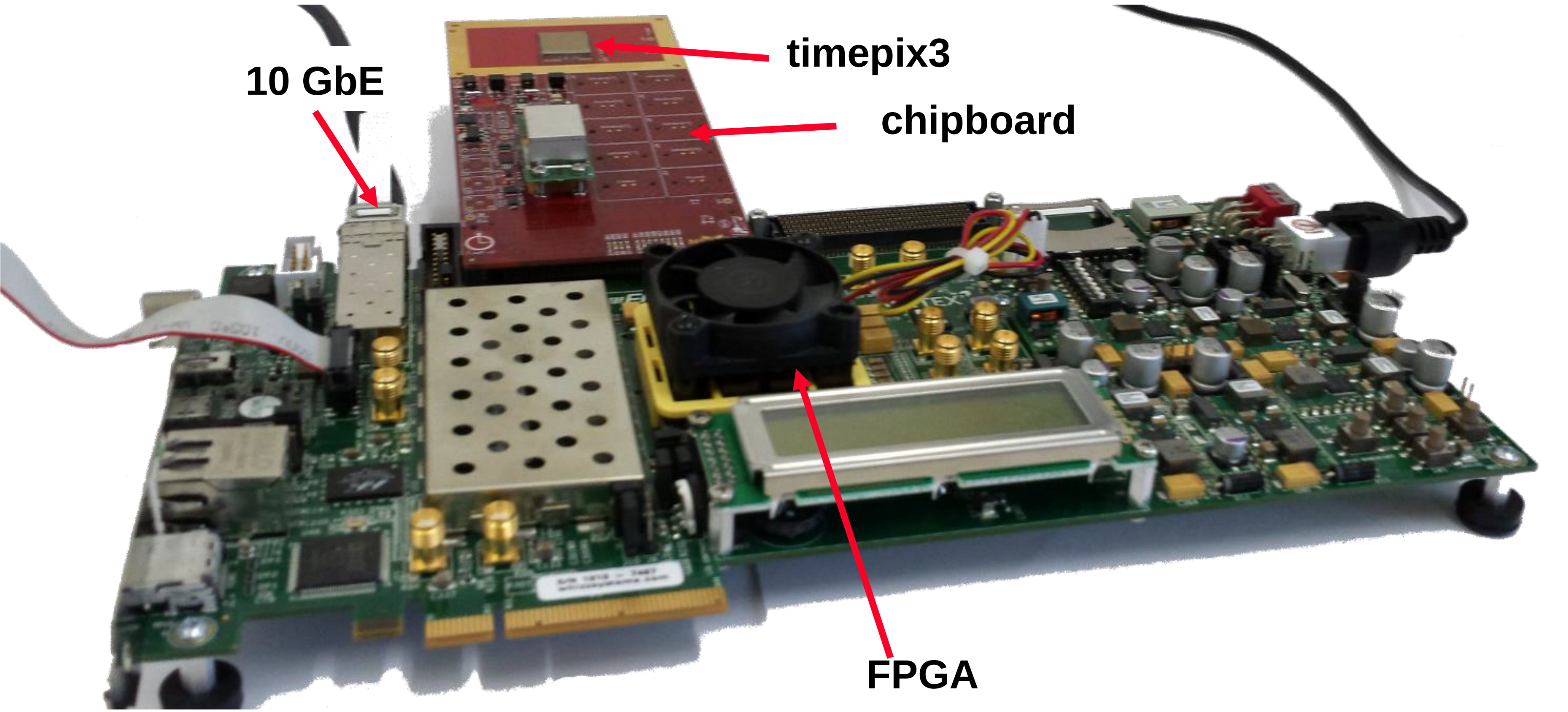
trigger-less, data driven readout



- **Each pixel hit gives a 48 bit data packet with address, ToA and ToT**
- **SPIDR readout adds 16 bit coarse timestamp, -> 64 bit packets**
  - **range 26.8 sec**
- **Max. count rate (homogeneous illumination): 40 Mhits/cm2/s**

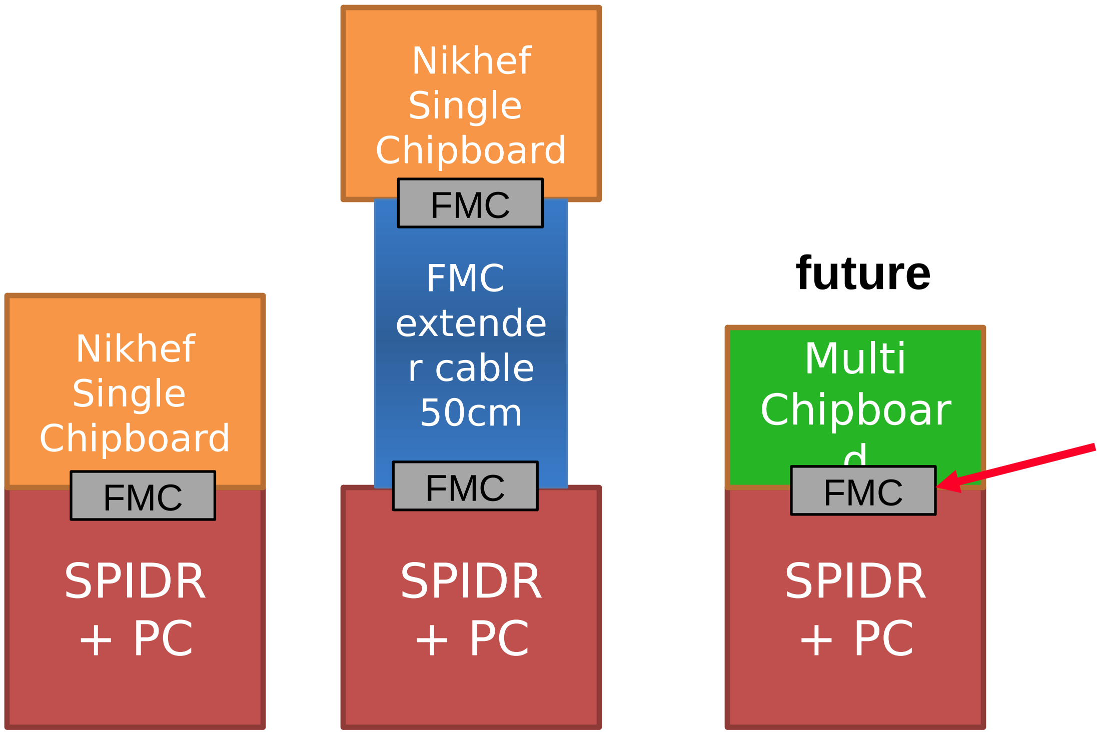
SPIDR

- **Speedy PIxel Detector Readout**
- **Developed on Xilinx VC707 evaluation board**
  - **Dedicated board under development: Compact SPIDR**
- **Fully working system, used for TPX3 characterisation and wafertest**
  - **additional features being added**



SPIDR

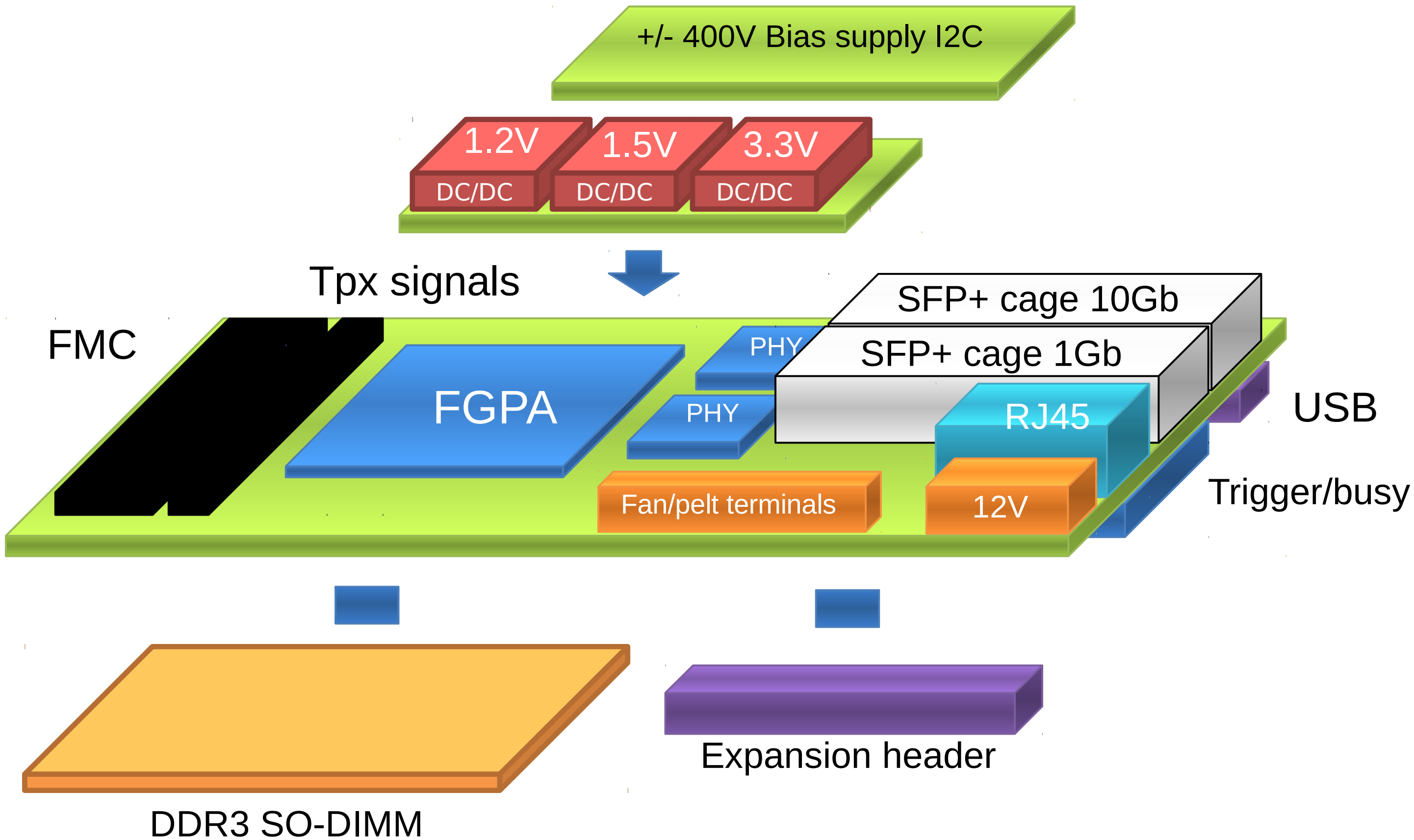
- **Each SPIDR is connected to its own DAQ PC via 10 Gbit ethernet**
  - **Max. bandwidth of 1 TPX3+overhead = ~ 6 Gb/s**
  - **Max speed continuous data-streaming requires solid state disk array**
  - **At lower rates you can use 1 PC for multiple SPIDRs**
- **C++ software library (DAC + control) available**



- **FMC connector has 8 data lanes**
- **readout one TPX3 at max speed**
- **or up to 8 TPX3s at lower speed**

Compact SPIDR

- More compact (~ 7x15 cm2) and cheaper than VC707 based SPIDR
- PCB layout started
- Expect to have tested boards available late summer



Extensions to SPIDR firmware

- **Add external trigger input for T0 signal**
  - **Aim for sub nanosecond resolution (t.b.c.)**
  - **Data packets with trigger timestamps will be merged with DAQ stream**
- **Add 1 Gbit ethernet interface**
  - **Intended for monitoring stream (spy data) at high rate running**
  - **both DAQ and monitoring stream can be sent to 1 or 10 GbE, allows running at 1 GbE with e.g. laptop**
- **Readout of Timepix(1)**
- **Readout of Medipix3**

How to interface with SPIDR

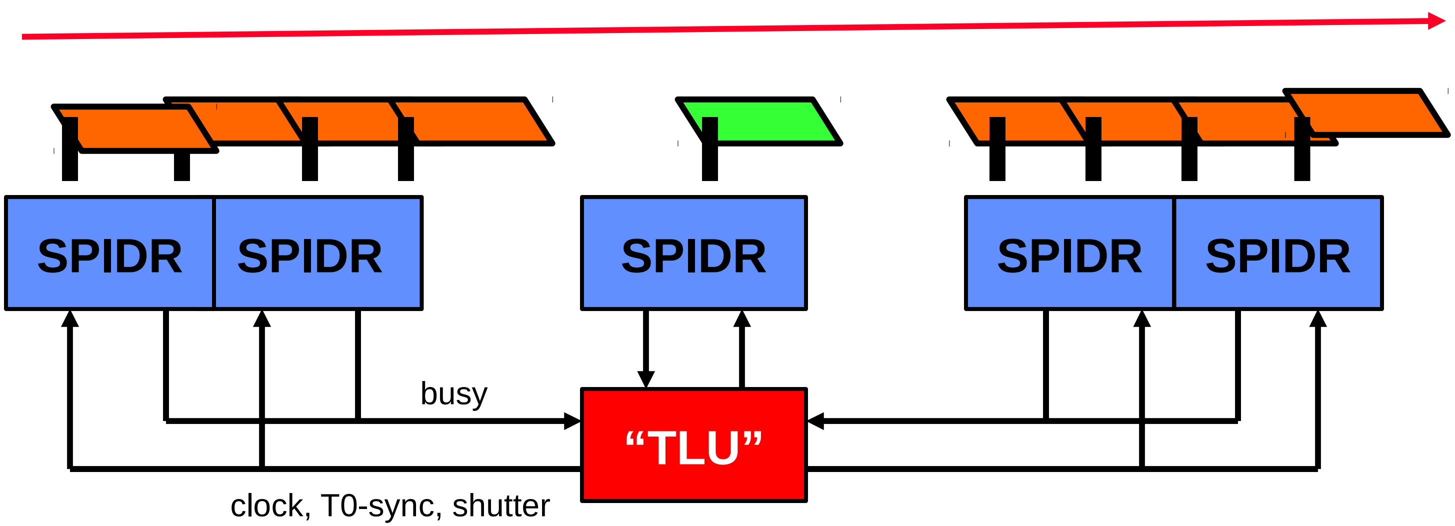
- SPIDR runs without trigger, continuous stream of time-stamped hits
- However gaseous detector typically require T0 timestamp (scintillator)
  - Will be provided by external trigger input on SPIDR
  - Does not trigger the TPX3, but only provides extra timestamps to the DAQ stream
- Readout of multiple SPIDRs requires a central logic unit
  - We plan to use TLU (Trigger Logic Unit) boards developed by Bristol university

4 signals:

  - Distributes master 40 MHz clock to SPIDRs
  - Distributes T0-sync to synchronise timestamps (sent from master SPIDR)
  - Combine (OR) busy outputs of SPIDR; cuts shutter signal
  - Distributes shutter signal to all SPIDR boards

High rate telescope

- **Developed by LHCb VELO (upgrade) group**
  - **Usage by 'external' users envisaged**
- **2 telescope arms with 3 or 4 Si planes each, based on Timepix3**
  - **Active area 1.4 x 1.4 cm2**
  - **Expect ~ 2 μm pointing resolution at 100+ GeV beam**
- **High speed data driven SPIDR readout, > 10 M tracks/s (burst mode)**
- **Trigger Logic Unit (TLU) provides clock, T0-sync and handles busy/shutter handshake**
  - **TLU HW developed by Bristol university**



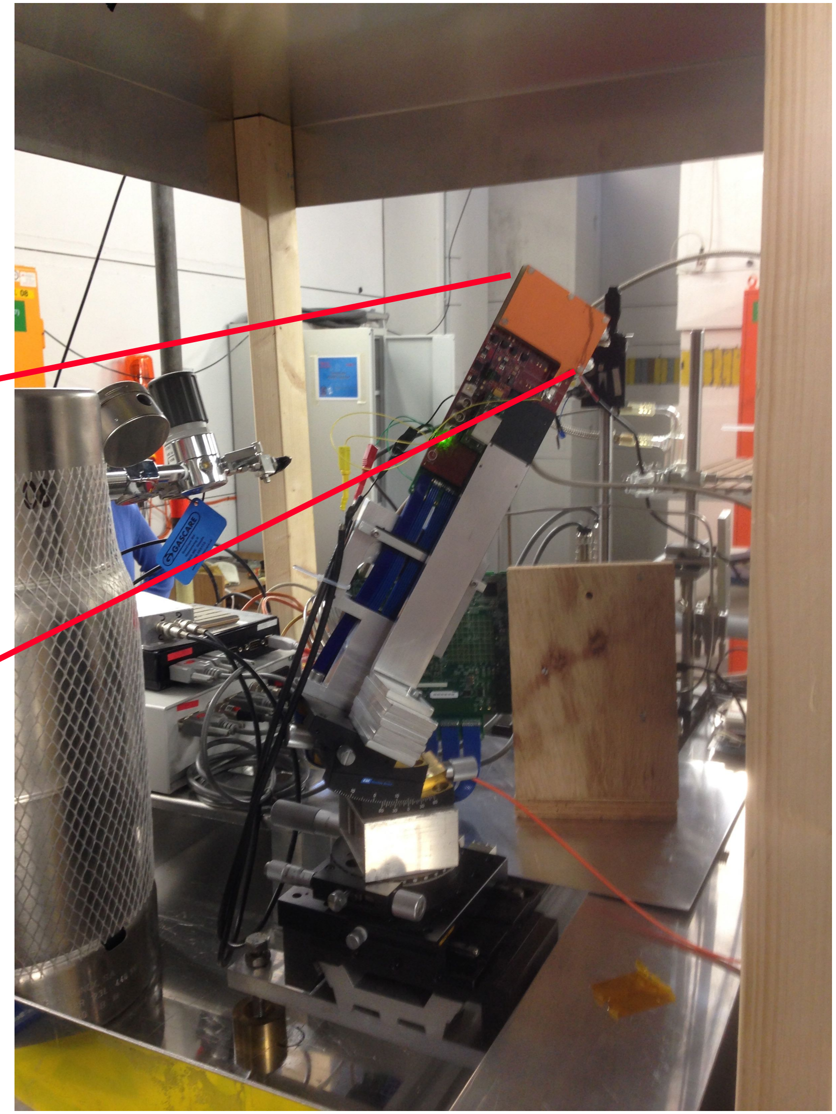
Telescope usage

What we envisage (being discussed):

- **The telescope provides a list of time-stamped tracks for ‘external users’**
- **Linking telescope tracks to data taken with non-TPX3 DUTs, could/should be done offline**
- **Synchronisation of data taking (Telescope and DUT) eases offline analysis**
  - **Use same 40 MHz clock**
  - **Use common T0-sync signal (sync input required on DUT readout)**
  - **Provide timestamps for 1 external input on the SPIDR (e.g. scintillator trigger)**

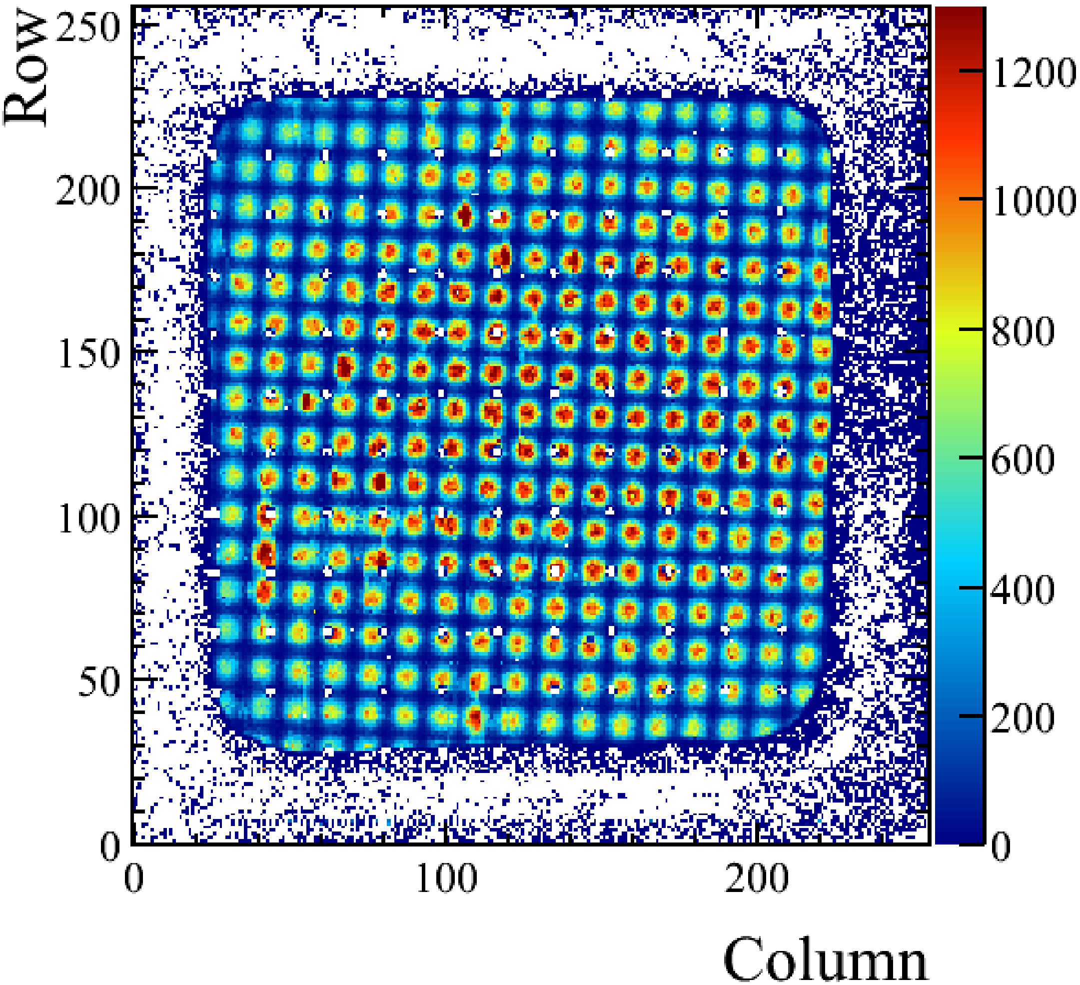
First tracks with Timepix3 + SPIDR

- DESY testbeam
- 2 GeV electrons, few kHz tracks
- ran with gas He/iC4H10 95/5
  and Ar/iC4H10 90/10

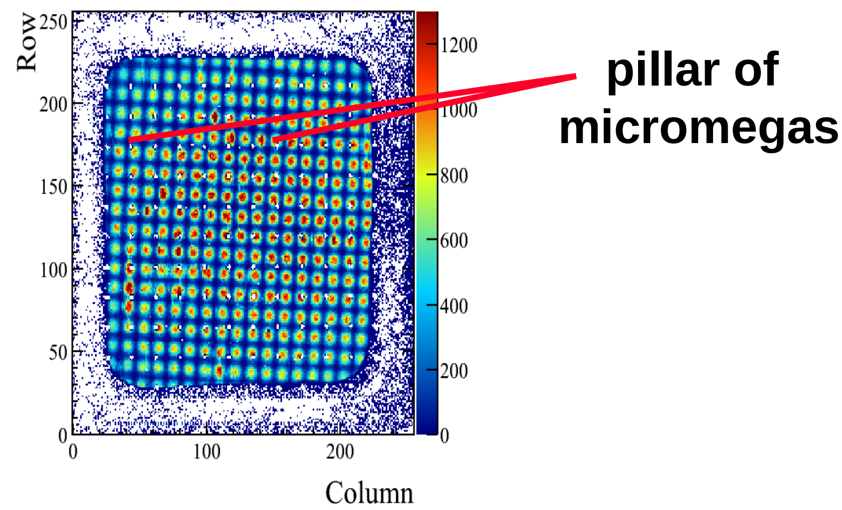


- Micromegas foil in frame
  - Pitch 60 µm
  - Does not match TimePix3 pitch (55 µm)
- Unprotected Timepix3

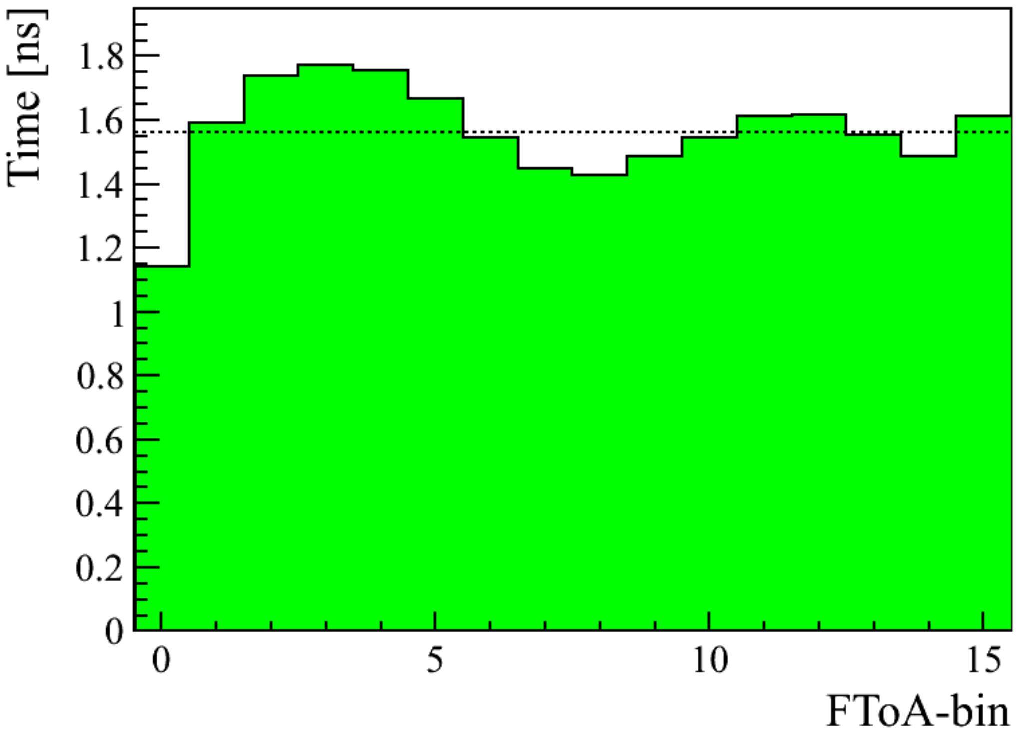
Hitmap



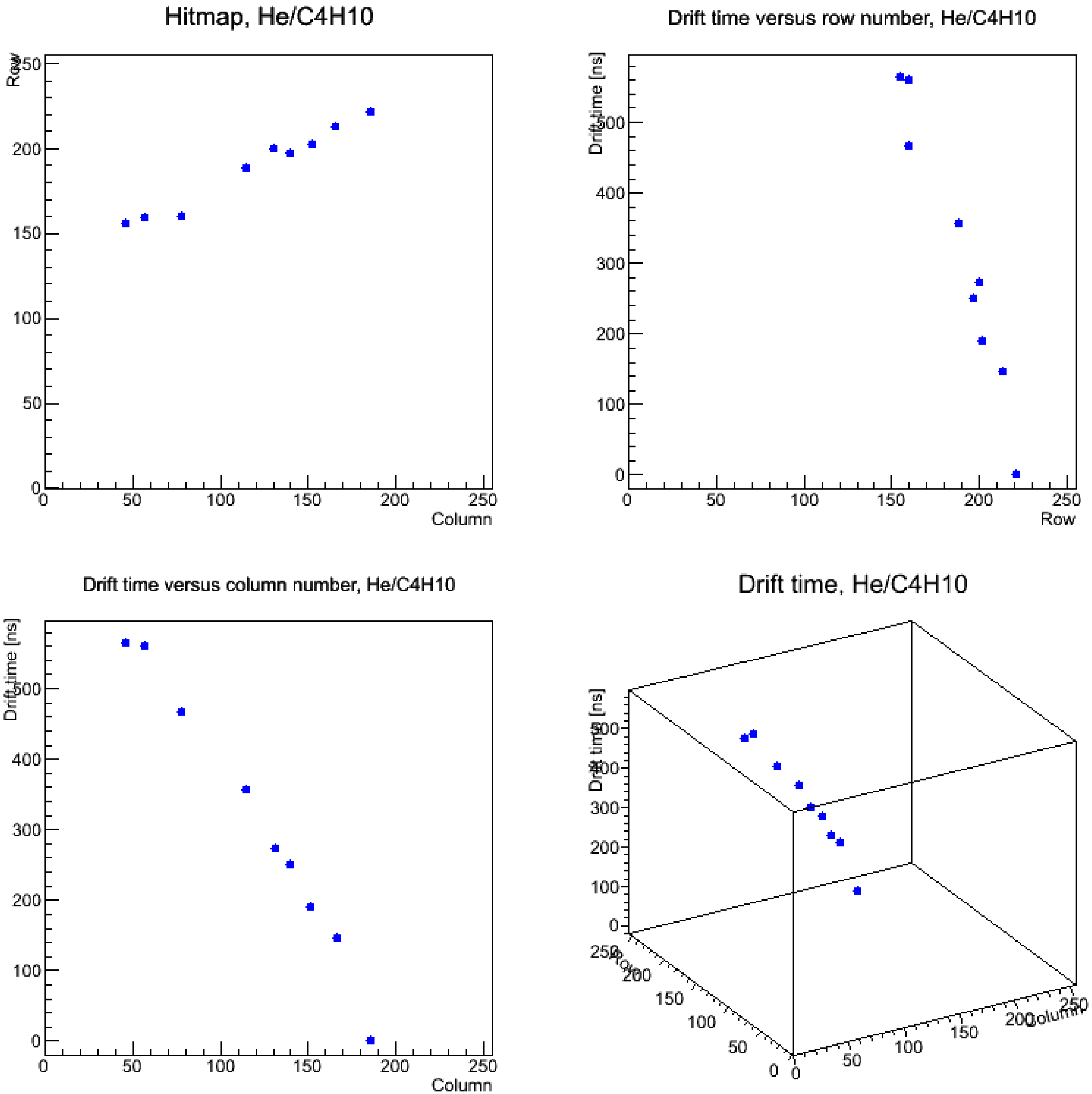
- few minutes data
- Moiré pattern due to mismatch of TPX3 and micromegas grid (55 and 60 μm, resp.)



Fast time measurement

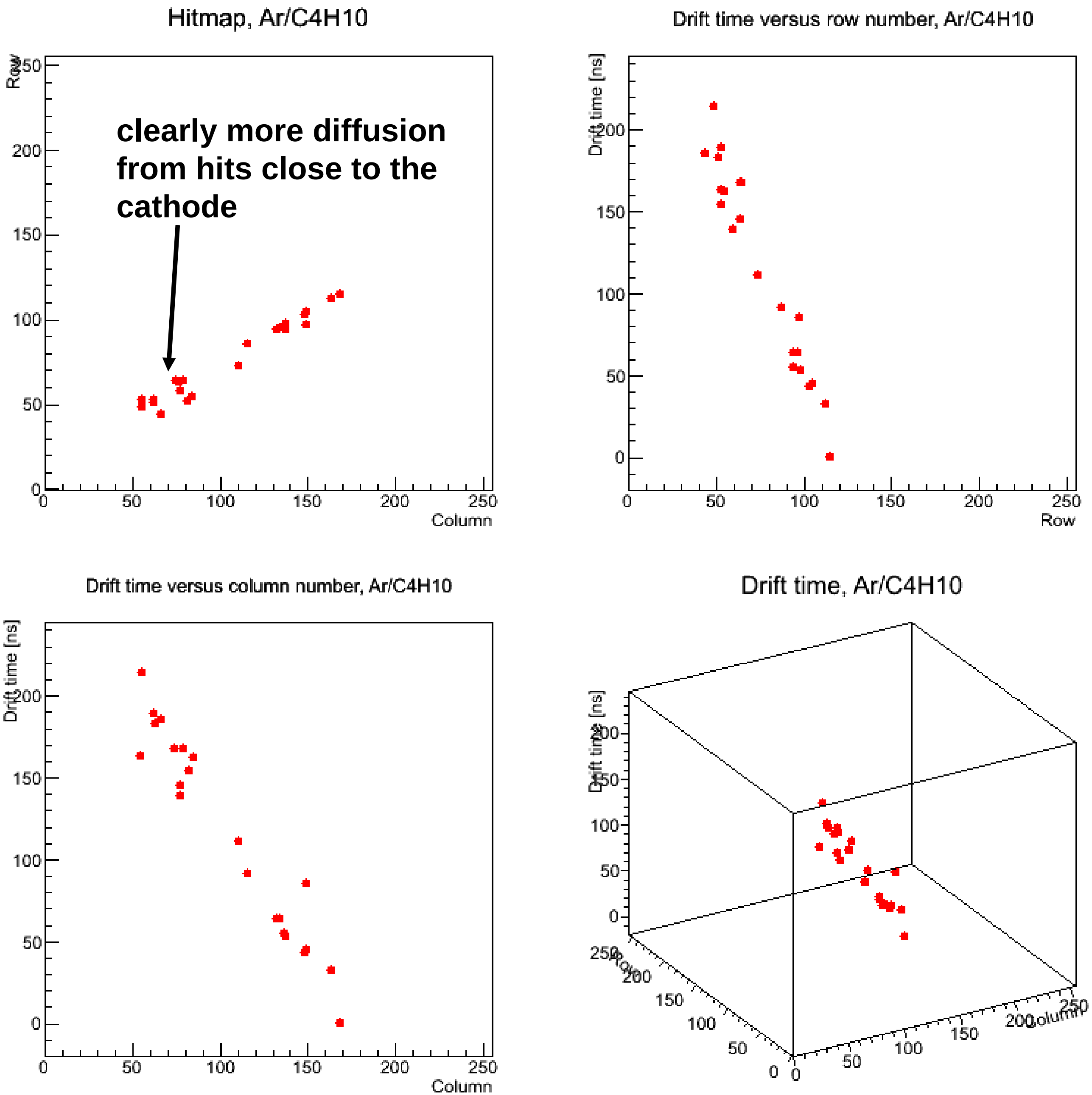


- **Continuous beam**
  -> arrival time is random
- **Should yield a flat distribution**
- **Smaller bin-0 is known behaviour**
- **Dashed line = ideal bin-size (=25ns/16)**



Track projections

He/iC4H10 95/5

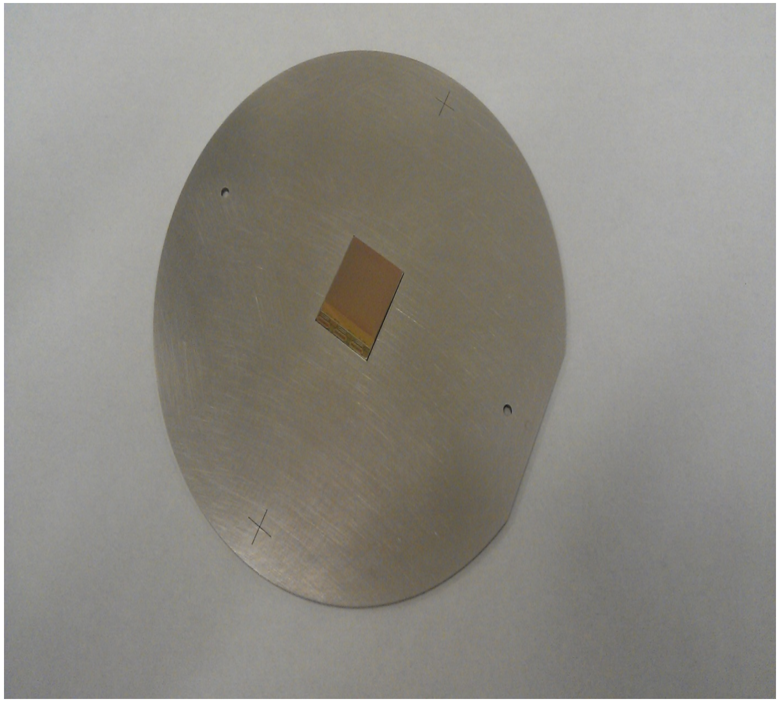


Track projections

Ar/iC4H10 90/10

Development of Ingrid on TPX3

- Chip with 4 μm SixNy protection layer finished (DIMES, Delft University)
  - To be tested with Micromegas as well
  - Using more suited gas mixture (DME/CO2) and higher gain
  - The Moiré pattern at different grid voltages will enable us studying the alignment tolerance of the holes of the grid to the pads



- In parallel MESA+ (University of Twente) is adding InGrid onto diced chips
  - We will use this opportunity to revise the photolithographic process