Status report on the development of a TPC readout system based on the SALTRO-16 chip and some thoughts about the next step

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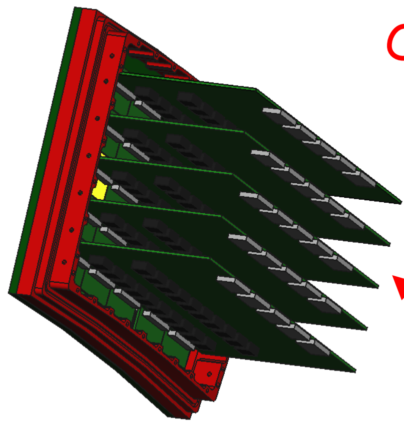
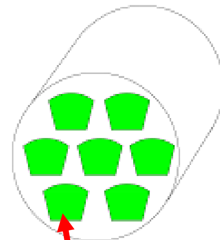
Overview of the SALTRO16 readout system

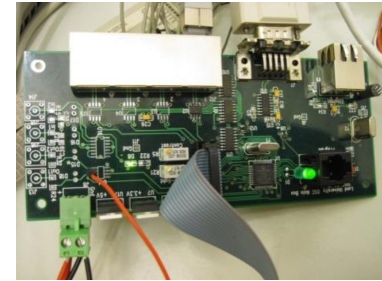


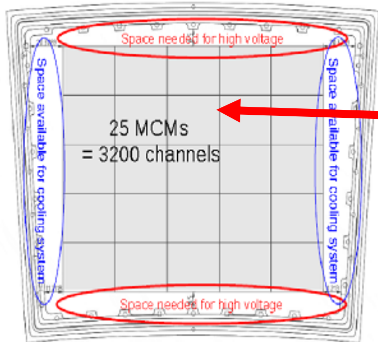
LowVoltage boards attached to one pad module



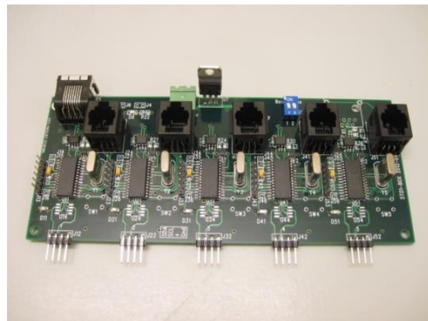
The Large Prototype TPC

Detector Control System – Master module





MultiChipModules on a pad module



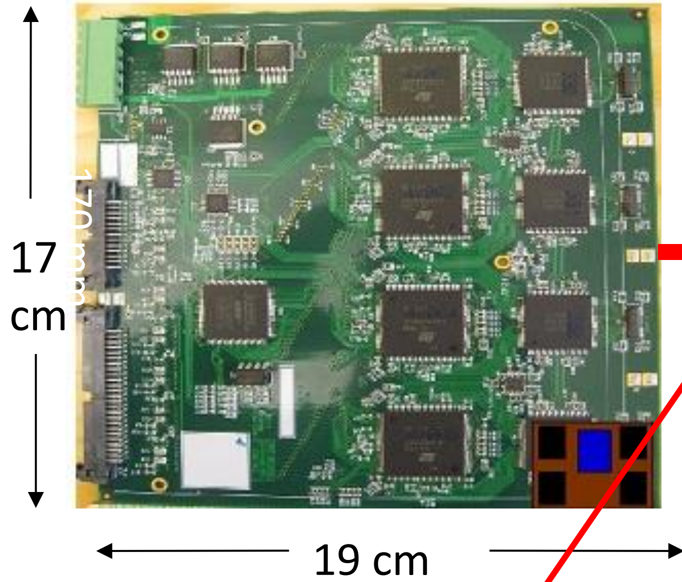
Detector Control System – 5to1 slave module

High Voltage
RS485 to control room
DCS Master
I2C < 50 cm
RJ45 < 5 meters
Power
DCS
5to1
Power
Low Voltage
Cooling
S R U
ALICE Date based?
Ethernet/UDP?
DDL?
Ethernet
Local DAQ/Monitor
Network
DOOCS
Detector Control
Common DAQ
Common TLU
Clk
Trig
Busy
Spill
Local Fanout Box
Trigger
Busy
Scint coinc
Power Pulsing
Other SRUs
Multi Chip Module (MCM)
Pad plane

Scalable Readout Unit (SRU)
LVDS
Serial Readout Unit
40 MHhz clock
Data
Trigger/Command
Reply
MCM1
MCM25
LVDS
Power pulsing
Busy
Trigger
40 MHz Clock

From ALTRO to SALTRO16
A decrease in size by a factor 40 of the front end electronics

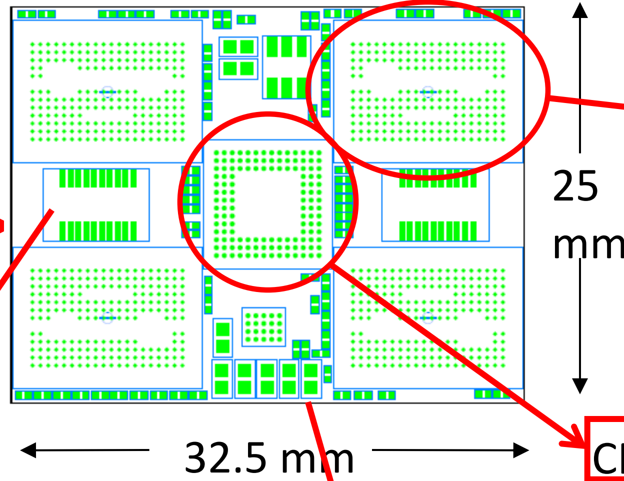
FEC with 8 ALTRO



17 cm

19 cm

MCM with 8 SALTRO
on carrier boards

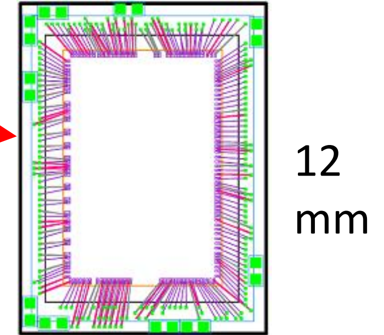


25 mm

32.5 mm

CPLD

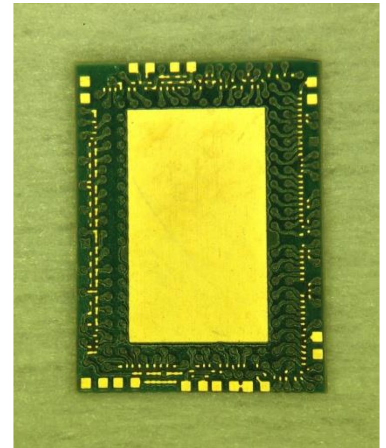
Carrier Board



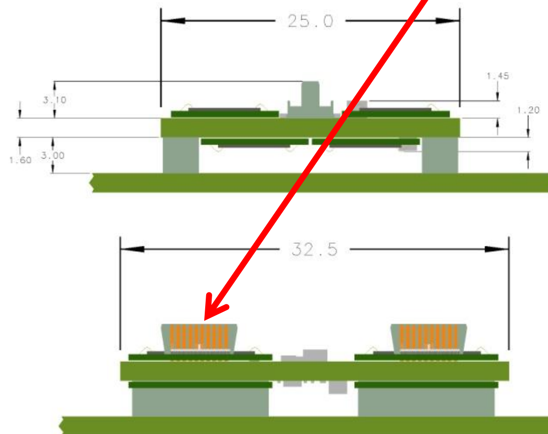
12 mm

8.9 mm

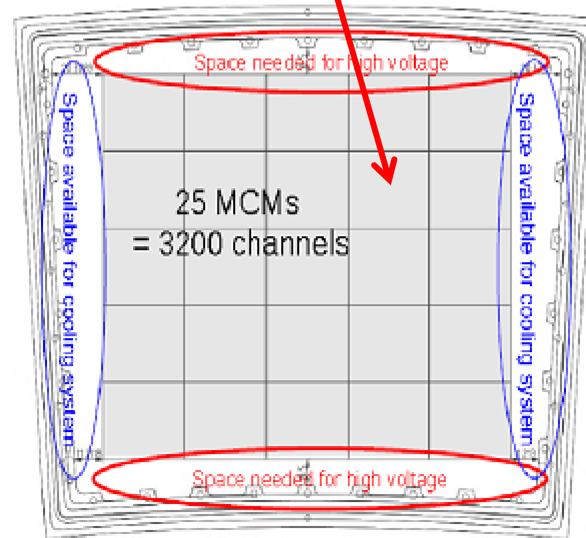
Carrier Board PCB



Side views of an MCM

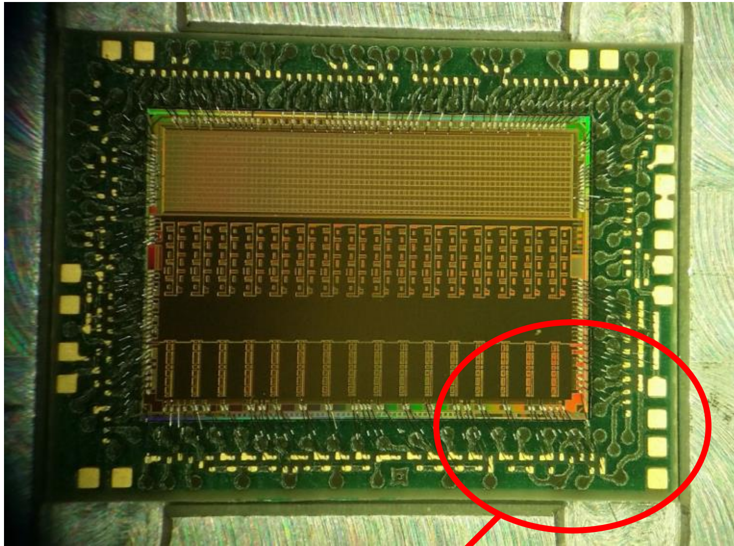


Pad Module

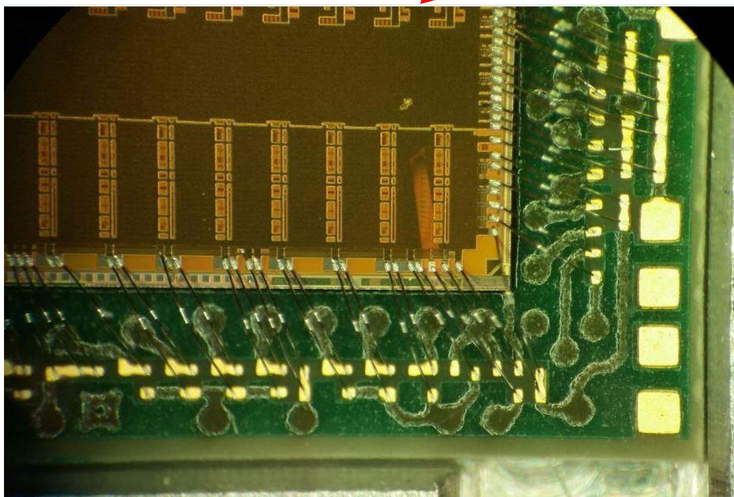


Status of the Carrier Board

Carrier Board with SALTRO chip mounted



Bottom side of the Carrier Board with tin balls

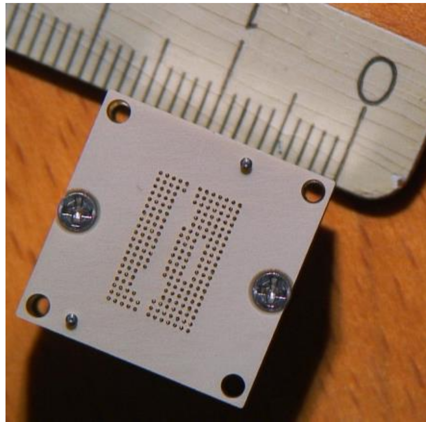


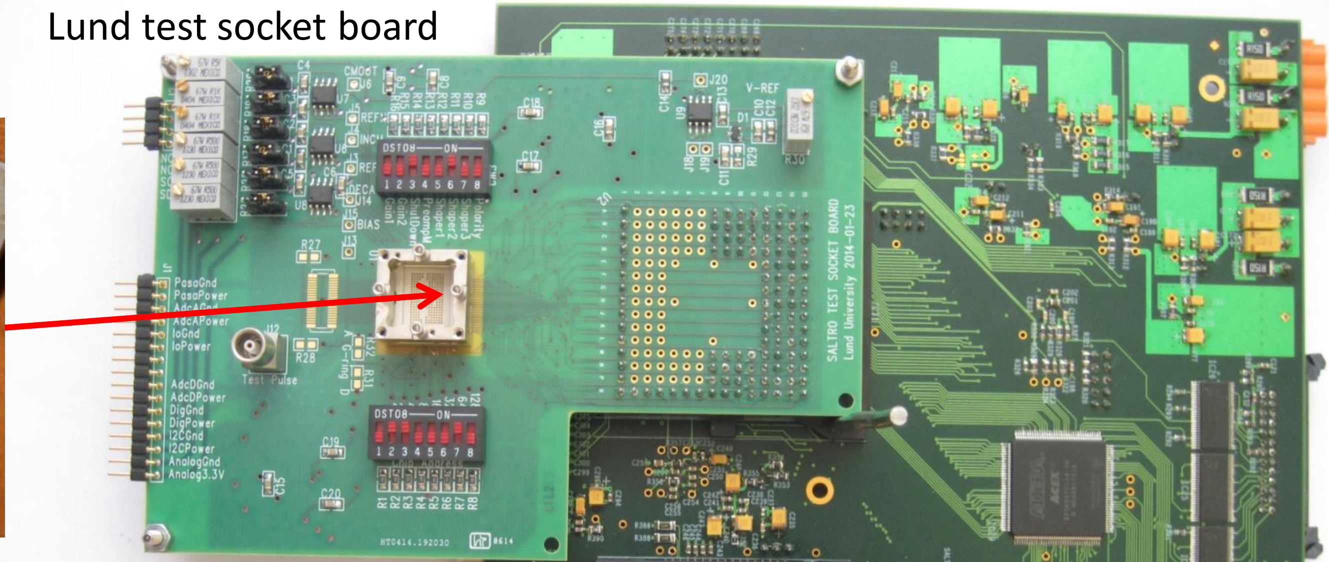
- A test sample of three Carrier Boards with bonded SALTRO-chips are ready
- There has been some problems with the application of the epoxy layer
- A new molding fixture had to be fabricated and new material with smaller surface tension had to be found

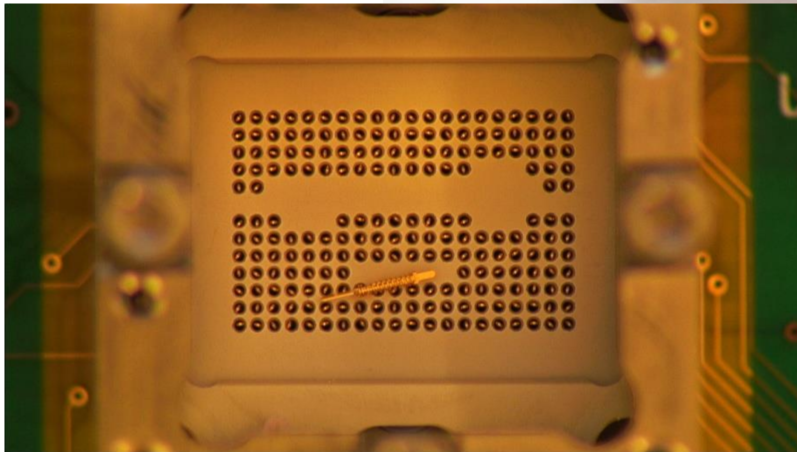
Test set-up for testing SALTRO16-chips on Carrier Boards

Lund test socket board

Test socket



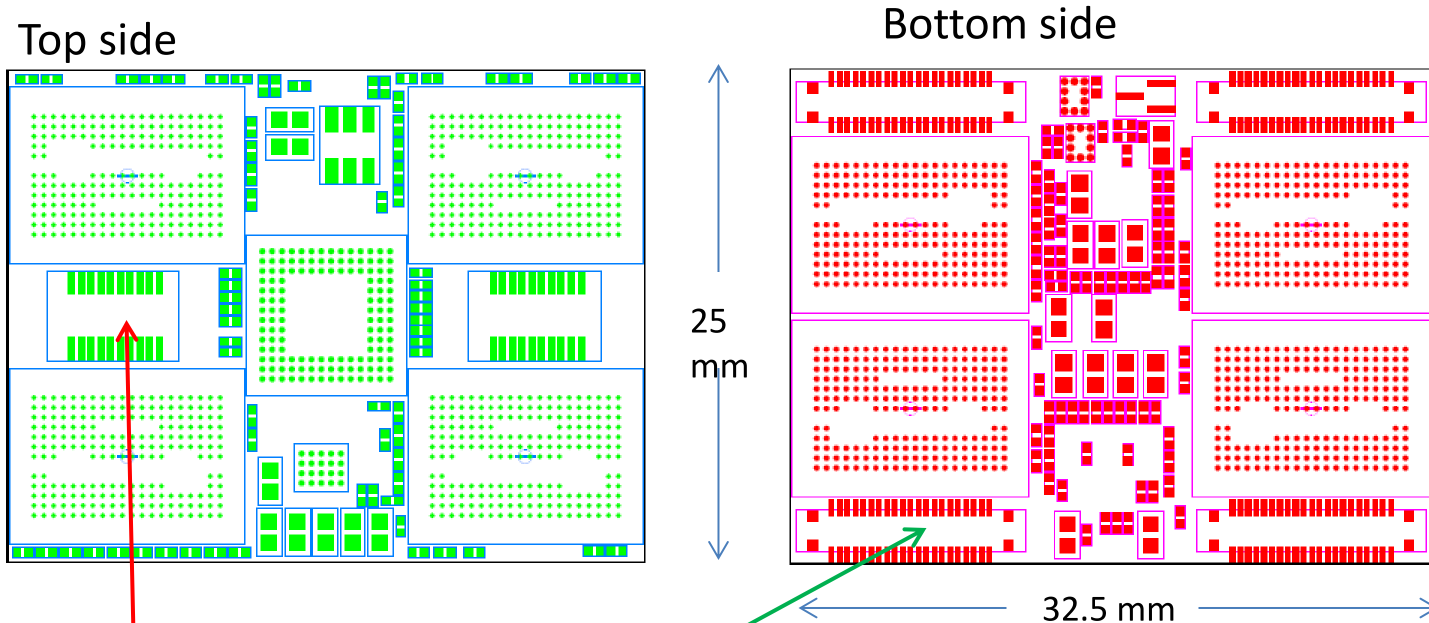




CERN test board

- Some modification of the CERN test board was necessary to fit our system
- The test set-up is assembeled and the communication to the CERN test board has been established with packaged SALTRO16 chips.

The final MCM-board

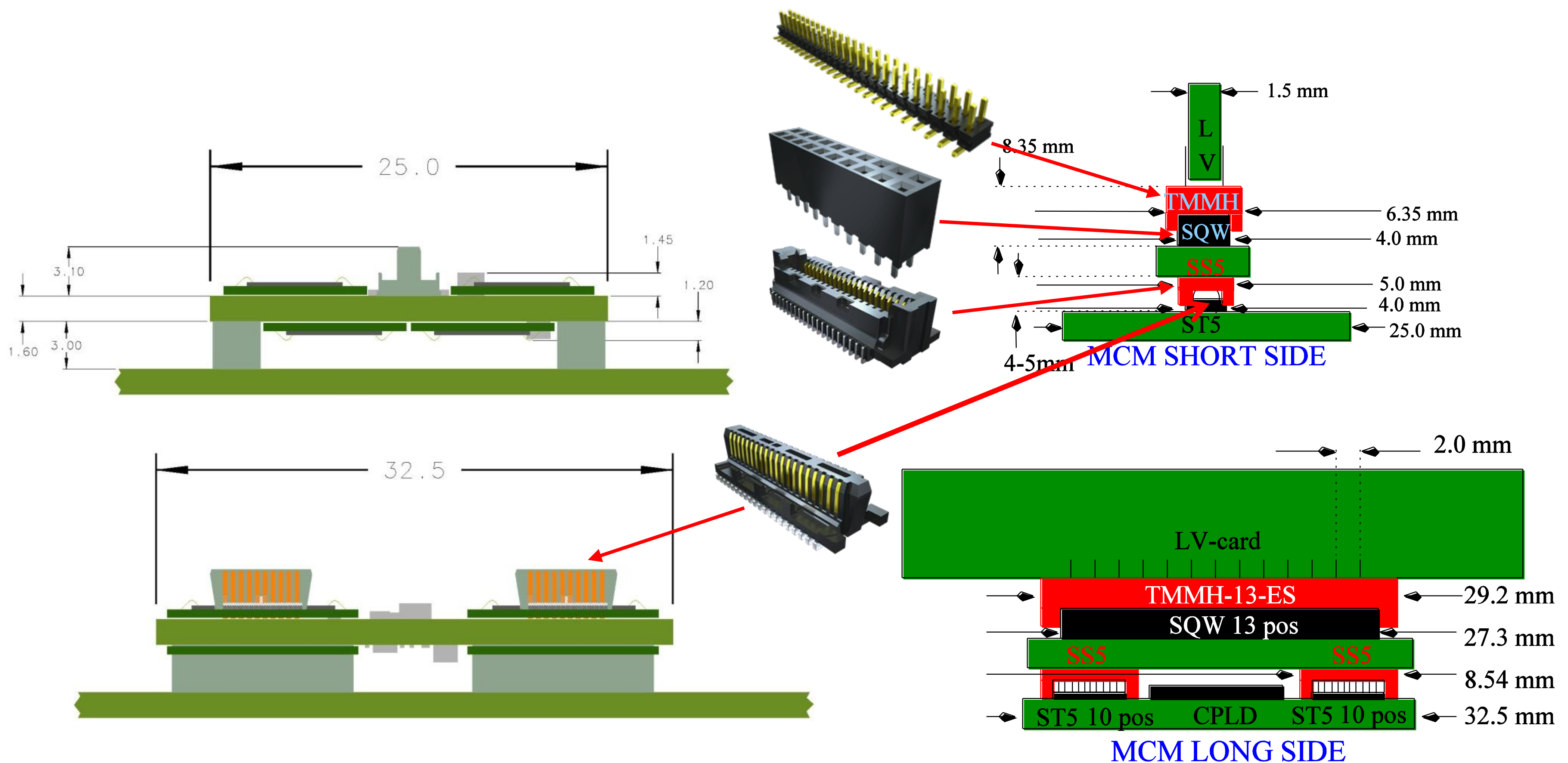


- The MCM-board will be redesigned in HDI-technology (High Density Interconnect) → The number of layers can be reduced (from 20 layers to 10 ?).
- This is a useful exercise for the design of the final front end electronics.
- The Panasonic connectors, which link the MCM-board to the padplane have arrived.
- The Samtec connectors on the top side of the board have also been delivered.
- We plan to produce a mock-up system to make sure that the mounting of the Carrier Boards and the connectors does not create problems.

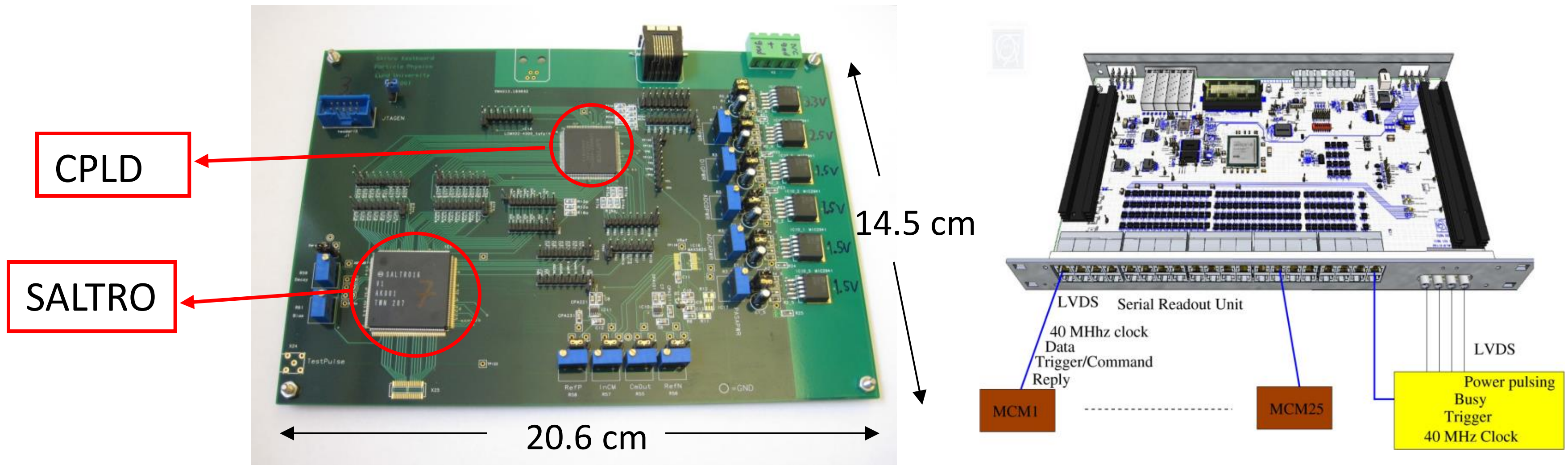
Complication with connectors

The problem with the male connectors on the upper side of the MCM-board is that the female partner can not be mounted on a vertical LV-board. This has forced us to introduce an adaptor board and a pair of additional connectors, which are suited for such mounting. The MCM-board plus the adaptor board can be regarded as a unit, which will not be separated.

The mock-up system will also be used to test that everything fits together



The MCM-development board (stand alone board)

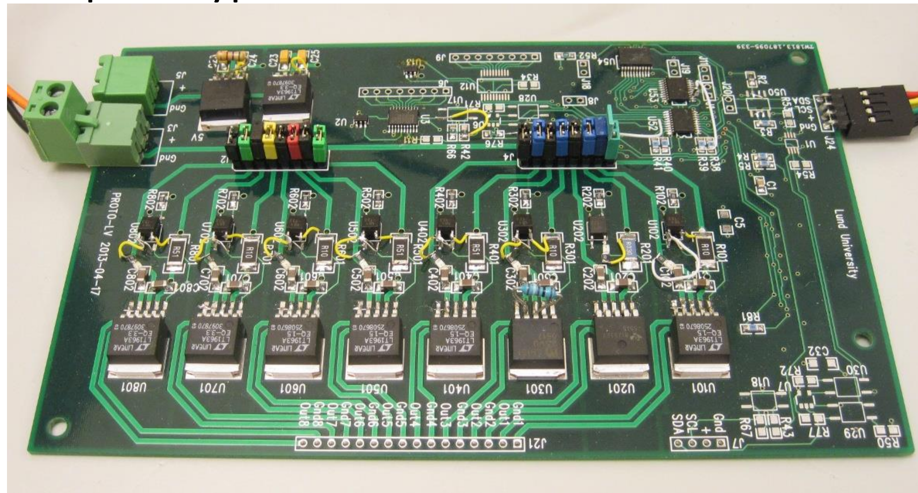


- Three MCM-development boards have been prepared (Lund, Brussels and Wuhan Univ.) and sent to Brussels for mounting of SALTRO-chips.
- The purpose is to develop firmware for communication between the SALTRO-chip and the CPLD (Yifan Yang), and the SRU (Fan Zang), respectively.
- SALTRO-chip in CQFP208 packaging.

- The first tests in Brussels were succesful
  - The firmware for the CPLD was installed and communication between SALTRO and CPLD was established.
  - Communication with the SRU could also be established
- Readout via ALICE DDL worked but data was corrupt due to the firmware, which has to be modified
- We have decided to use ethernet connection for readout and control

LV-prototype board and the final LV-board

LV-prototype board



10 cm

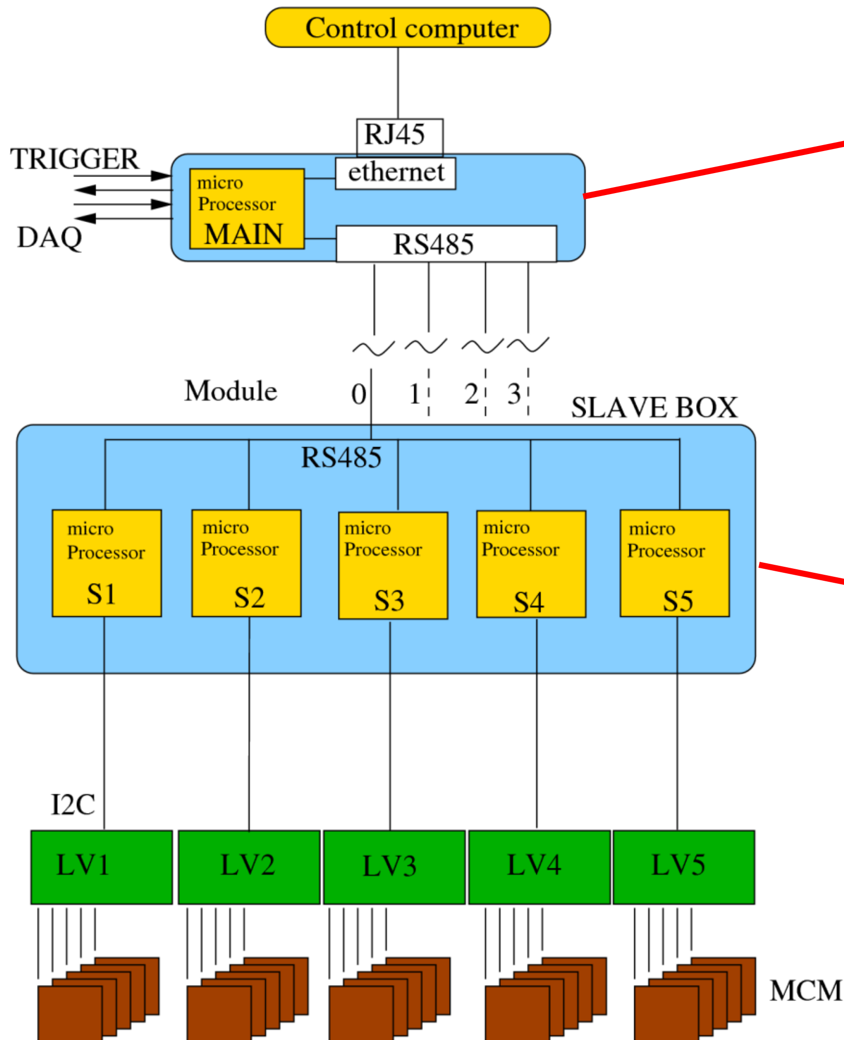
16 cm

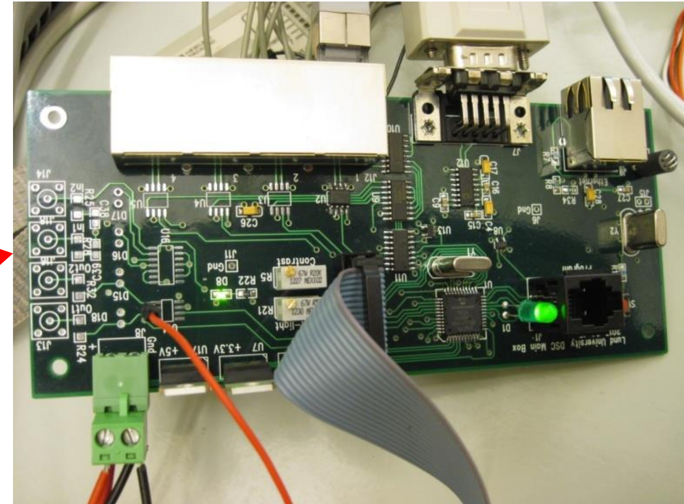
- The Low Voltage Prototype Board is used to test the concept of the final LV-board.
- It will also supply the test set-up with voltage and provide some configuration.
- The board is ready and has been succesfully tested together with the test set-up.

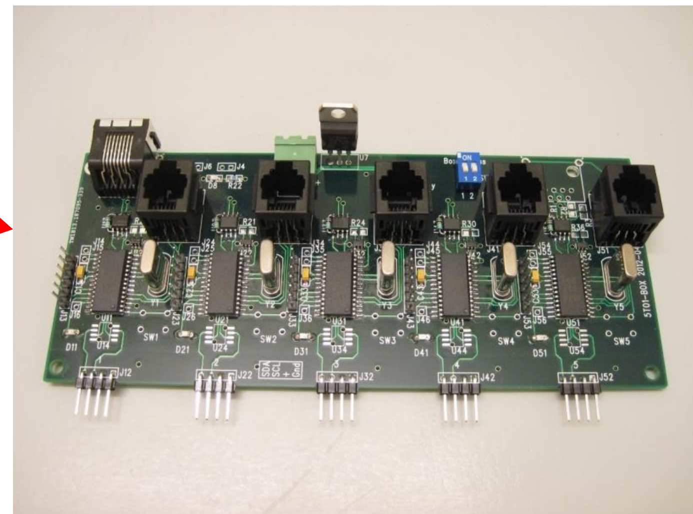
- For the final LV-board the concept is ready. We are waiting for the positioning of the cooling pipes and the final design of the mechanical support.

The Detector ControlSystem

~700 parameters from the LV- and MCM-boards has to be monitored per module
DOOCS will be used







- The two boards have been successfully tested
- Will be used for tests of SALTRO-chips mounted on Carrier Boards

Summary of the status and future work

- The test set-up for testing SALTRO-chip mounted on Carrier Boards is assembled.
- Three Carrier Boards with bonded chips have been produced although the application of the epoxy layer is still missing. When the top side is completely ready, tin balls are going to be applied on the bottom side.
- The functionality of the test set-up will be tested using an unmounted Carrier Board.
- The next step is to test the three mounted Carrier Boards to investigate the performance of the Carrier+SALTRO.
- If ok bonding of the remaining SALTRO-chip and testing. If not ok another iteration of the Carrier Board design.
- Production of a mock-up system with dummy Carrier-, MCM- and adaptor boards to verify the soldering procedure and check that the various parts fit together.
- The design of the final MCM-board will be completed and the PCB ordered.
- As soon as the mechanical support structure and the layout of the cooling pipes is fixed the design of the LV-board can be finished.
- Modification of the firmware for the CPLD and the SRU and further tests of the communication.
- Development of an Ethernet based DAQ-system and common DAQ integration.
- Tests of a complete readout chain.

Several activities going on in parallel

What have we learned so far ?

- The SALTRO-chip is not an ideal solution but required many cumbersome compromises in the PCB-design
  - -too many connectors to interconnect the various subsystems
  - -too many voltage levels $\rightarrow$ bulky voltage supply
  - -too many functions set external (gain, shaping time, decay time etc.)
  - -bulky cooling system

- Further, the new chip has to have a higher channel density

What can be done better in the future ?

Chip design:

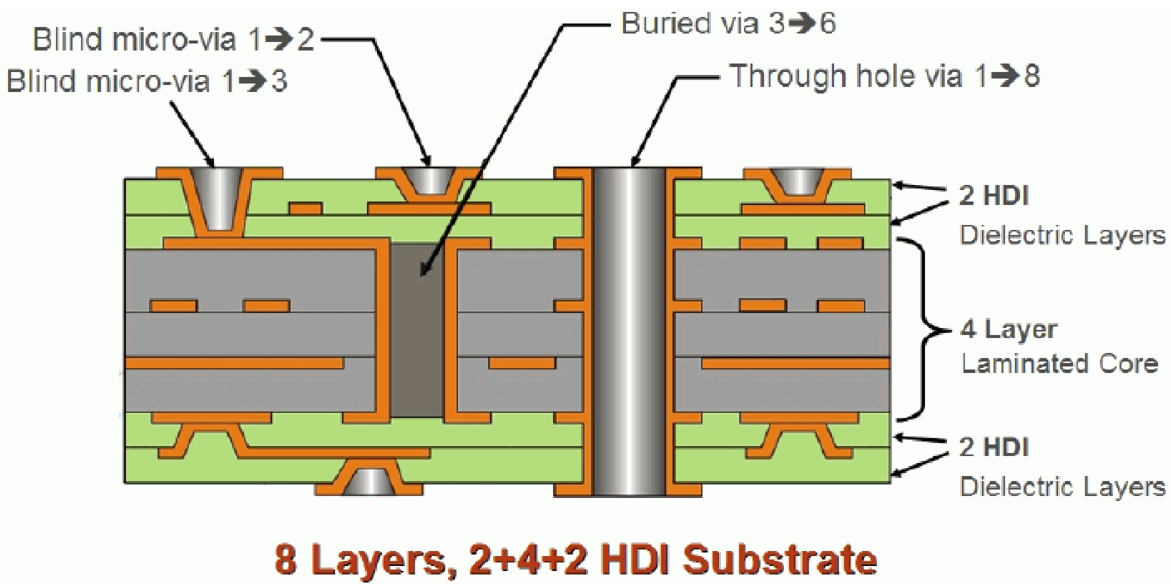
- the new chip should have ≥ 64 channels
- lower power consumption with fewer voltage levels
- integrate functions that are now provided externally
- should have a fast serial bus

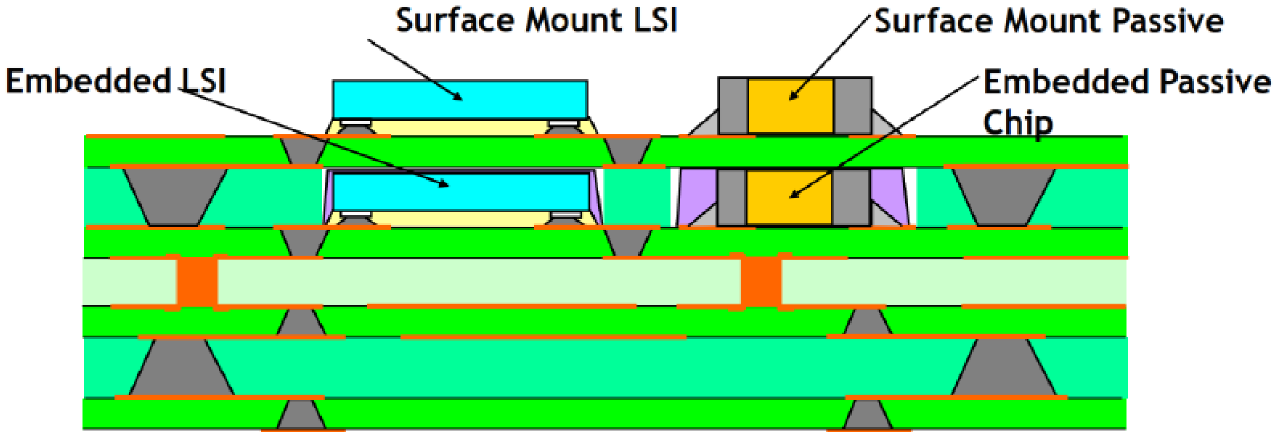
PCB design = Pad plane design:

- design pad plane in HDI technology (higher routing density both for signals and voltage supply).
- this technology offers the possibility to create cavities in the PCB where electronic och mechanical components can be mounted and thus embedded into the PCB so that essentially the full surface is available for surface mounting of chips.
- this technology may also offer a solutionto integrate cooling into the PCB (development project together with PCB manufacturer)
- chips mounted on small carrier board in 3D technology, where the carrier boards are bump bonded onto the pad plane

These two development projects should not proceed separately but there should be continous interaction to arrive at an optimal solution

The principle of HDI-design (High Density Interconnect)





Estimated fraction of work remaining: 40%
The project has significanlty expanded since the AIDA-application.

Fraction of AIDA money spent: 100%

Usage of DESY test beam infrastructure:

June 2011
Sept 2012
Dec 2012
March 2013
June 2013
Nov 2013