Chip Development Progress

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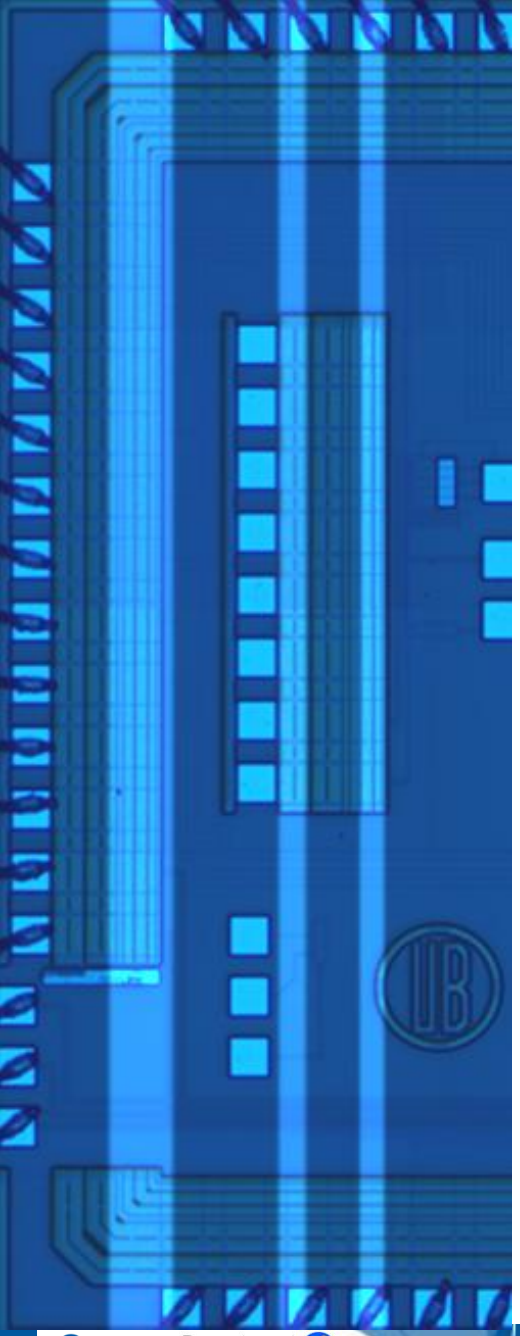


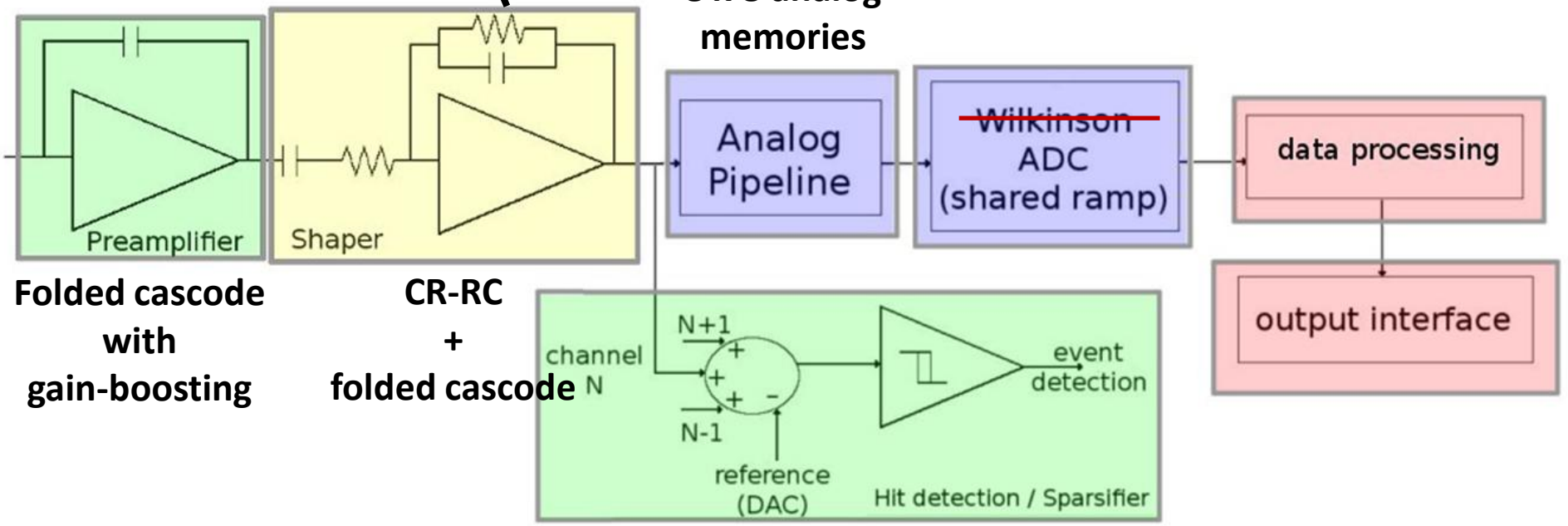
➢Outline

1. **Reminder of the general structure of the readout system**
2. **Shaper design**
   - MOSFET based solution
   - Noise comparison
3. **ADC design**
   - Problem of typical Wilkinson ADCs
   - Incremental data converters
   - Comparison

1. General structure of the readout circuit.

Different options for shaper resistor →

a) Polysilicon resistor (large area, discarded)
b) Active resistor (current mirror based, explored and finally discarded)
c) Single MOSFET (presented today)

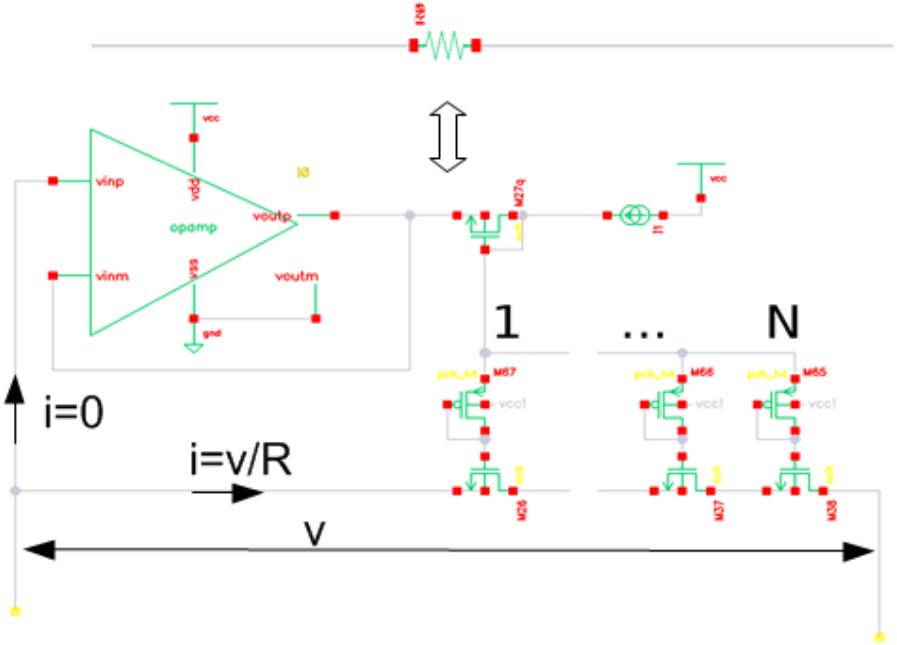


Folded cascode with gain-boosting

CR-RC + folded cascode

Addition circuit + comparator

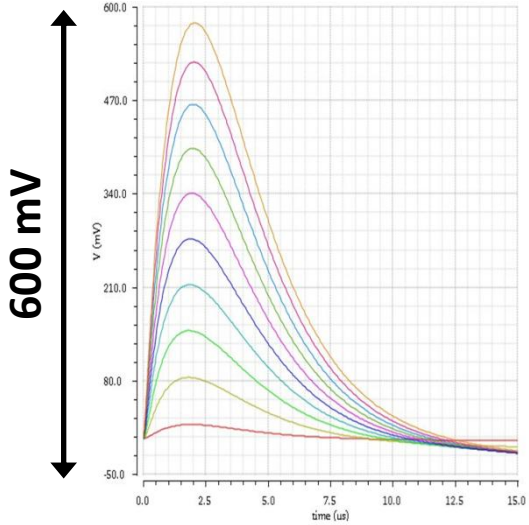
2. Shaper design. MOSFET based solution.



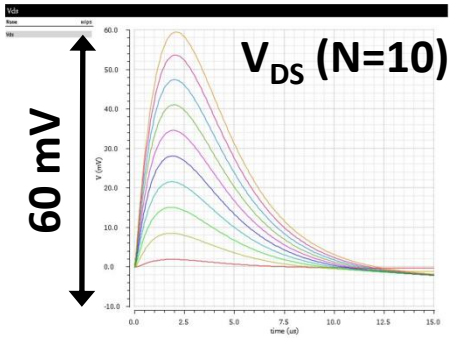
- V_{GATE} is referenced to V_{SOURCE} of the first transistor with a follower. Regulated with a programmable current.
- The voltage in the resistor is divided with N transistors.

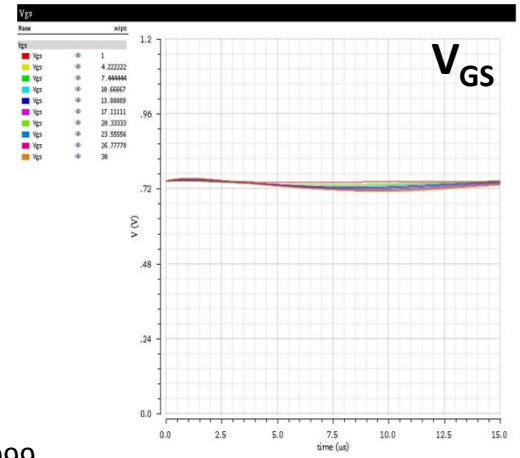
- ~ GΩ equivalent resistor.
- Quasi-floating gate transistor

- V_{GATE} ~ constant (gate is capacity-coupled to source)



- Very low V_{DS} variations due to multiple transistors in series (linearity ↑↑)





1) E. Özalevli, P.E. Hasler, IEEE Trans. Circuits Syst. 55 (2008) 999.
2) J. Ramírez-Angulo et al., Electron. Lett. 41 (2005) 511.

2. Shaper design. Noise comparison.

- **Noise comparison**:

$$ENC = A + B \cdot C_d$$

- A, B = noise parameters
- C_d = detector capacity

- **Simulation conditions**:
  - Dynamic range: 30 MIPs
  - Different sensor thickness
  - 2µs of peaking time

	sensor thickness	A	B	Noise at 20pF
Poly. resistors	300µm	260e-	4.9e-/pF	350e-
	200µm	188e-	4.5e-/pF	272e-
Current mirror based	300µm	180e-	7.7e-/pF	326e-
	200µm	228e-	7.7e-/pF	374e-
MOSFET based	300µm	148e-	6.3e-/pF	266e-
	200µm	129e-	5.5e-/pF	233.1e-

- **Comparison with other front-ends**:

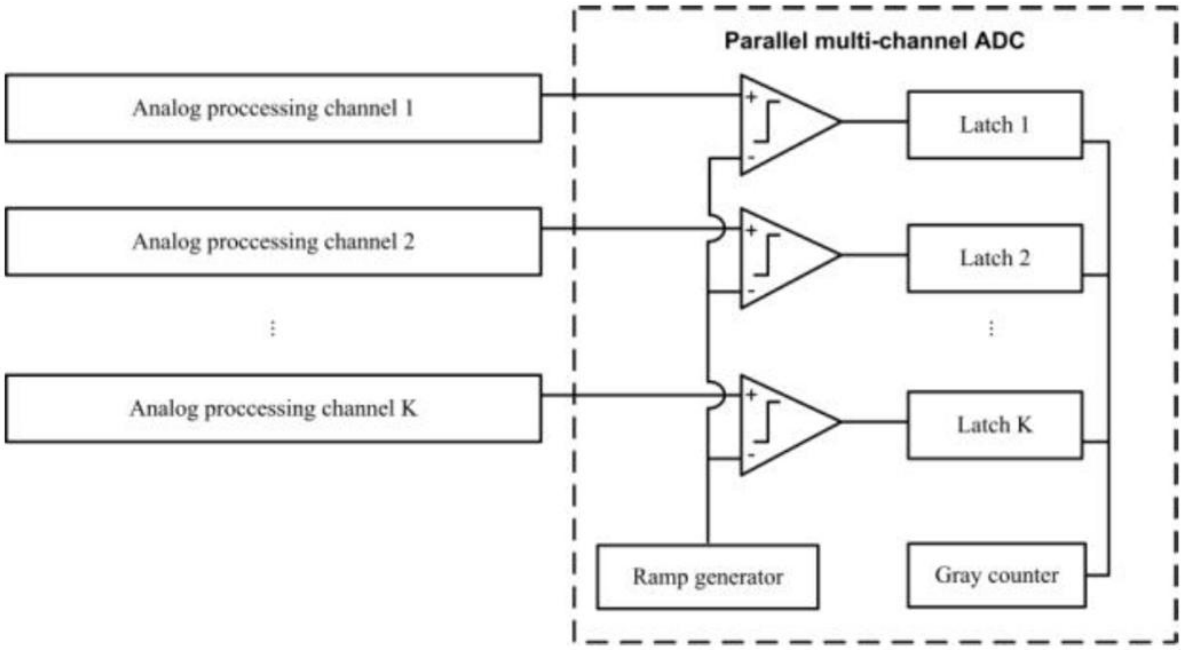
Front-end	A (e-)	B(e-/pF)	Shaping time
APV25	246	36	50 ns
MX6	340	20	
VA1	200	8	1µs
Beetle	303	33,6	25 ns
KPix	300	35	
This des., polysilicon	260	4.9	2µs
This des., current scaling	180	7,7	2µs
This des., quasi-floating gate	148	6,3	2µs

Simulated data →

3. ADC design. Problem of typical Wilkinson ADCs.

- **Preferred ADC option** → multi-channel parallel **Wilkinson ADC**.
- Problem → sensitive to parameter spread in nm technologies + limited speed **(time=2^{nbits} clock cycles)**.

Multi-channel parallel Wilkinson ADC

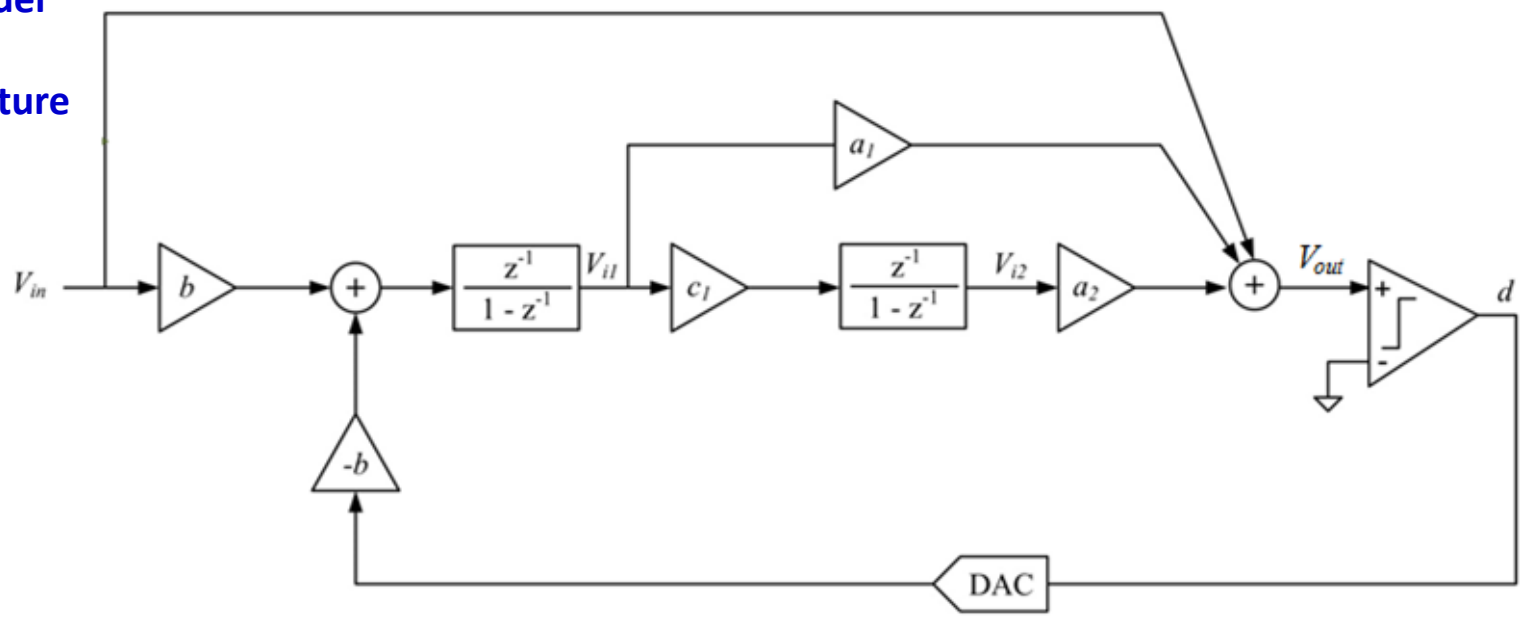


- **Proposed solution** → **Incremental data converter (IDC)**.
  - Sigma-delta converter with stop/reset (to fit ILC timeline).
  - **Insensitive to parameter spread**.
    - Highly digital circuits.
  - **Higher operating frequencies** (1 order of magnitude faster than Wilkinson ADCs).
    - Possibility to multiplex several channels per ADC + reduction of area.

3. ADC design. Incremental data converters.

- Possible architectures:
  - First order (1 integrator + 1 comparator) → long conversion times of 2^{nbits} clock cycles
  - **Second and higher orders by cascading integrators (Cascaded-Integrators Feed-Forward or CIFF)**

2nd order CIFF architecture

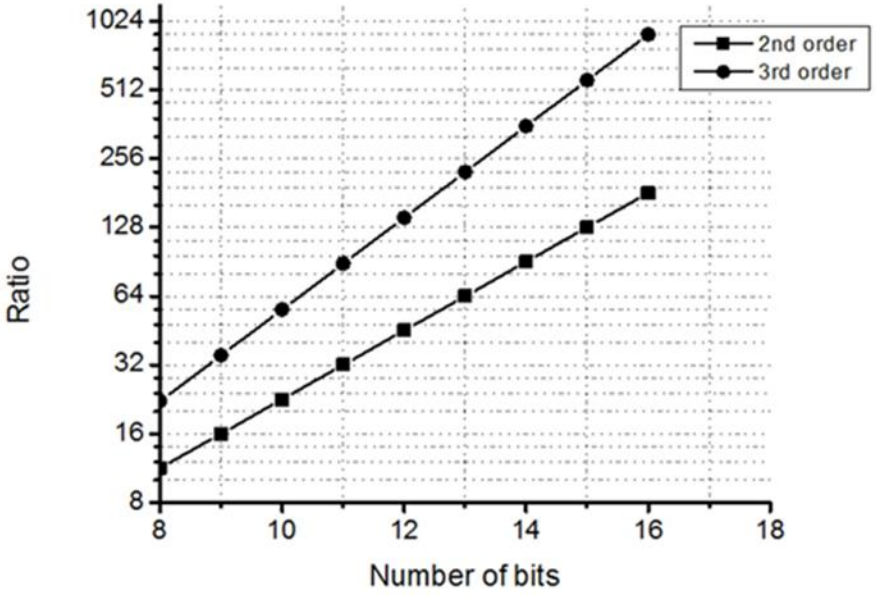


- Advantages of CIFF architectures:
  - **Short conversion times → $\sqrt{\frac{2^{nbits+1}}{c_1 \cdot b}}$ clock cycles (2nd order), $\sqrt[3]{\frac{3 \cdot 2^{nbits+1}}{c_2 . c_1 \cdot b}}$ clock cycles (3rd order)**
  - Less sensitive to non-linearities.
  - Less voltage swing.
  - 1 DAC only (less matching problems).

3. ADC design. Comparison.

- **Number of clock cycles or n** (assuming b, c_1 and c_2 = 1):

nbits	n		
	Wilkinson	*second order*	*third order*
8	256	23	12
9	512	32	15
10	1024	45	19
11	2048	64	23
12	4096	91	29
13	8192	128	37
14	16384	181	47



- **Inputs**:
  - 256 channels
  - 8 hits per strip (expected)
  - 8 samples to reconstruct each hit
  - 12 bits of resolution (n bits)
  - 40 MHz of clock frequency

$$8\ \frac{\text{hits}}{\text{stripe}} \cdot 8\ \frac{\text{samples}}{\text{hit}} \cdot \text{n} \cdot \frac{1}{\text{clock frequency}} =$$

Results per channel:

6.5 ms (256 channels parallel Wilkinson ADC)

0.14 ms (2nd order IDC) → 45 times faster! (area ↓)

0.046 ms (3rd order IDC) → 141 times faster! (area ↓↓)

3. ADC design. Comparison.

- **Number of clock cycles or n** (exact value of b, c_1, c_2, a_1 and a_2?):

order	b	c_1	c_2	a_1	a_2	n
2	0.7	0.6	-	1.107	0.515	139
3	0.35	0.5	0.65			60

- The coefficients must be set below 1 to avoid the saturation of the integrators
- Coefficients simulated with Matlab (Sigma Delta Toolbox)

$$8\,\frac{\text{hits}}{\text{stripe}} \cdot 8\,\frac{\text{samples}}{\text{hit}} \cdot n \cdot \frac{1}{\text{clock frequency}} =$$

Results:

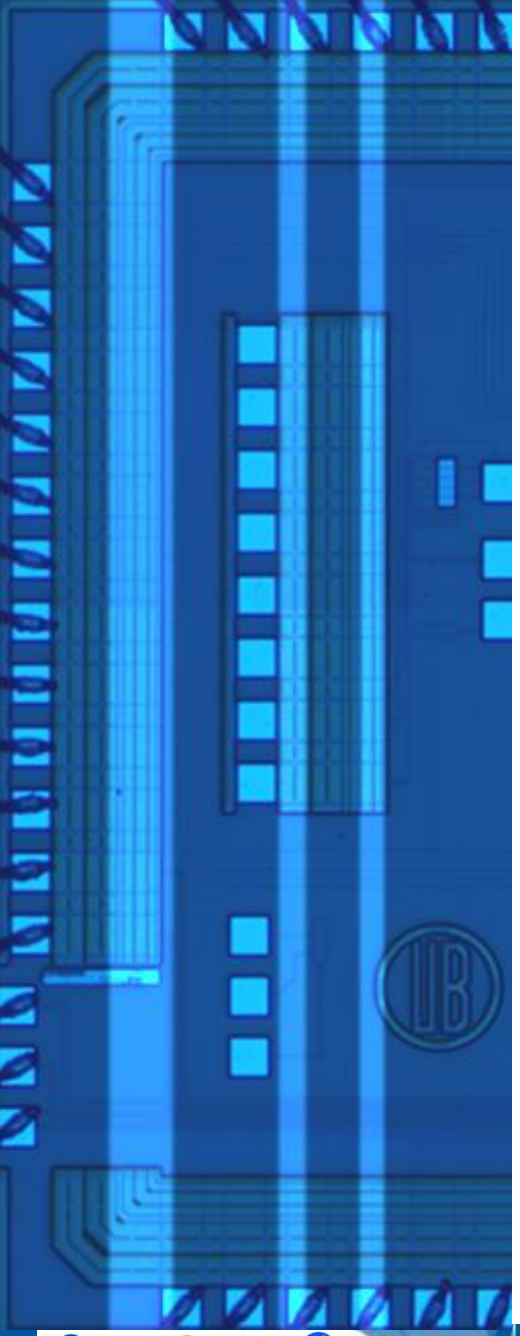
6.5 ms (256 channels parallel Wilkinson ADC)

0.22 ms (2nd order IDC) → 0.056 s per 256 channels

0.096 ms (3rd order IDC) → 0.024 s per 256 channels

- IDCs offer higher conversion rates than Wilkinson ADCs (at the same clock frequency)
- **In IDCs, it is possible to multiplex several channels per ADC (area ↓, same conversion time):**

- 256 channels parallel Wilkinson ADC
- 2nd order IDC → 9 IDCs (9 ADCs) for a conversion time of ≈ 6.5 ms (28 channels per ADC)
- 3rd order IDC → 4 IDCs (4 ADCs) for a conversion time of ≈ 6.5 ms (64 channels per ADC)



Thank you for your attention