Task 9.5: Granular Calorimeter Studies Infrastructure

Applications in the CALICE AHCAL and ScECAL

- HCAL Base Unit (HBU)
- Power Pulsing
- New Tiles
- Data Acquisition System (DAQ)

AIDA

Aliakbar Ebrahimi - DESY
AIDA 3rd Annual Meeting 2013
Vienna, Mar 26-28 2014

HELMHOLTZ ASSOCIATION

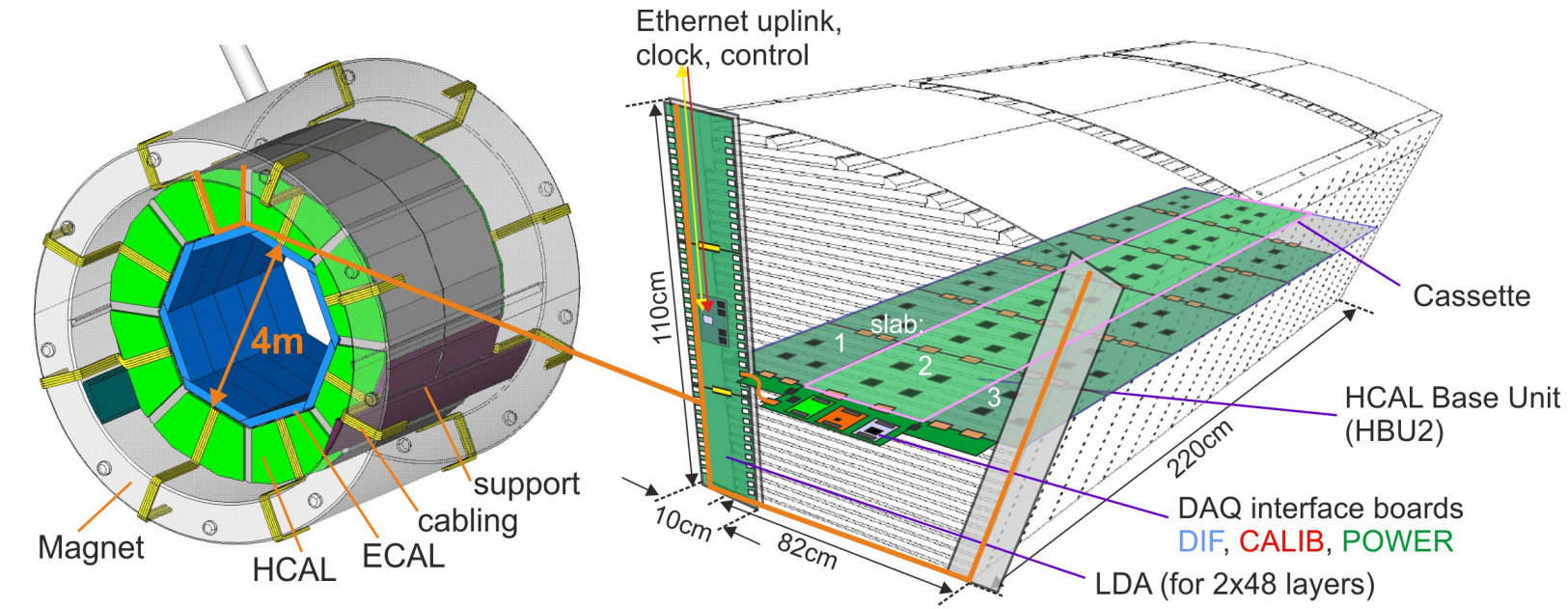
THE PICOSEC MC-NET PROJECT

Universität Hamburg

CALICE Calorimeter for ILC

CALICE Analog Hadron CALorimeter (AHCAL)

- A highly granular hadron calorimeter for ILD
  - Iron or Tungsten absorbers
  - 3x3cm^2 plastic scintillator tiles
  - Readout by individual Silicon PhotoMultipliers (SiPM)
  - 8 millions channels, 50k PCB → Readout fully integrated into the layers



Who is involved?

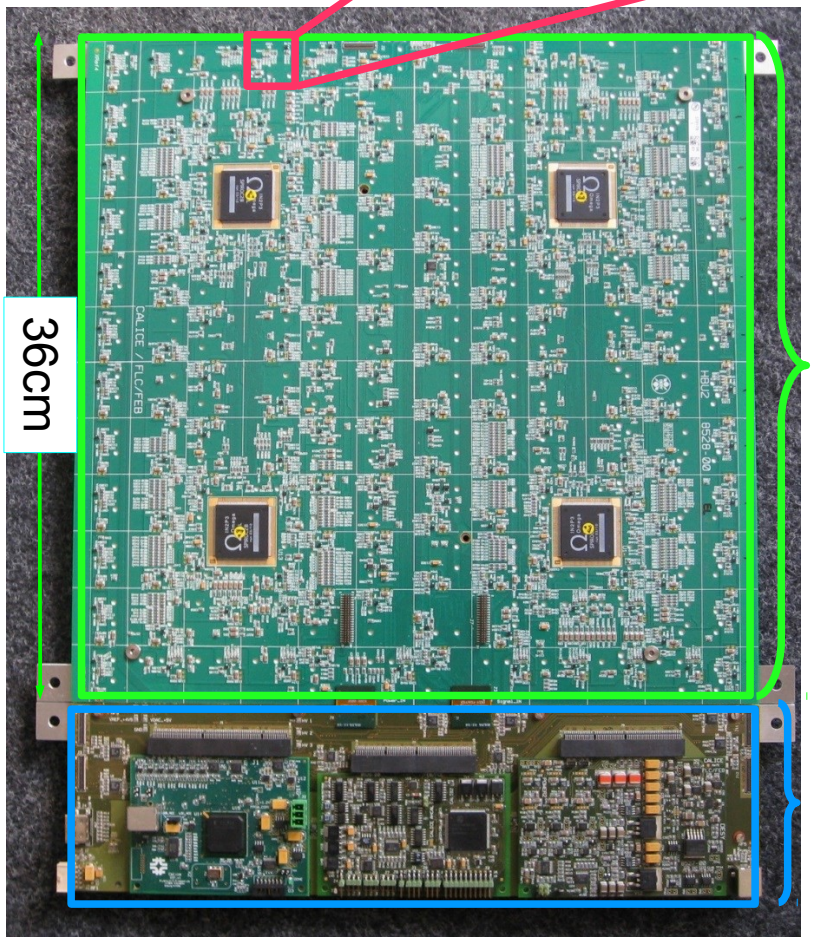
- DESY: steel structures, electronics and integration, test beam support, software, project management
- Heidelberg: high gain ASICs, SiPM mass tests and characterisation
- MPI Munich: SiPM development, tile optimisation, cassettes, tungsten timing
- Wuppertal: embedded LED electronics and test stands
- Mainz: Data Acquisition System
- Omega: SPIROC ASICs
- CERN: tungsten absorber, testbeam and Geant4 support
- Prague: fibre based calibration system
- Bergen: calibration studies

- Hamburg: SiPM & tile optimisation, test beam and commissioning w/ DESY
- ITEP: tiles and SiPMs, test bench characterisation
- Dubna: power supplies and distribution
- NIU: alternative SiPM coupling, DAQ interface
- Matsumoto: scintillator strip alternative, photosensors

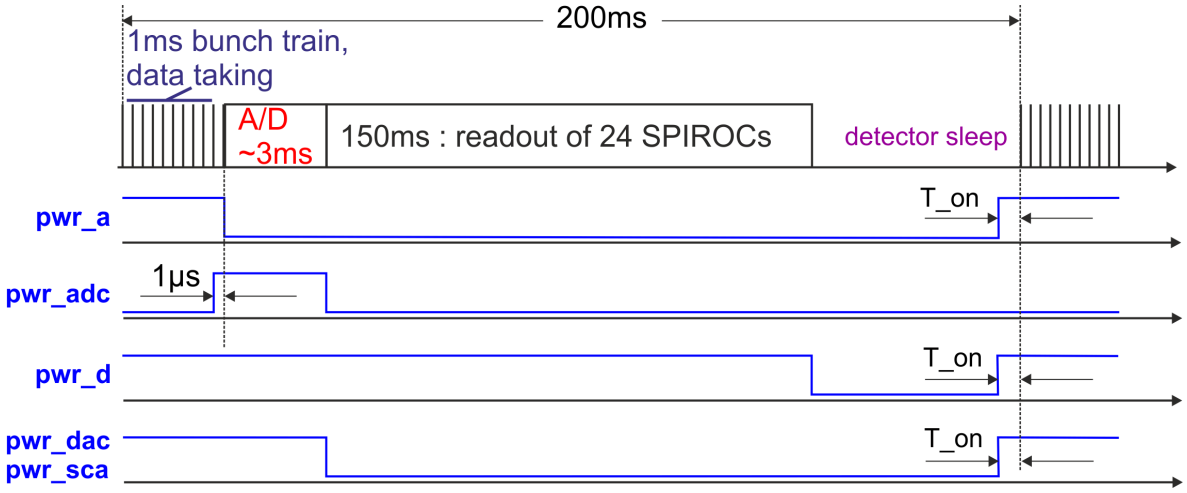
DESY

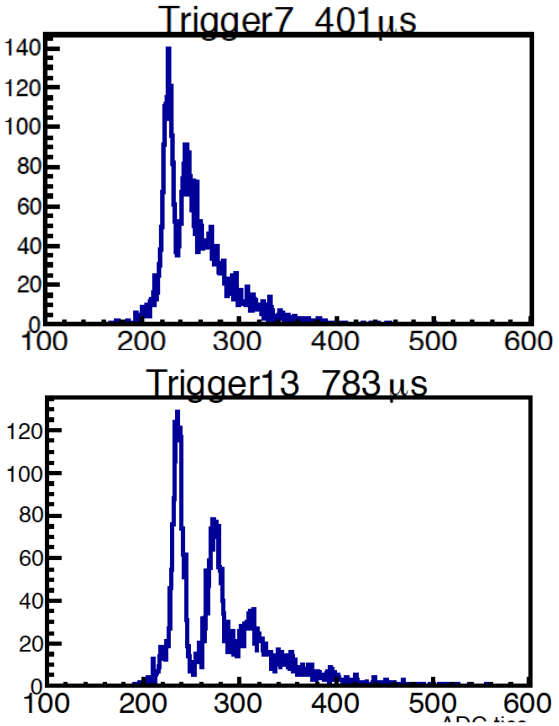
HCAL Base Unit (HBU)

- 144 detector channels
- 4 SPIROC2b ASICs
  - Designed by OMEGA (France)
  - 36 channels per ASIC
  - 12 bit ADC and TDC
  - Auto trigger
  - Power pulsing (25 μW/channel)
- Integrated SiPM calibration system
  - 1 LED per channel
- Each layer (18 HBUs) has a Central Interface Board (CIB)
  - DAQ interface, Calibration board, Power board
- 8 HBUs in use, more to be equipped with tiles by the end of the year



Power Pulsing

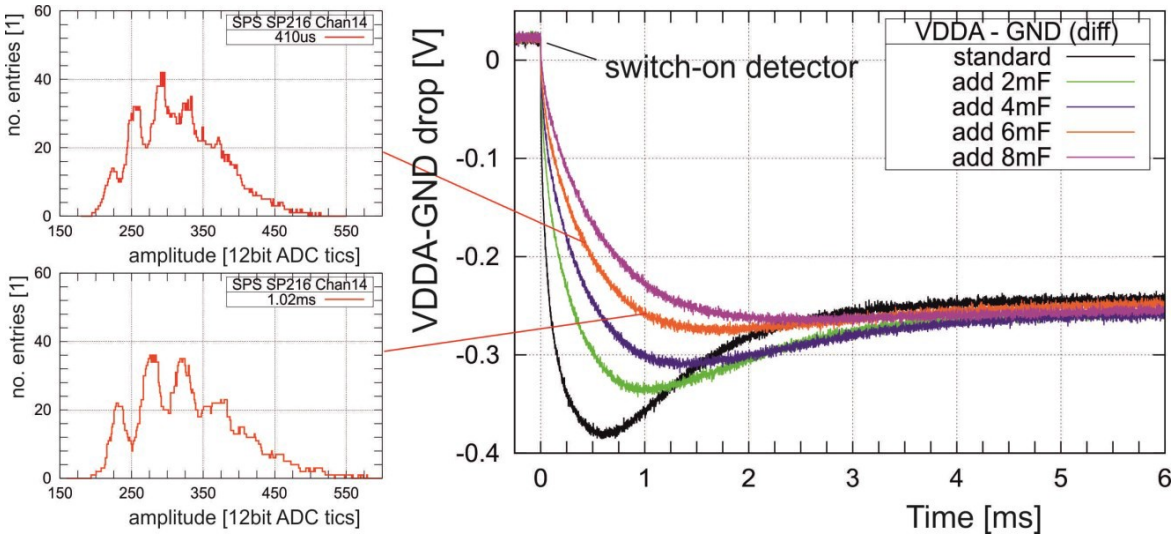


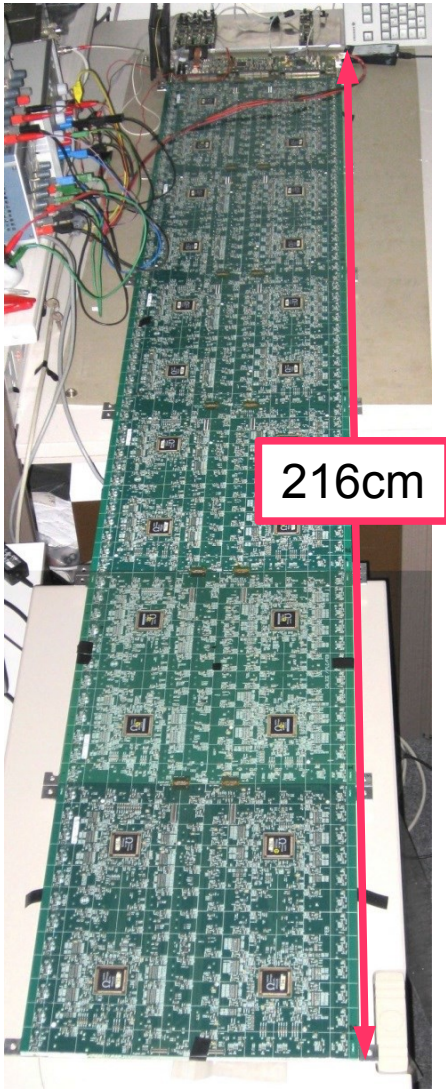


- No active cooling inside absorber gaps
- Switch off the detector between bunch trains
- How long T_on should be to save maximum power without limiting detector performance?
- HBU Power pulsing tested successfully using LED calibration system
- T_on time is longer than ASIC design expectation
- Too short Switch-on time → Low gain and high noise

Power Pulsing: Full Extension Test

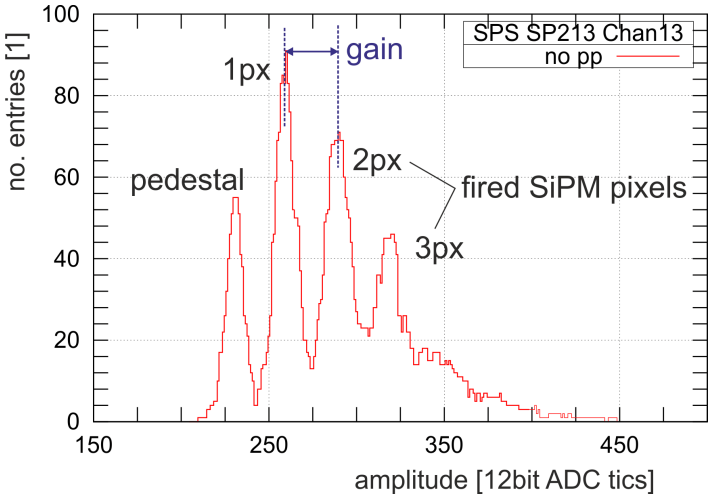
- Power pulsing tested in a full slab
  - 6 HBU2s with 864 channels
- Switched current: 2.75A (Analog supply voltage VDDA)
- Voltage drop across 216cm (dominated by flexeads)
  - 0.18V on VDDA and 0.04V on GND
- Additional block capacitors are needed
- Tradeoff between switch-on time and capacitors

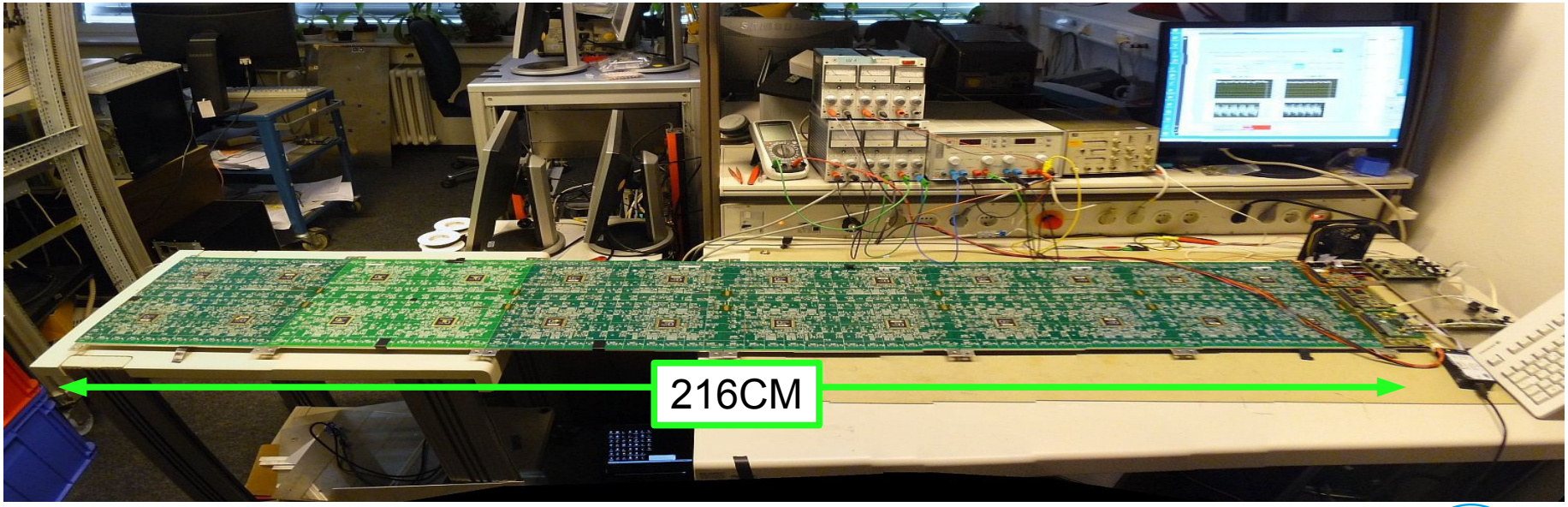




Full Extension Slab: 6xHBU in a row

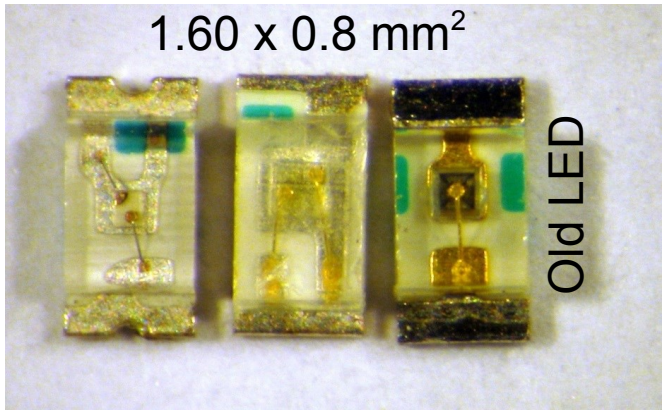
- Signal transportation over 216 cm is challenging
  - Power, 40 MHz LVDS clock, LED trigger
- Single-Pixel Spectra measured on the last HBU
- First results prove suitability of the solution

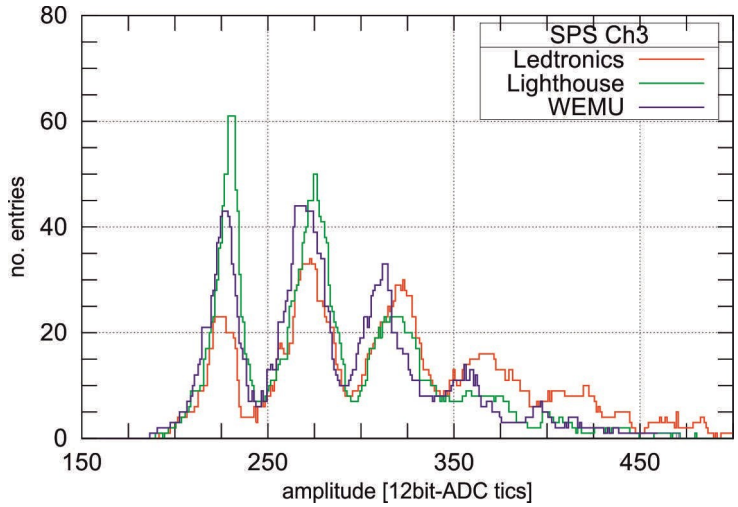




HBU Redesign

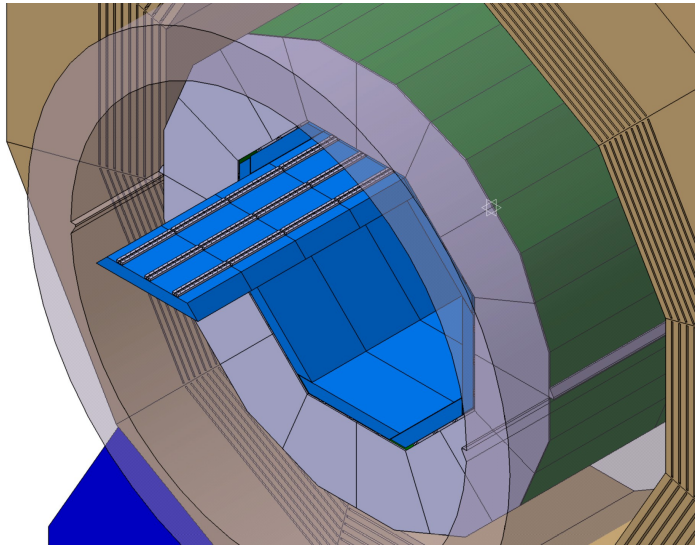
- UV LEDs used for calibration are obsolete
- Two new LED types are investigated
- New LEDs have narrow pad
- Integration required redesign of the HBU
- LED driver circuit is modified to improve chanel-to-chanel uniformity
- HBU redesign is completed:
  - 2mF additional block capacitors
  - Termination of the SiPMs and SPIROC bias reference to VDDA
  - VDDA/GND next to flex connectors
  - LED trigger: line length equalization
- Ready to order HBU3 board



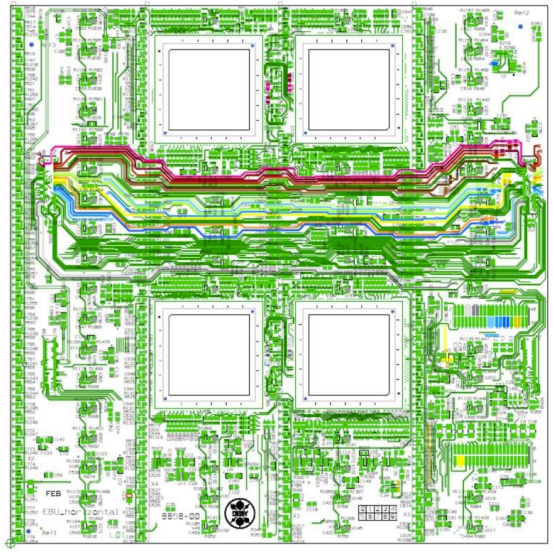


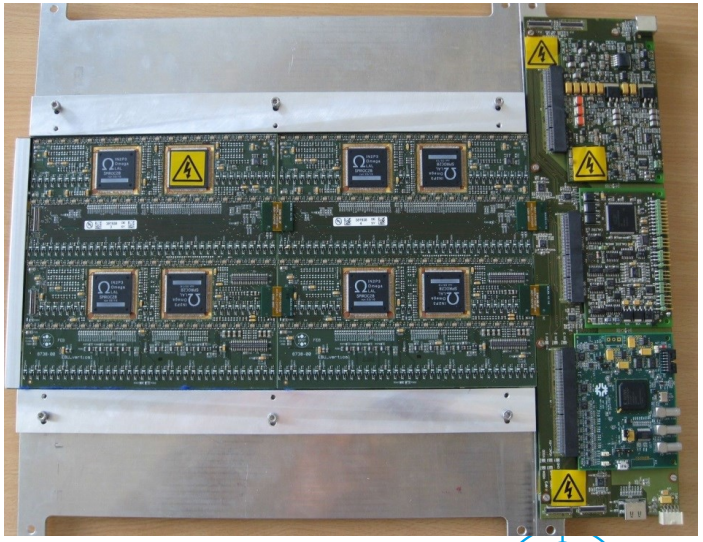
ScECAL Base Unit (EBU)

- In collaboration with Universities of Shinshu, Kyushu and Tokyo
- ScECAL uses scintillator strips
- HBU Architecture, scintillator strip
- Two different PCB designs needed
- One orientation is produced and in use
- Second orientation produced and tested



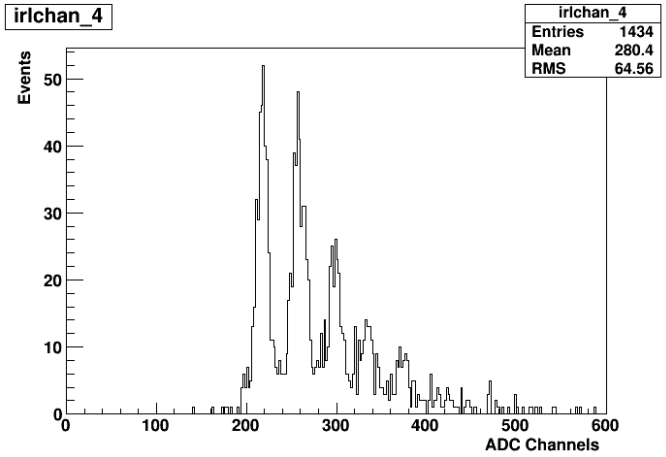
Horizontal EBU Layout

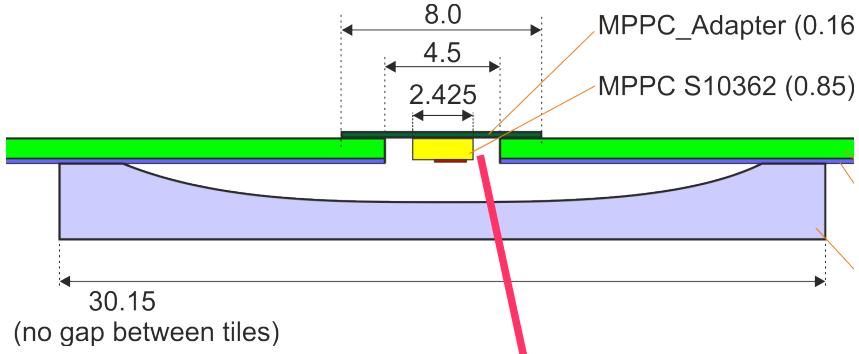


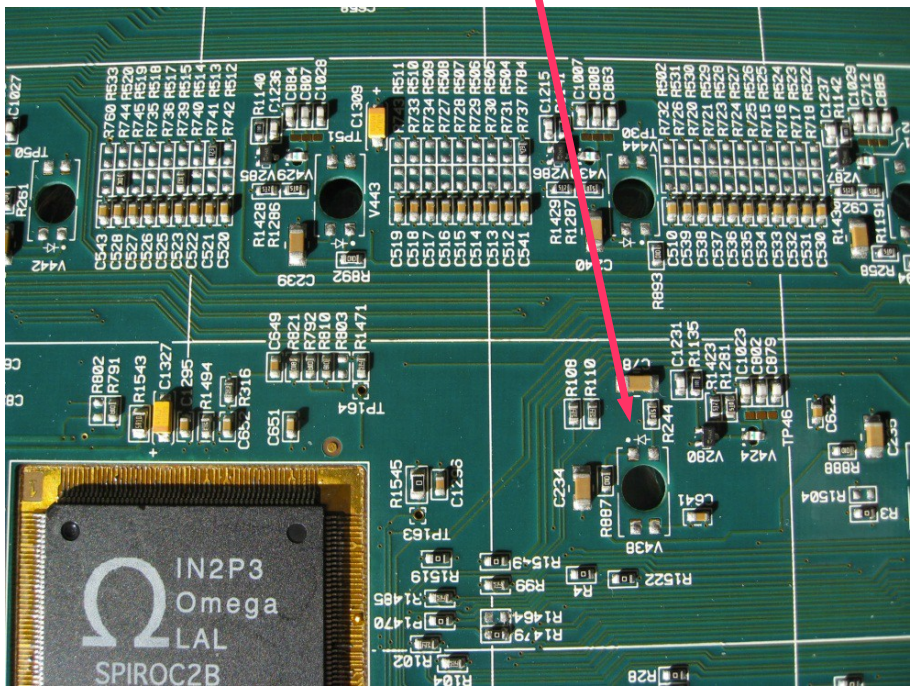


Surface Mounted HBU (SM_HBU)

- Collaboration with Northern Illinois University
- Tiles with concave cavity to improve uniformity
- One “megatile” per HBU
- SiPM is mounted on the PCB
- Two SM_HBU are produced
- Tested successfully at NIU

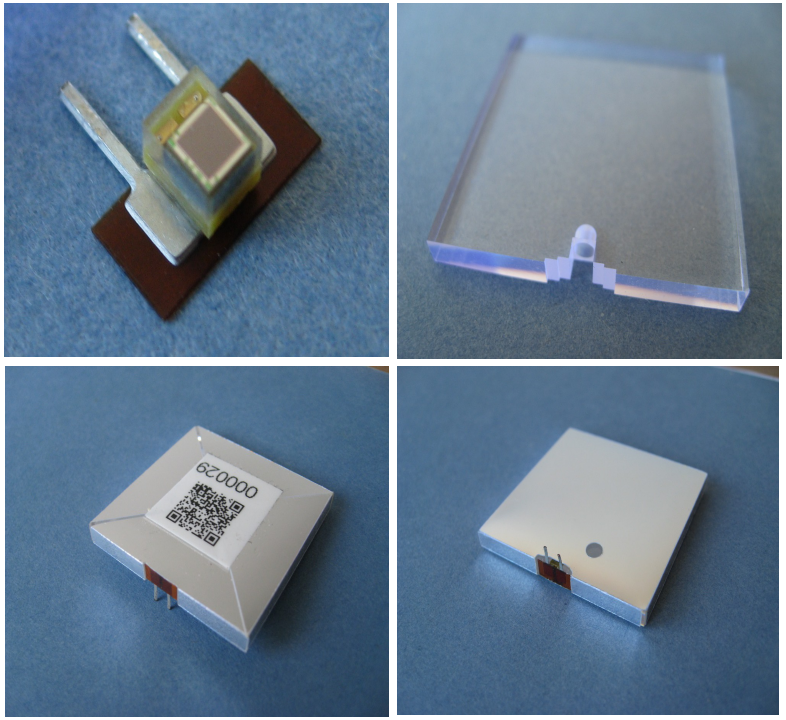


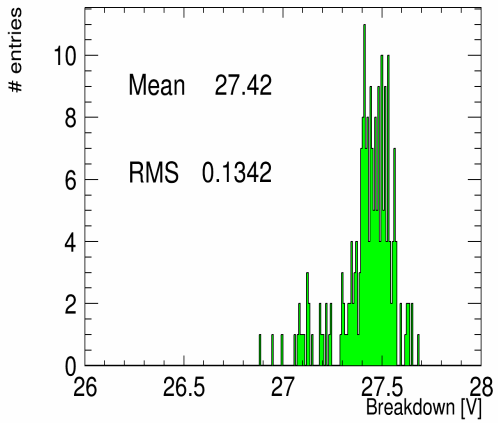


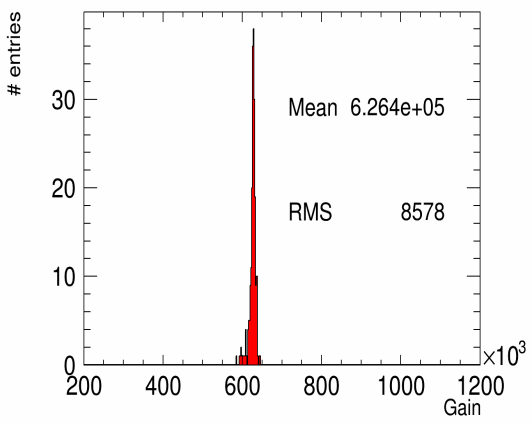


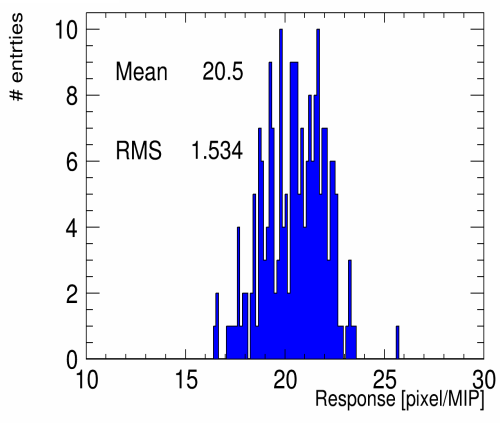
University of Hamburg Tiles

- Machined tiles
- Without wavelength shifting fiber
- Individually wrapped in reflector foil
- KETEK PM125 SiPM
- Reduced spread of operating voltage
- Four HBUs fully equipped and tested
- Performance at fixed excess bias (+2.5V):
  - Break-down min-to-max: 0.8V
  - Gain spread: 1.4%
  - Response spread: 7.5%



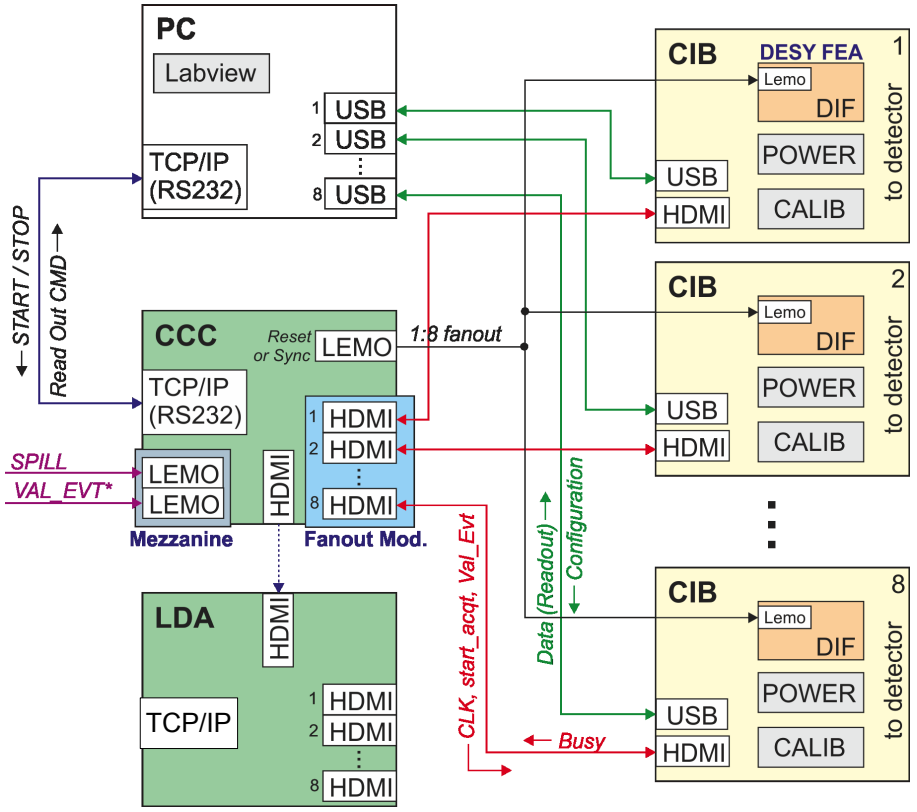






Current Data Acquisition System

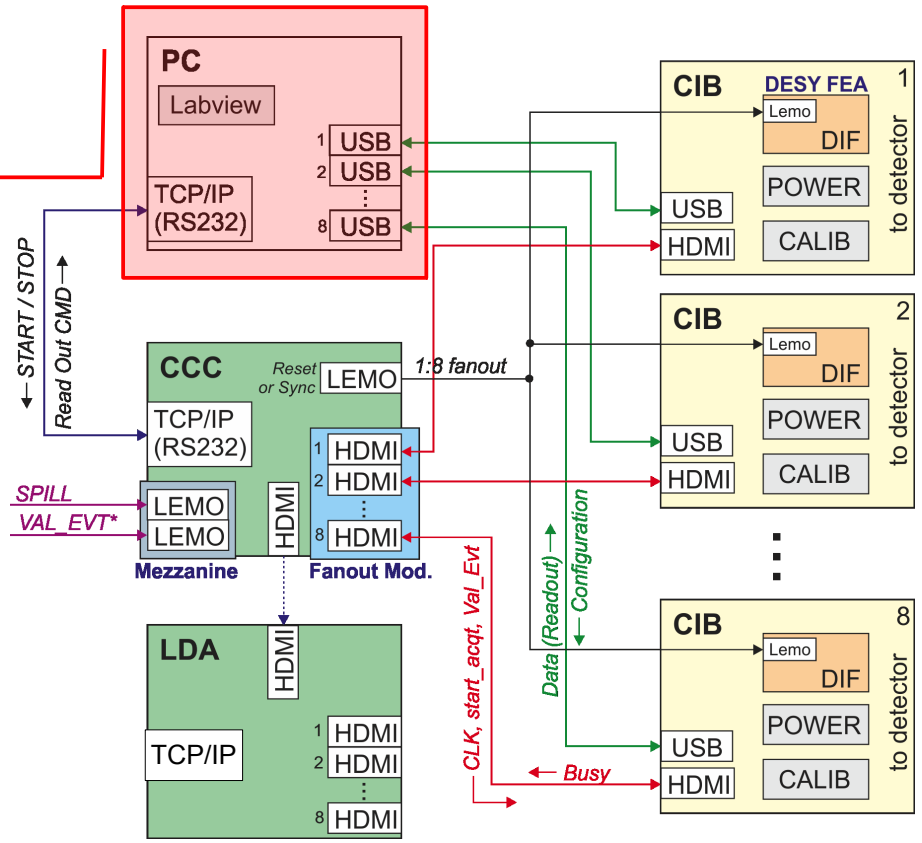
- The original DAQ could operate only one layer
- New multilayer DAQ based on the original CALICE DAQ concept
- Built on the single layer DAQ
  - Software improvement
  - Multiple-DIF configuration
  - Global clock and control
  - Data aggregator
  - Parallel readout
  - Scalable
- Currently there are 2 connections to DAQ interfaces (DIF):
  - HDMI for fast signals
  - USB for slow signals and data



AHCAL DAQ Block Diagram

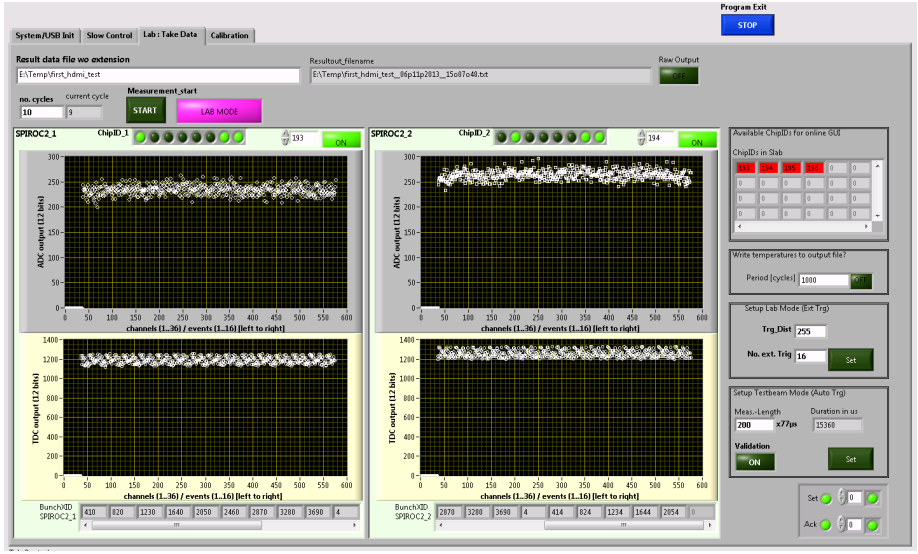
Main Subsystems of the DAQ

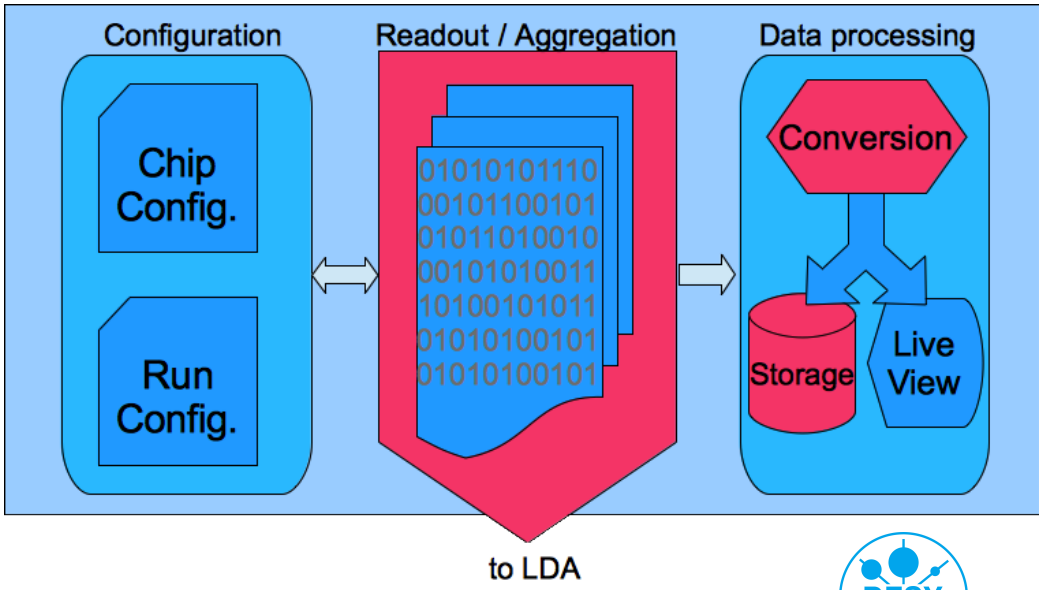
- DAQ Software
- Clock and Control Card (CCC)
- Link and Data Aggregator (LDA)



AHCAL DAQ Software

- Based on LabView
  - Easy modification
  - Live monitoring
- Modular and Multithreaded
- Some tasks done by C++ lib
  - Decoding
  - Storage
- Readout data aggregation to be moved to LDA
- Intensively tested and used during several testbeam campaigns





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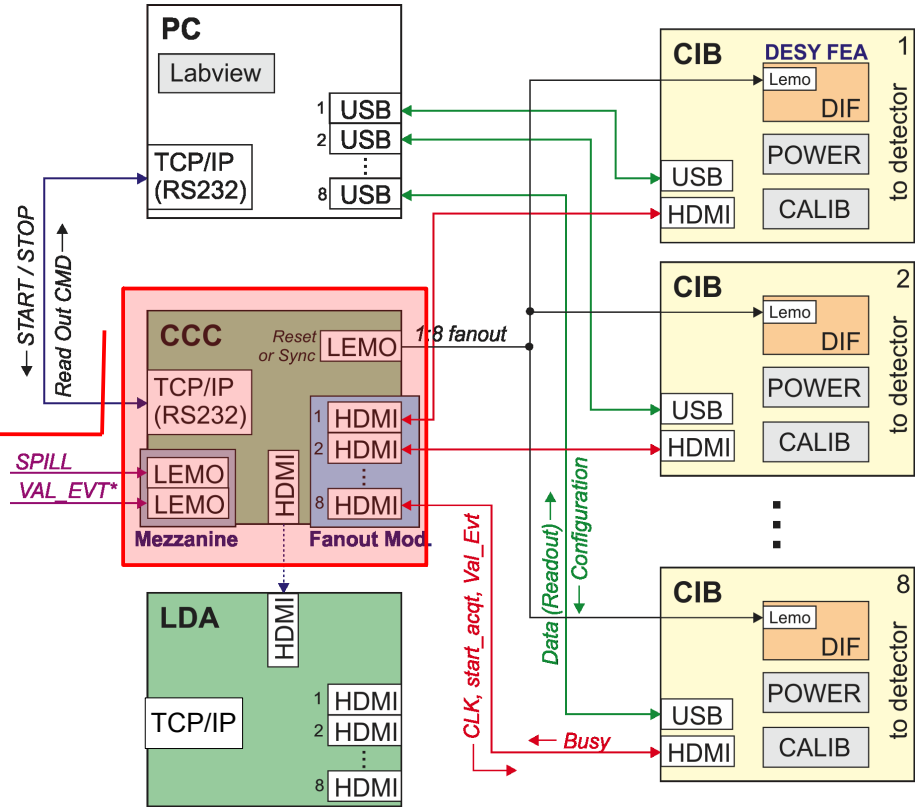
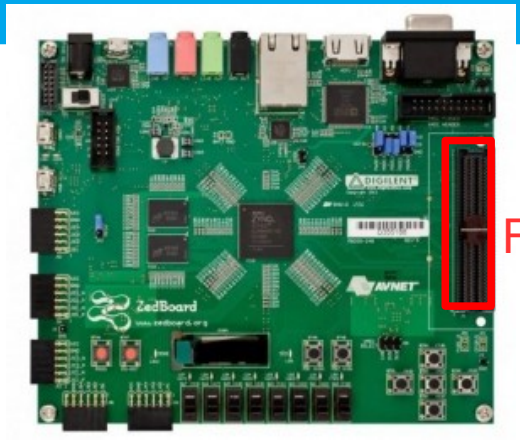
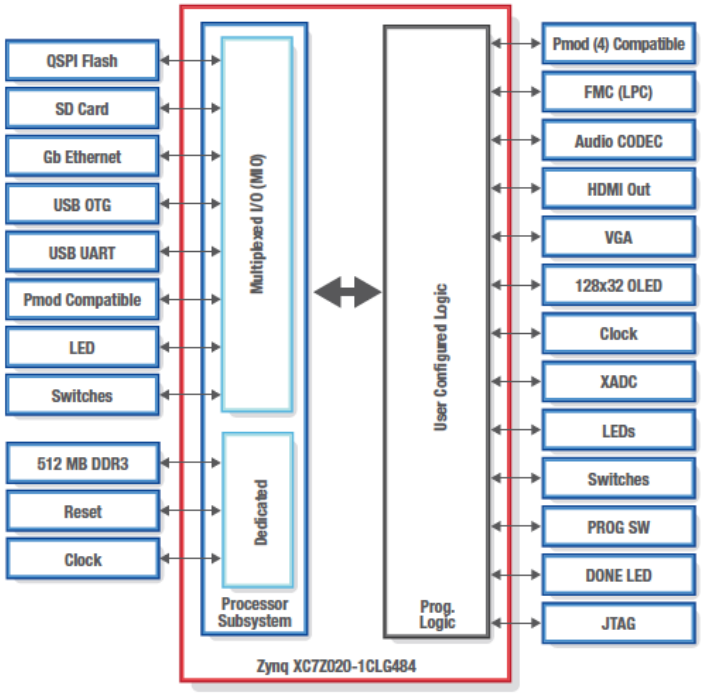


ZedBoard

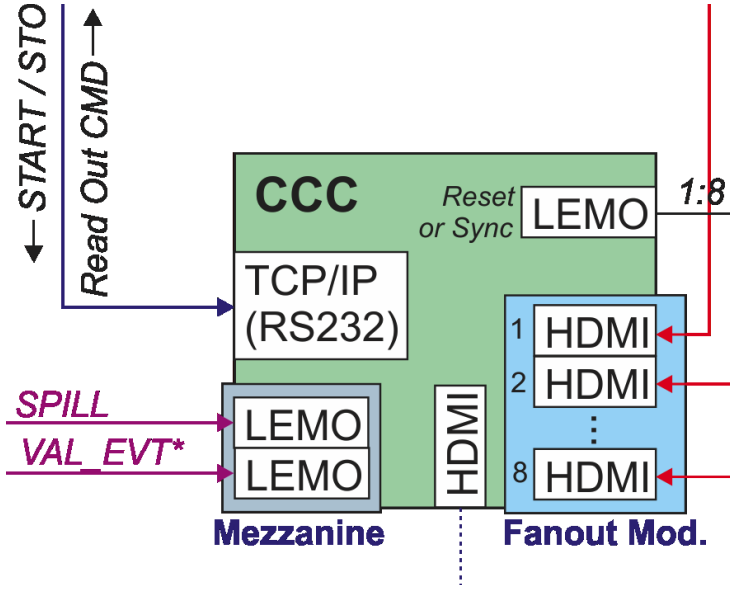
- Zynq Evaluation & Development Board
- Xilinx Zynq-7000 SoC
  - Processor Subsyst. (PS): Dual ARM Cortex-A9
  - Programmable Logic (PL): Xilinx 7 series FPGA
  - 100Gbps interconnect bandwidth
  - ARM programmability+FPGA flexibility
- On board memory
  - 512 MB DDR3 + 256 MB QUAD-SPI
- PS is able to run Linux
- FPG Mezzanine Connector (FMC)
  - Allows adding custom boards

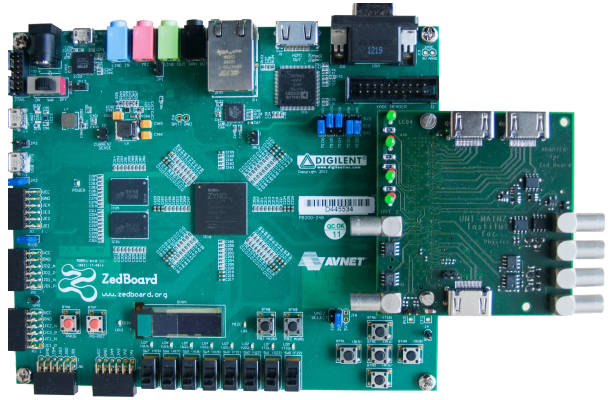




Clock and Control Card (CCC)

- New CCC design by university of Mainz
  - Compatible with CALICE DAQ
- Based on the ZedBoard
- Mezzanine board designed at Mainz uni.
- Ethernet connection to DAQ PC
  - Start / Stop / Readout
- In temp. setup while LDA is being developed
  - 8 layers are served using an 1:8 HDMI fanout
- LEMO connections for
  - Trigger/Validation signal
  - Spill signal
  - Reset / Sync signal
- Tested successfully and is in operation

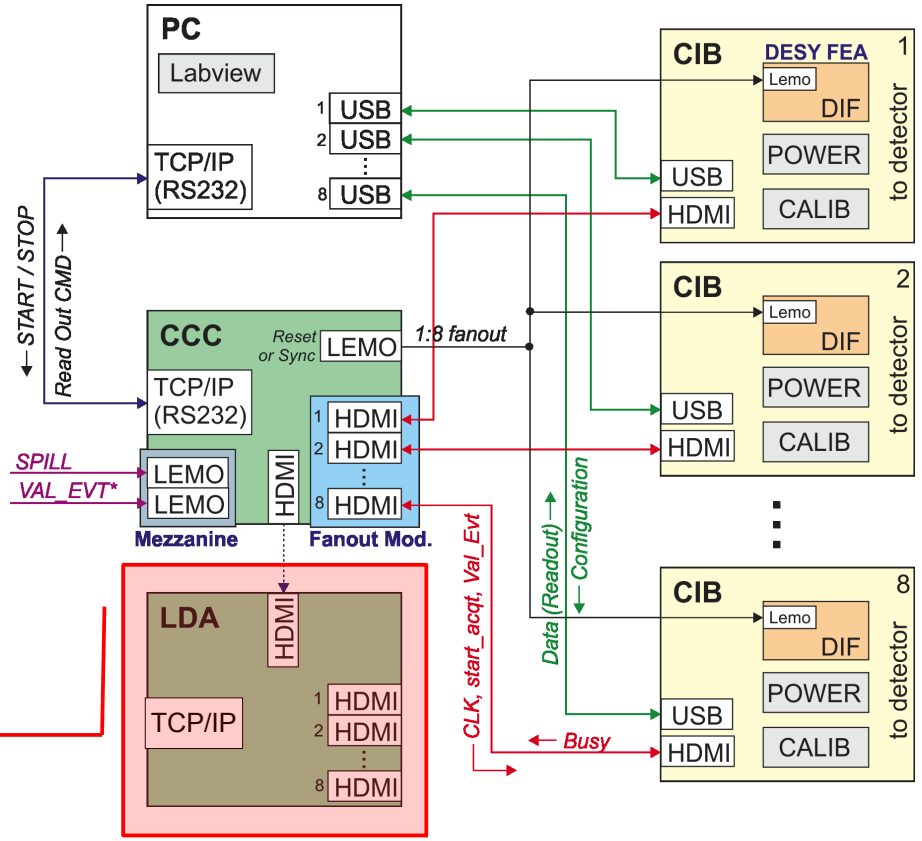




ZedBoard and Mezzanine

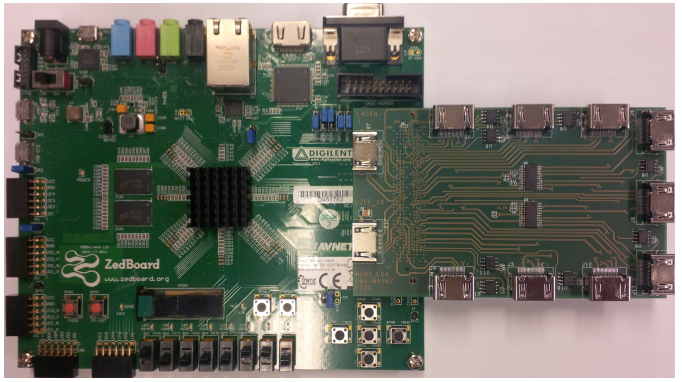
Main Subsystems of the DAQ

- DAQ Software
- Clock and Control Card (CCC)
- Link and Data Aggregator (LDA)

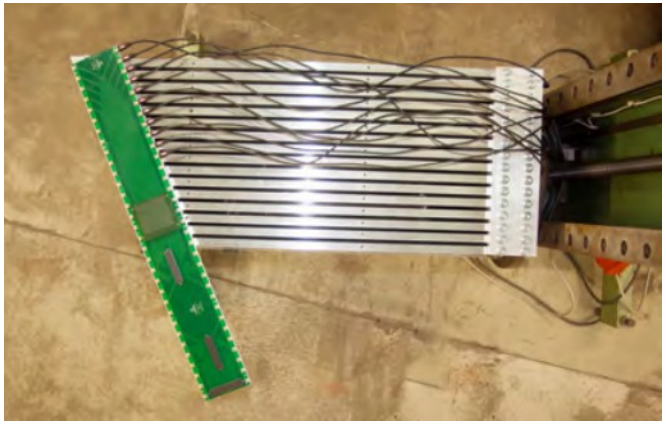


Link and Data Aggregator (LDA)

- New LDA design by university of Mainz
  - Compatible with CALICE DAQ
- Based on the ZedBoard
- Mezzanine board designed at Mainz uni.
- There are two options
  - Mini-LDA: ZedBoard + Mezzanine → Generic
  - Wing LDA → AHCAL geometry specific
- Mini-LDA hardware is ready
  - 1 HDMI connection to the CCC
  - 10 HDMI connections to the the DIFs
- Used as fanout in January testbeam



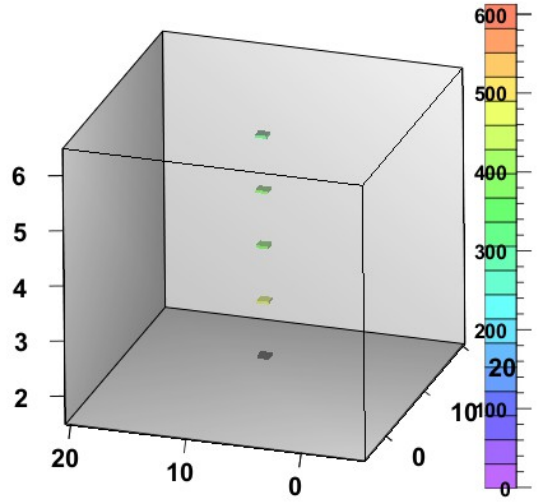
Mini-LDA and Mezzanine



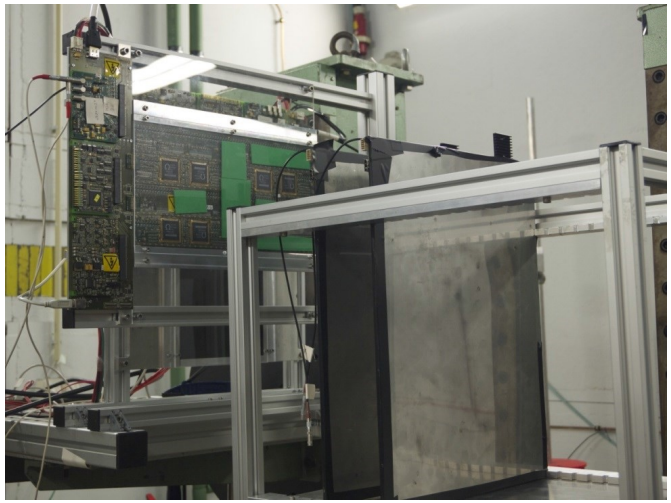
Wing LDA and the Absorber Stack

Performance of the DAQ system

- Current version of the DAQ tested in different setups
  - Lab Setup, Cosmic Muon run, Test beams
- Fully synchronous operation of 8 layers
- Very stable operation
  - 72+ hours cosmic Muon run
- Faster than ever
  - ~9Hz readout frequency
  - ~150Hz sustained trigger rate
- Successfully tested in a two detector setup
  - 2xHBU + 2xEBU
- It could be used to operate other calorimeters

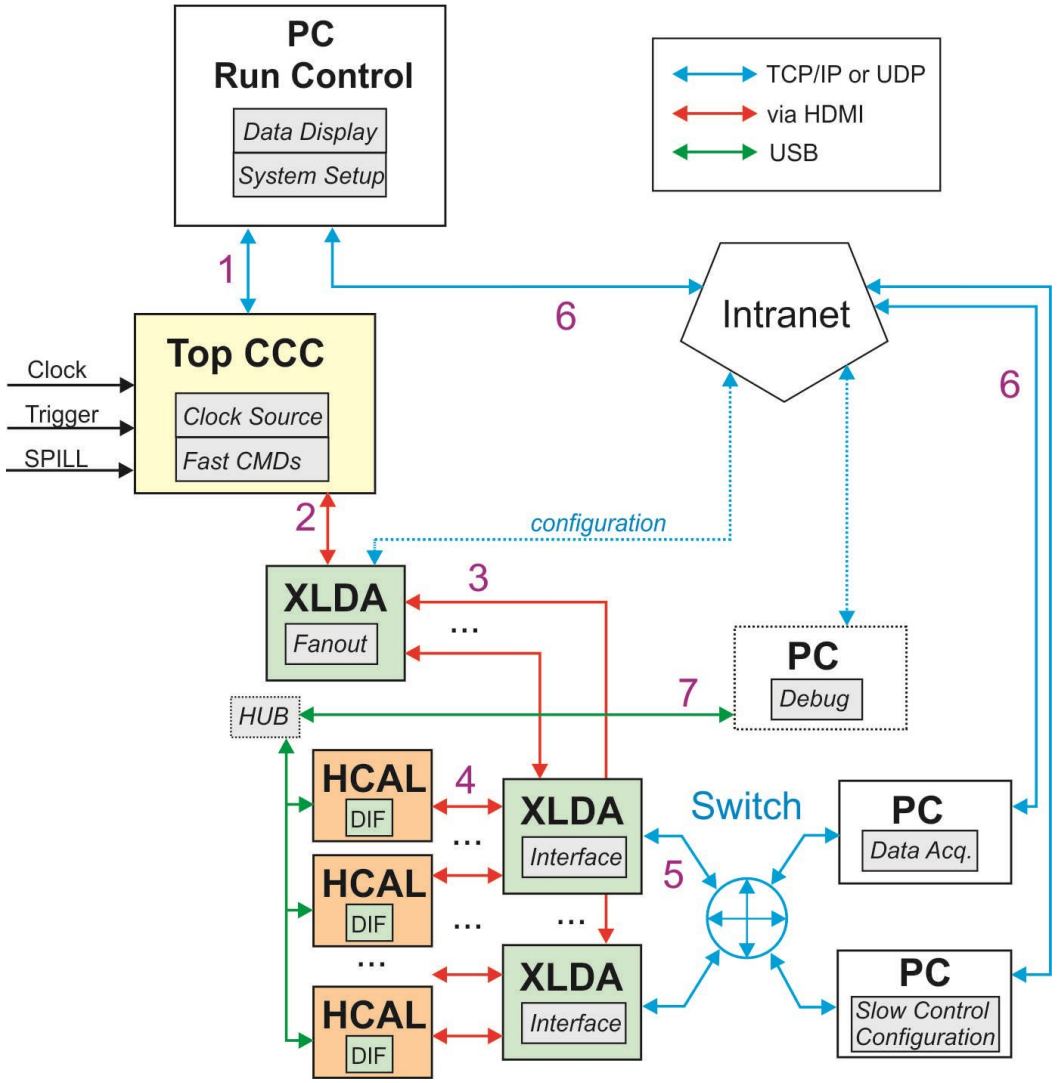


A track in 5 layers at test beam


HCAL+ScECAL

Next Version of DAQ

- In cooperation with university of Mainz
- Currently in concept design phase
- More distributed task
- **x-LDA to be fully implemented**
  - **No USB**
- To be operated by the end of the year in testbeams at CERN
- Combined testbeam with other CALICE detectors possible



Reporting Issues

AHCAL Milestone

- MS 45: Calibration and power supply system
  - Due on month 36 (Jan 2014), lead by UIB
  - Short report is sent to management, public note in prpareation

AHCAL Deliverables (with other sub-tasks)

- D 9.7 - Integrated infrastructure for highly granular calorimeters
  - Due on month 40 (May 2014), lead by DESY
  - Plan to re-use periodic reports to compile a document
- D 9.9: Adequation of Geant4 simulation of hadronic showers in different media (report)
  - Due on month 46 (Nov 2014), lead by DESY
  - Bundle CALICE publications and notes

Next Steps and Summary

Next steps

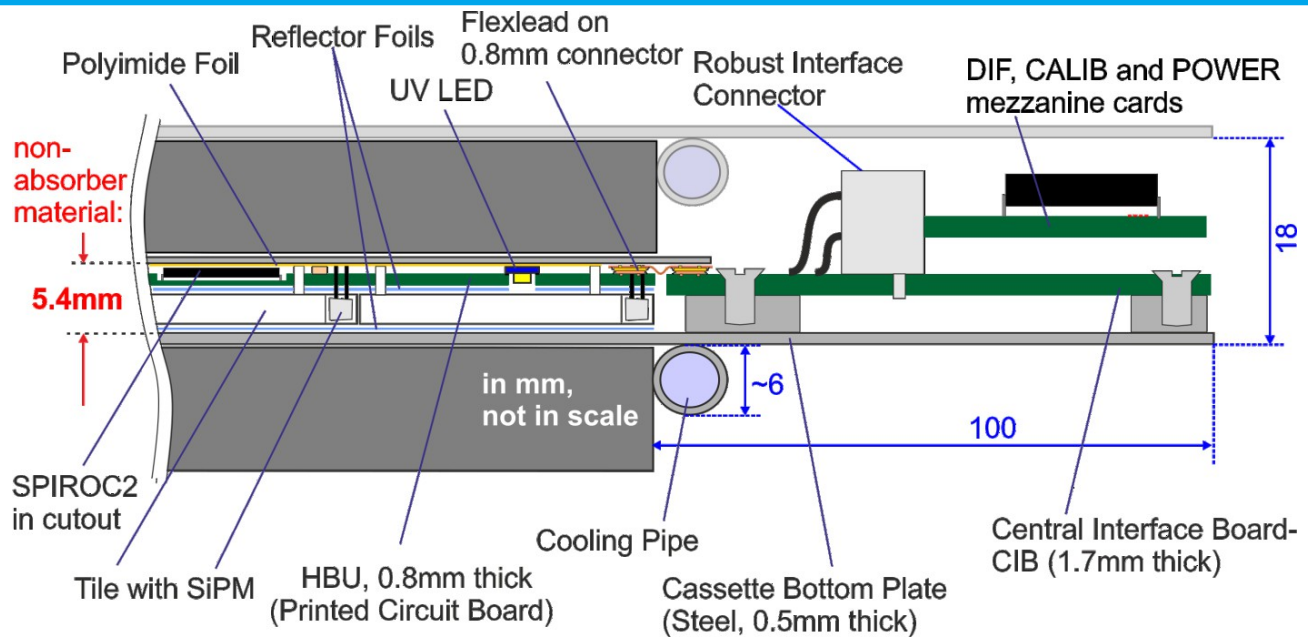
- HBU3 production
- More HBUs to be commissioned to enlarge the system
- Fully incorporate LDA into DAQ system
- CERN testbeam towards the end of the year

Summary

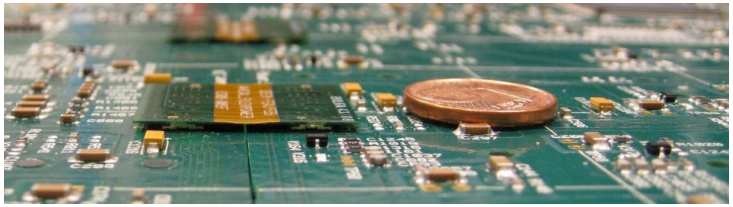
- AHCAL development is continuously in progress
- Electronics and DAQ tested successfully in various testsbeam
- HBU redesign is finished
- Power pulsing is being tested, so far successfully
- New tiles are tested and used to equip HBUs
- DAQ being further developed and tested

Backup

AHCAL Layer Cross-Section

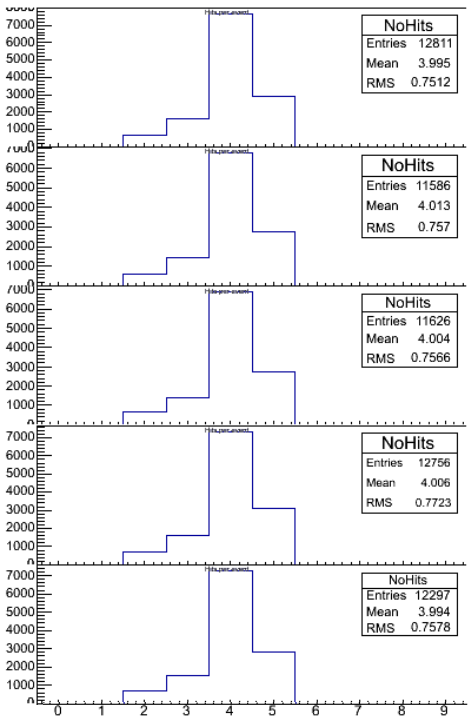


- Tight space between absorbers
  - 5.4 mm thick slits
  - 3 mm is used by the plastic scintillators
- Extra thin PCB
- ASICs are placed in cavities on PCB
- 0.8 mm connectors are used

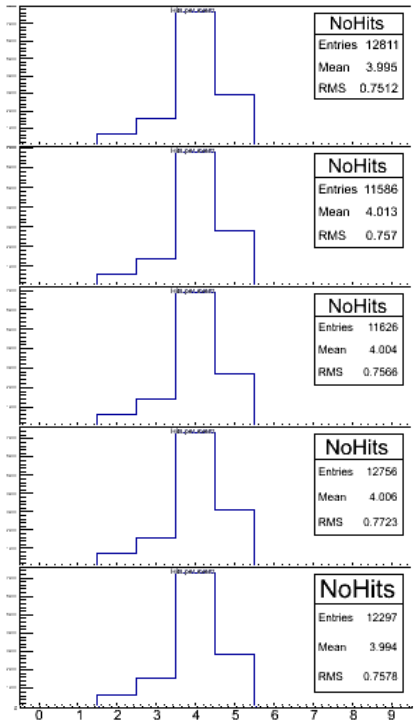


Multilayer Synchronicity

- During July test beam we tested synchronicity
- For the same run, number of hits was checked in two different event builders
  - Accepting only the same bunch crossing IDs
  - Accepting bunch crossing IDs +/- 1
- Absolutely no difference is observed



Same BunchX ID

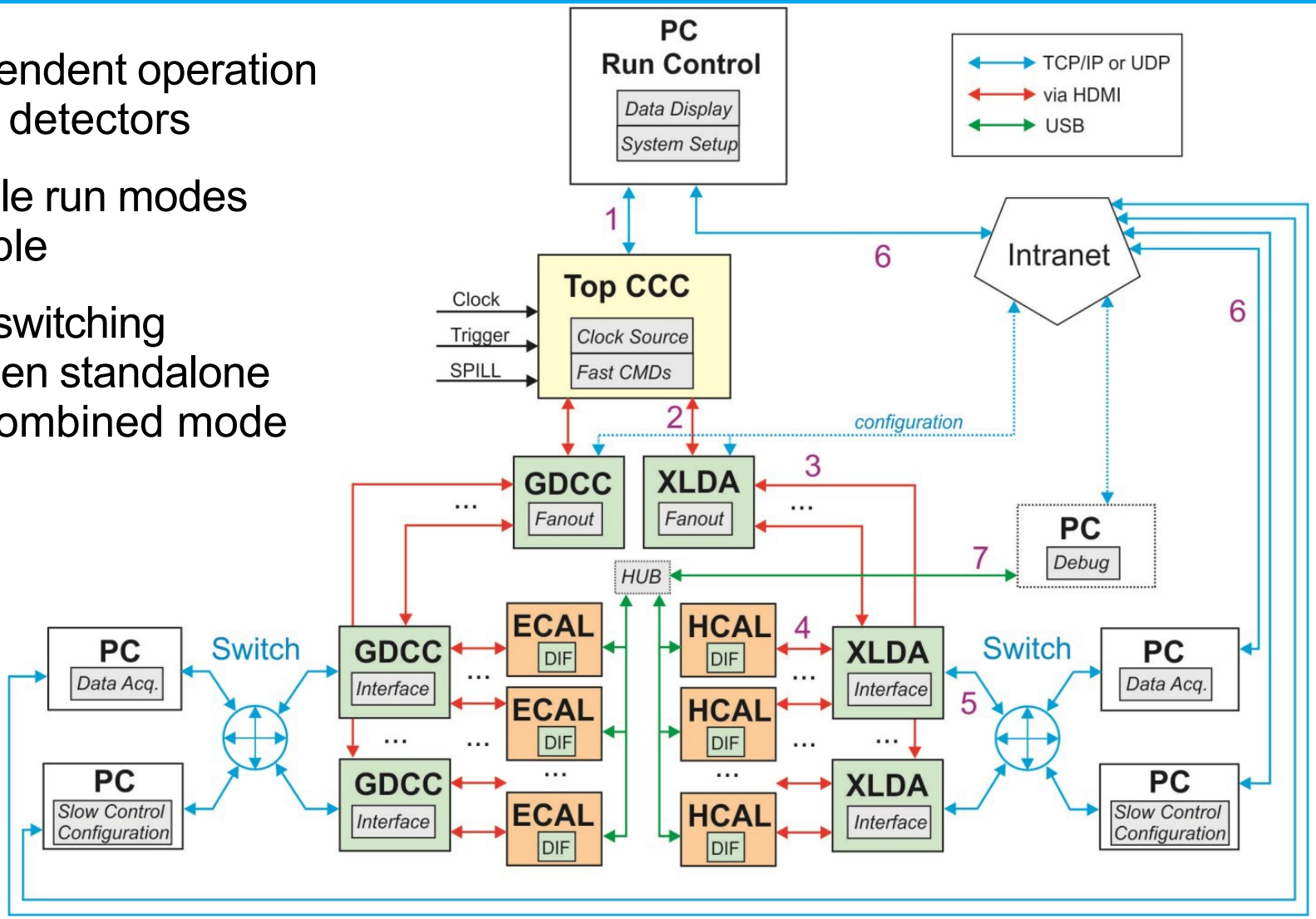


BunchX ID +/- 1

- We have a true synchronous detector 

Combined DAQ

- Independent operation of the detectors
- Multiple run modes possible
- Easy switching between standalone and combined mode



PFA

- International Large Detector(ILD)
  - The goal is to reconstruct energy of individual particles
- Particle Flow Approach(PFA)
  - Tracking detector → Charged Hadrons
  - EM calorimeter → Photons
  - Hadronic calorimeter → Neutral Hadrons
- PFA Performance is sensitive to detailed structure of hadronic showers
  - HCAL should be able to distinguish between W and Z decays
- Requires excellent tracking and highly-granular calorimeters