SemiDigital HCAL Overview

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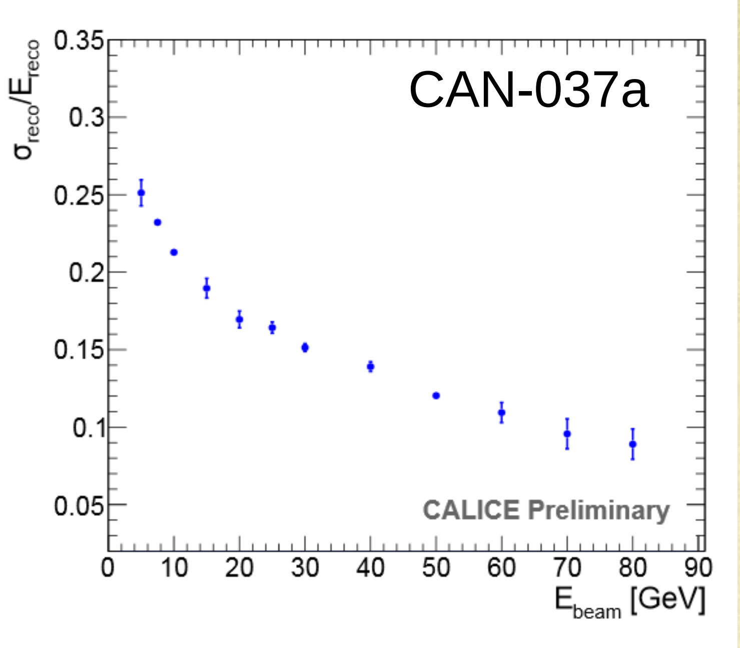
Outline

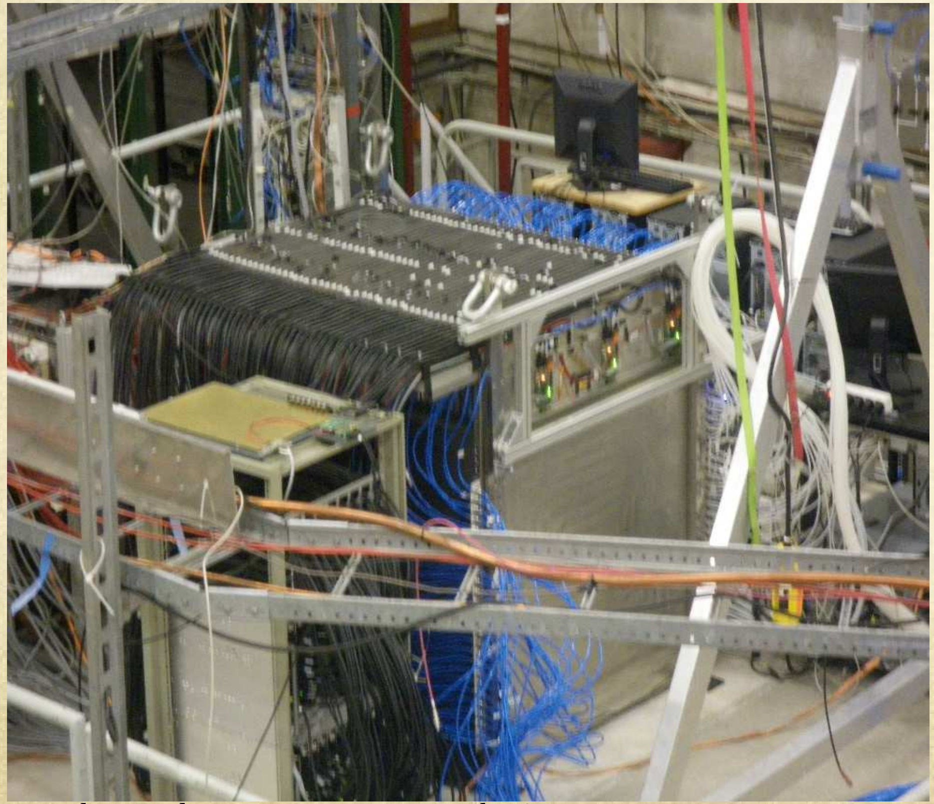
- ✓ Chambers
- ✓ Electronics
- ✓ Mechanics
- ✓ Conclusions

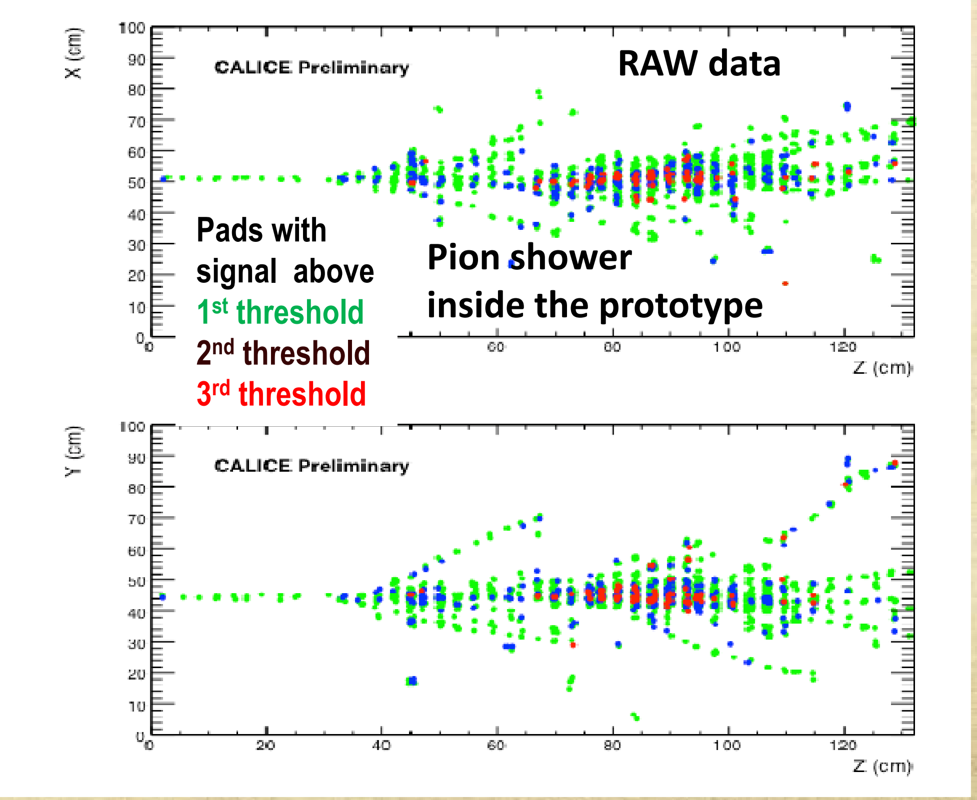
1m^3 prototype



SDHCAL GRPC (50 units)

→Large detectors : 100X100 cm^2 GRPC
→Readout : pads 1x1cm^2 , semidigital 3 thresholds
→Electronics : HARDROC, embedded
→ Cassette design : ok, part of the absorber
→ DAQ : ok, not the final





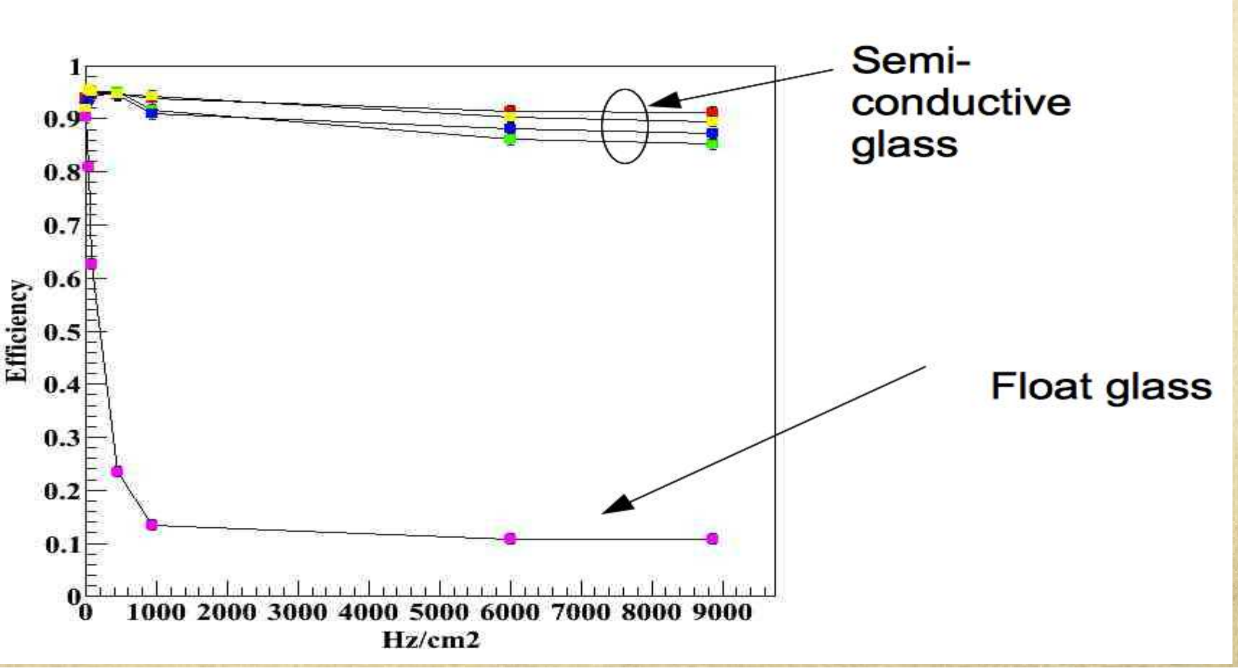
Chambers

High-Rate GRPC

High-Rate GRPC may be needed in the very forward region

✓Semi-conductive glass (10^{10} Ω.cm) produced by our collaborators from Tsinghua University was used to build few chambers.
✓4 chambers were tested at DESY as well as standard GRPC (float glass)

Performance is found to be excellent at high rate for GRPCs with the semi-conductive glass and can be used in the very forward of ILD region if the rate exceeds 100 Hz/cm^2 in future ILD upgrades as well as for CLIC



It has been also proposed for the CMS muon system upgrade

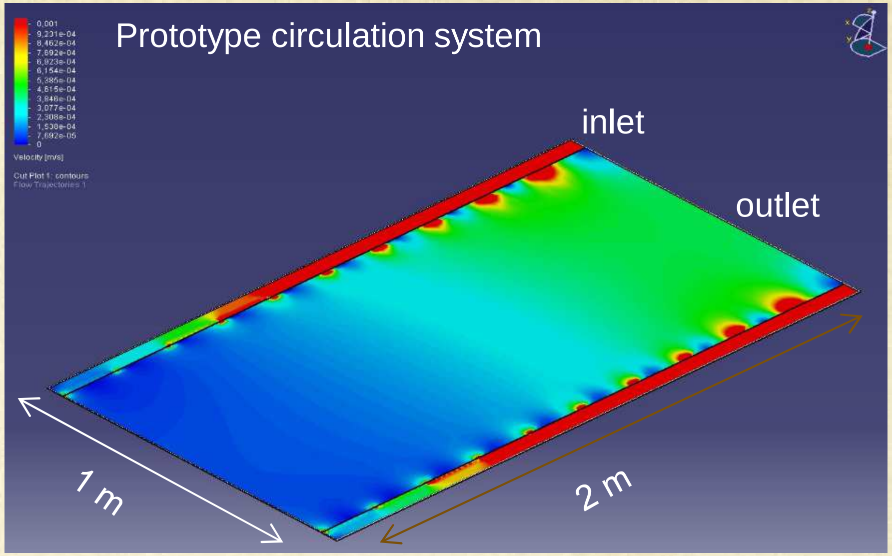
Large GRPC for ILD model:

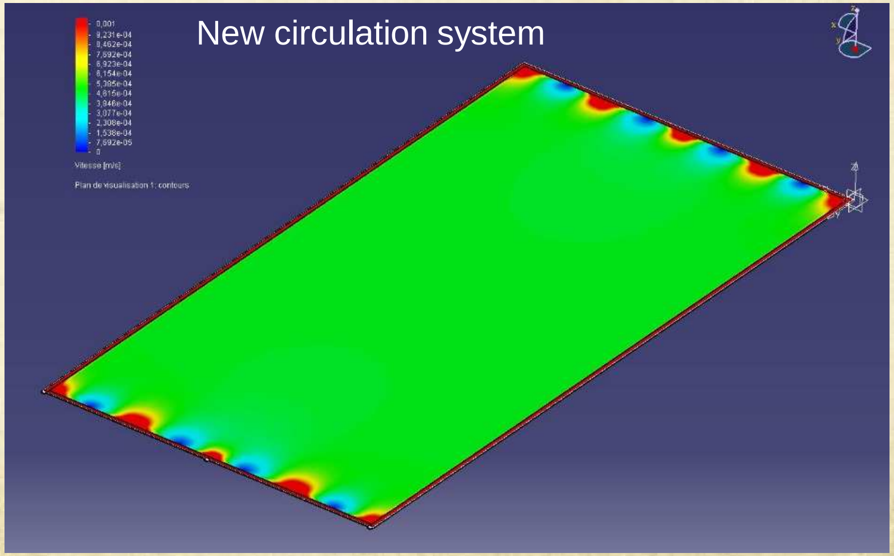
GRPC with a surface
≤ 3 m^2 are needed.

We intend to build
a $2m^2$ GRPC.

We are currently studying
the gas distribution system
to ensure a good gas
renewal.

Once the first large detector is built
the gas circulation of the new scheme
will be controlled using radioactive
^{183m}Kr

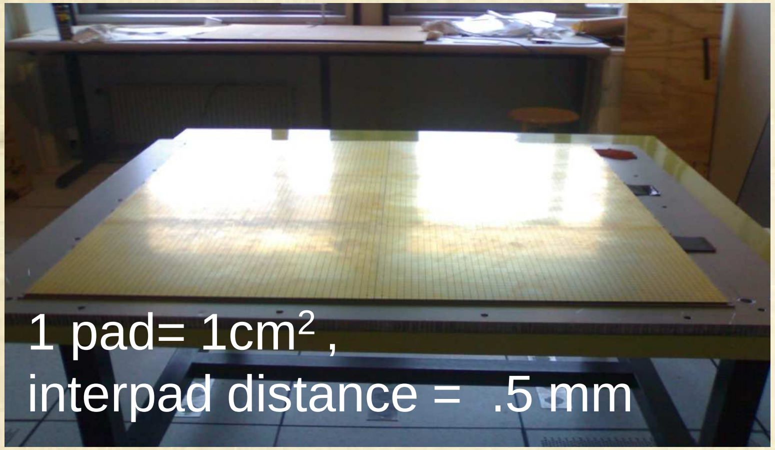


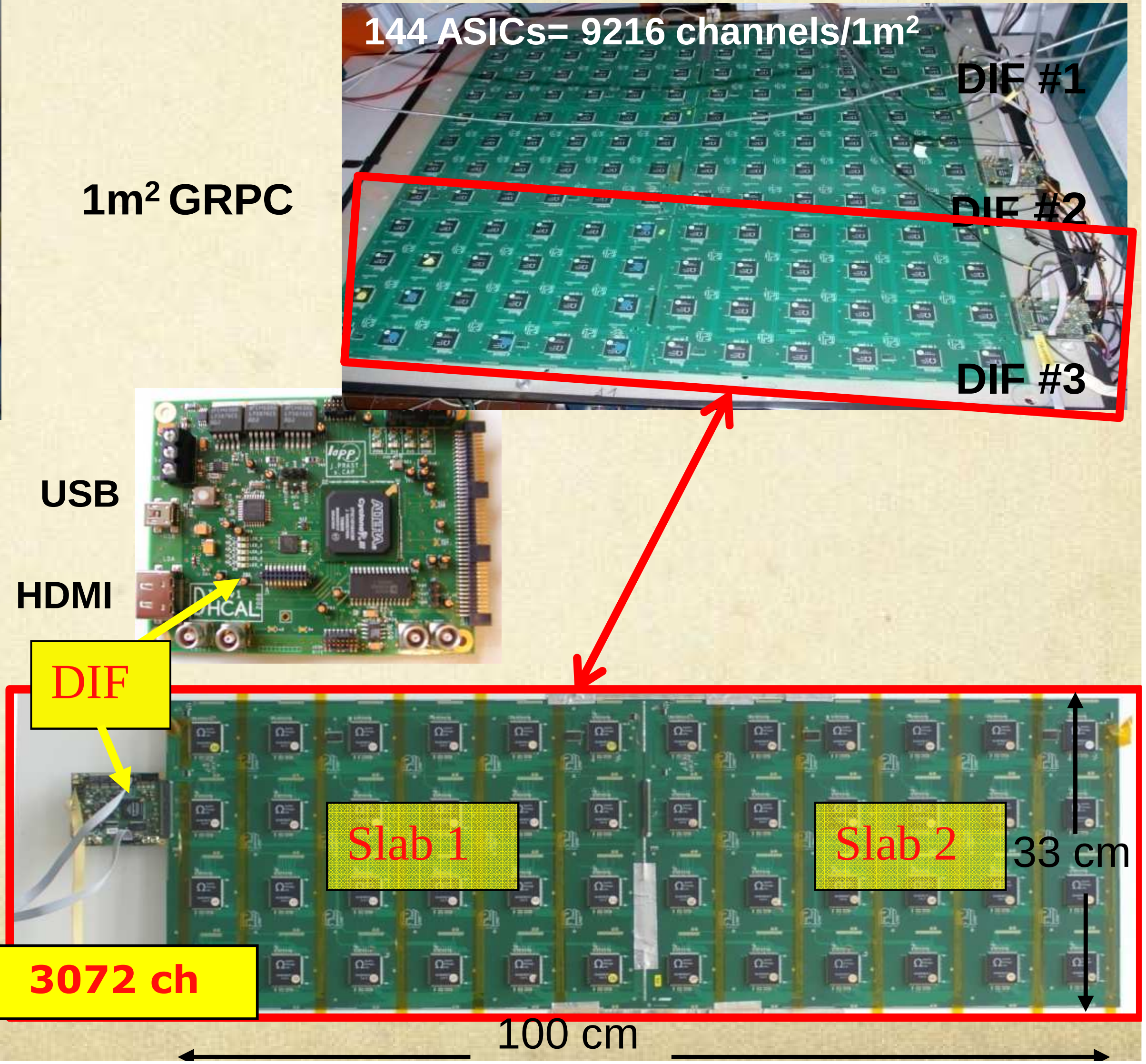


Electronics

GRPC electronics – 1m^3 prototype

The HARDROC ASICs are hosted in a Printed Circuit Board (PCB).
PCB provides the connection between adjacent chips and link the first to the readout system
PCB contains in the opposite face the 1x1cm^2 copper pads for the GRPC readout





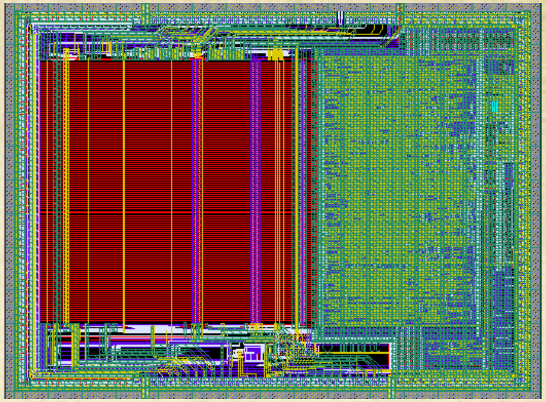
For the 1m2 detectors:

6 PCBs hosting 24 ASICs.

Every two PCBs connected to each other and connected to one DIF (Detector InterFace) card

3 DIFs per GRPC

HARDROC3



This new version of the HARDROC ASIC has:

-64 independent channels, zero suppression

-I2C link

-PLL: Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz

Bandgap: new one with a better temperature sensitivity

Triple voting

Roll mode

Temperature sensor: tested in a building block, slope – 6mV/°C

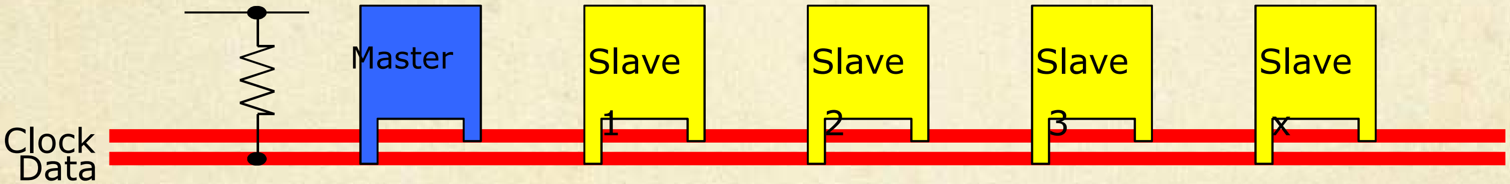
Die size ~30 mm2 (6.3 x 4.7 mm2)

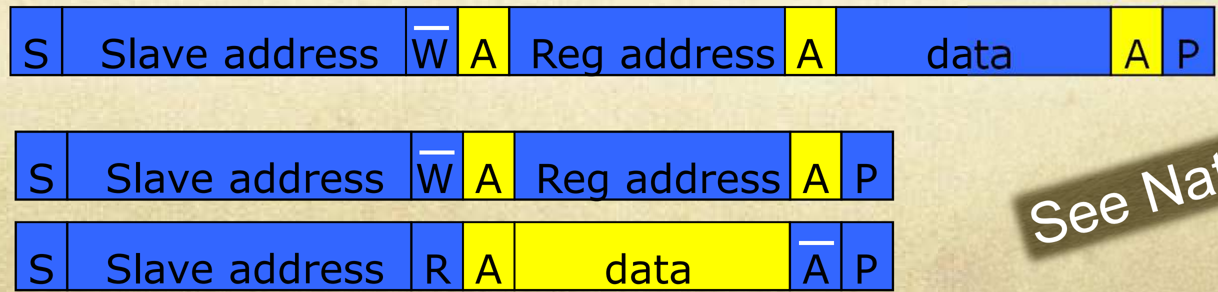
Packaged in a TQFP208

The ASIC was produced and tested. All functionalities were successfully tested.

A minor problem was found with the I2C scheme (buffer stuck to zero)

This I2C was however successfully tested after a BIF.

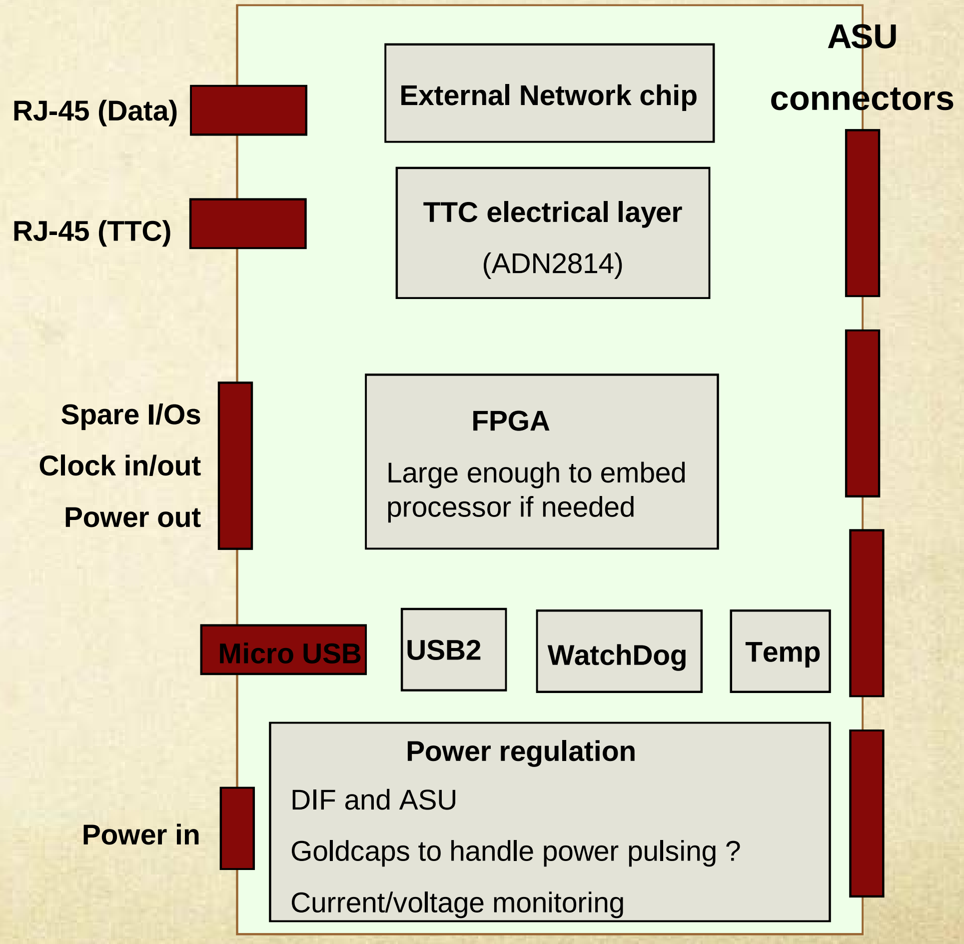




See Nathalie Seguin's talk

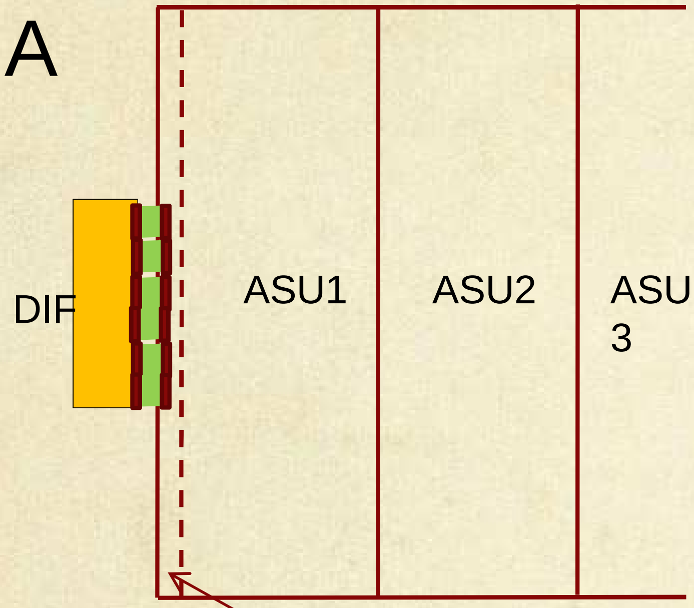
New SDHCAL DIF main features

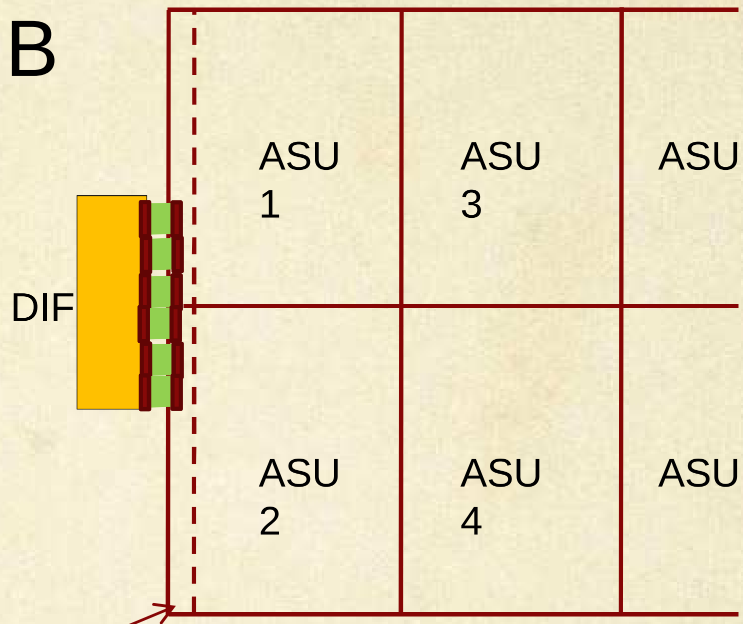
- Only one DIF per plane. For the maximum length plane (1x3m) the DIF will handle 432 HR3 chips
- Slow control through the new HR3 I2C bus
- Data transmission to DAQ by Ethernet using commercial switches for concentration
- Clock and synchronization by TTC
- USB 2.0 for debugging
- Synergy with R&D on fast links R&D of LHC(GBT)



New ASU layout options

As there will be only one DIF per plane, the distribution of the ASU boards in the plane will be rearranged to reduce the number of conections between the DIF and the plane





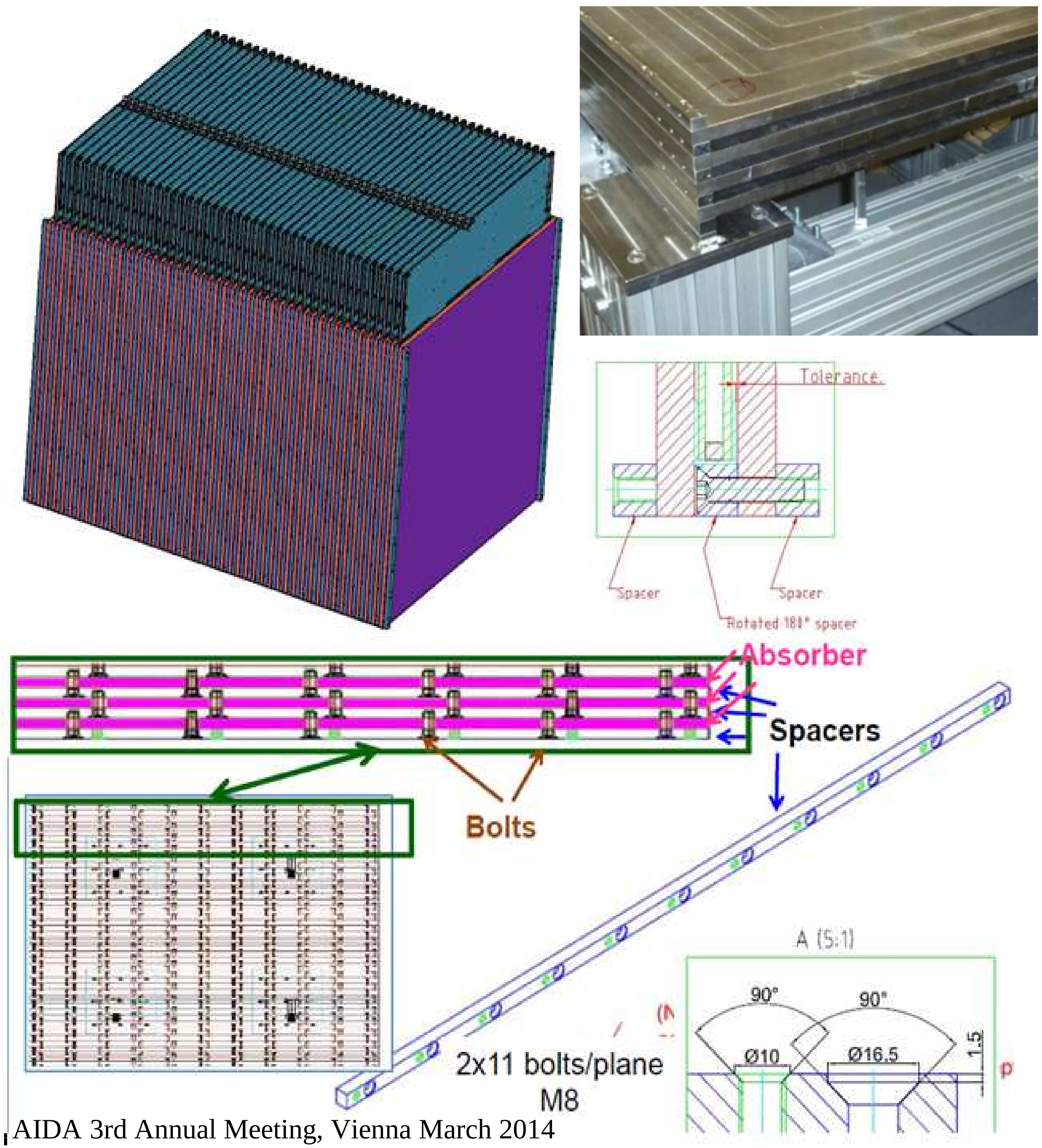
First ASU extension for drivers & connectors

- In option B the common signals for the plane have to be sent twice (one per slab) while in option B they can be sent only once
- But, option A looks more risky from the point of view of the feasibility of the 1m long ASU boards.

- In both options the ASUs connected to the DIF will be a bit longer to host the connectors and the buffers for driving the long lines. This extension provides more freedom for the connectors selection and moves the drivers heat disipation to the ventilation area

Mechanics

From the 1m³ mechanic structure to the final one



The 1m³ mechanical structure was made of 51 stainless steel plates assembled together using **lateral spacers fixed to the absorbers** through **staggered bolts.**

Thickness tolerance 0.05mm
Surface planarity < 0.5 mm
➔ **< 1mm for the big plates**

For the **final structure**
➔ **Welding instead of bolts**

Allows to **decrease the lateral size of the spacer**
➔ **Less dead zone**

Could introduce **deformations**

Welding

Standard welding:

Could introduce **deformations**

Electron beam welding:

The **best** but **need vacuum conditions** and could be not affordable for big modules

Laser welding:

Could have **reasonable deformations** and is **easier (and cheaper) than electron beam welding**

Planned tests

Width of plates = 15mm

➔ Tests with small prototypes

Few plates of **1x 0.80 m^2** welded by **electron beam welding (EBW)** process in vacuum at **CERN**.

Few plates of **1x 0.40m^2** with **standard welding** at **CIEMAT** trying to see if it´s possible to find methods for optimizing the procedure and minimizing the eventual deformations

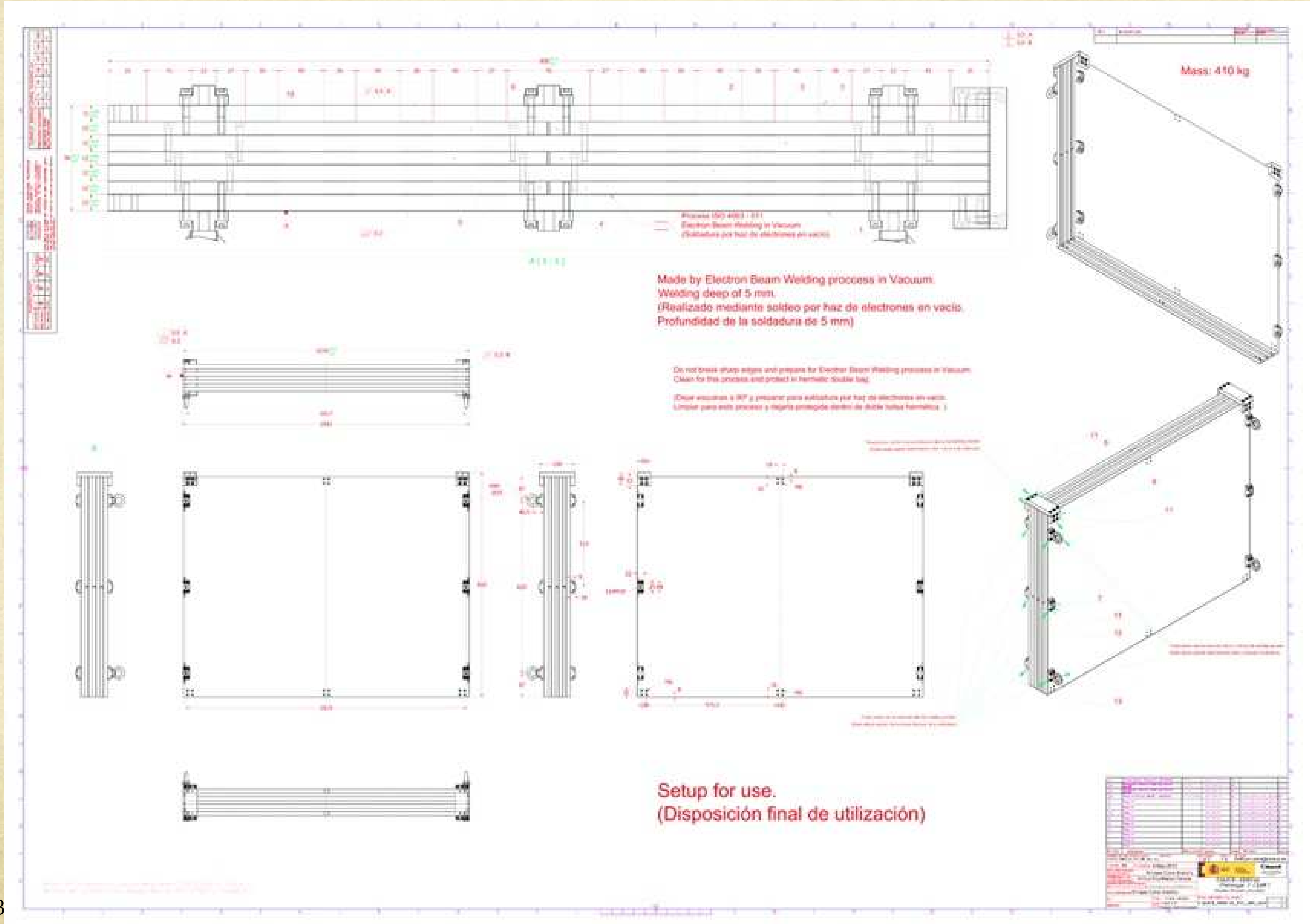
Depending on the results from those tests ➔ **Laser welding** test will be considered

➔ Test with a prototype with large plates

Assembly of a prototype with 4-5 plates with the largest dimensions (**3 x 0.80 m^2**) of an **ILD SHDCAL module**

➔ It will be equipped with some large GRPC chambers and its new electronics

Electron beam welding tests: Plans of the prototype



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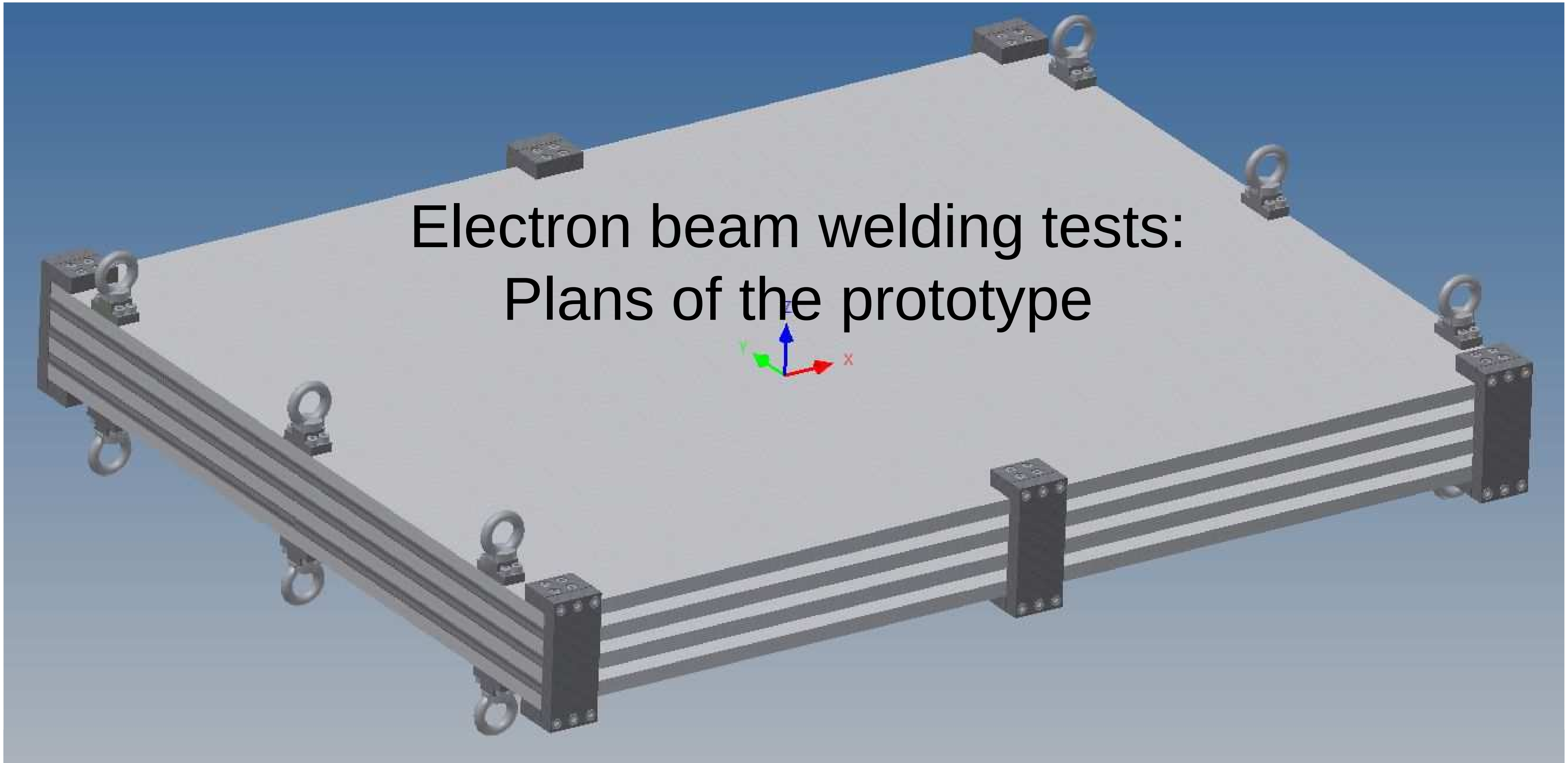
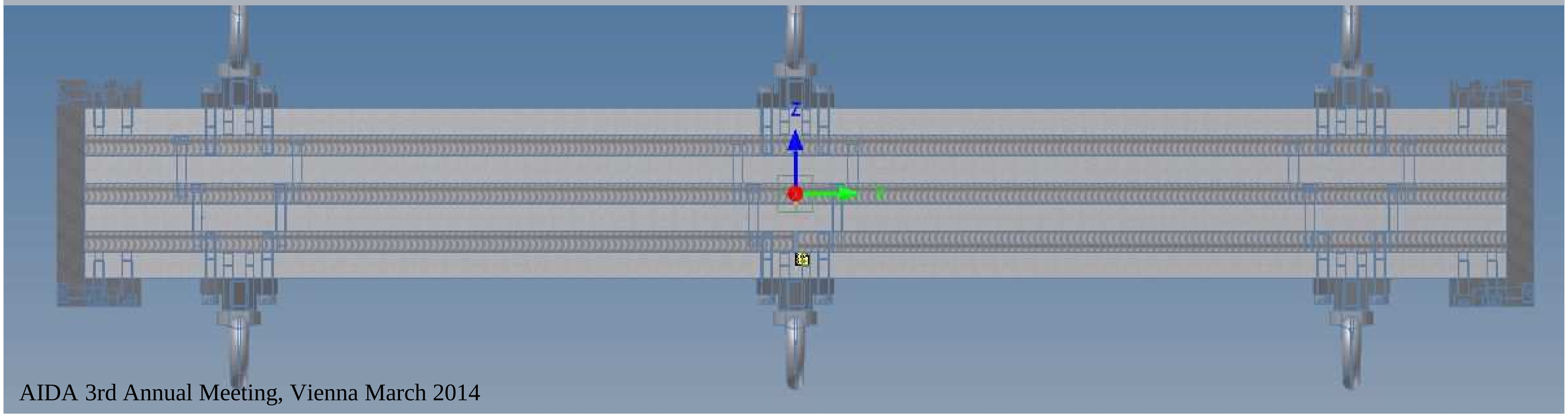
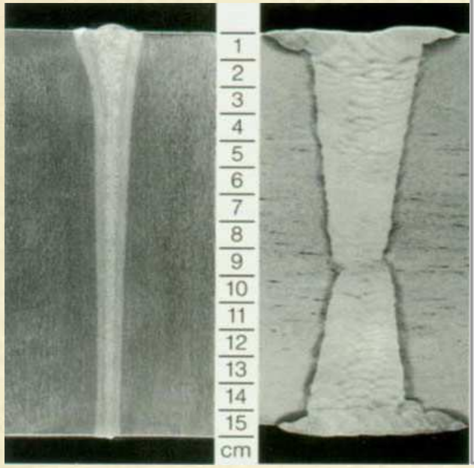
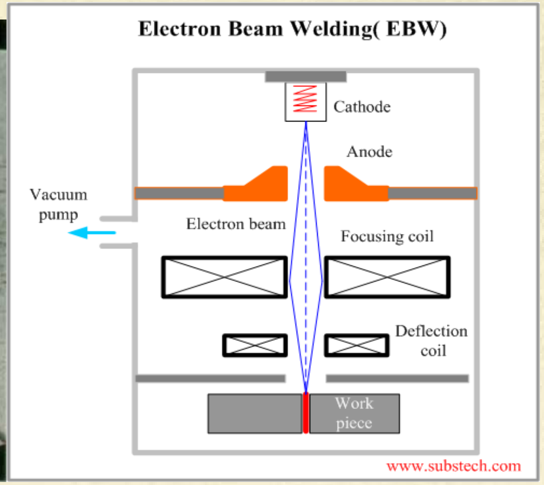


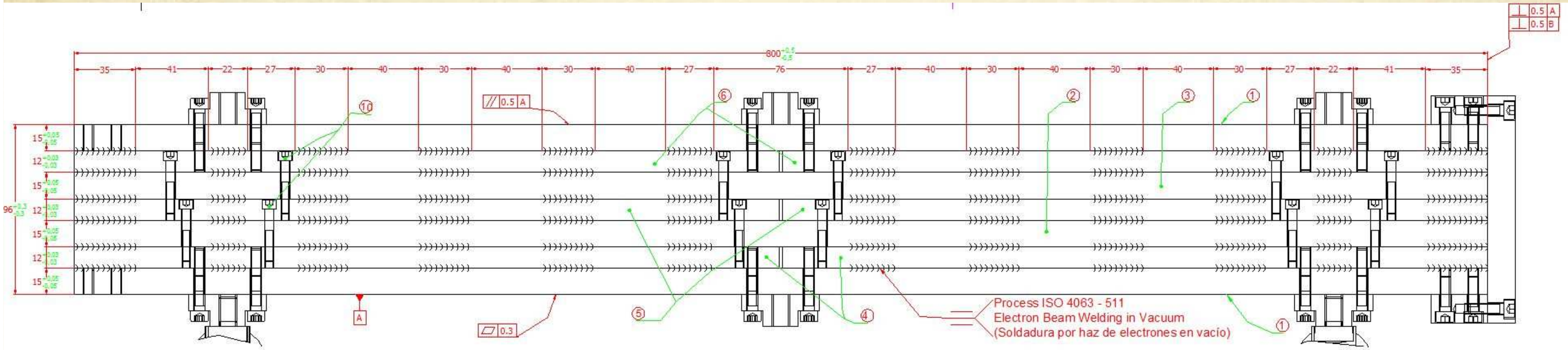


Electron beam welding tests: Welding details



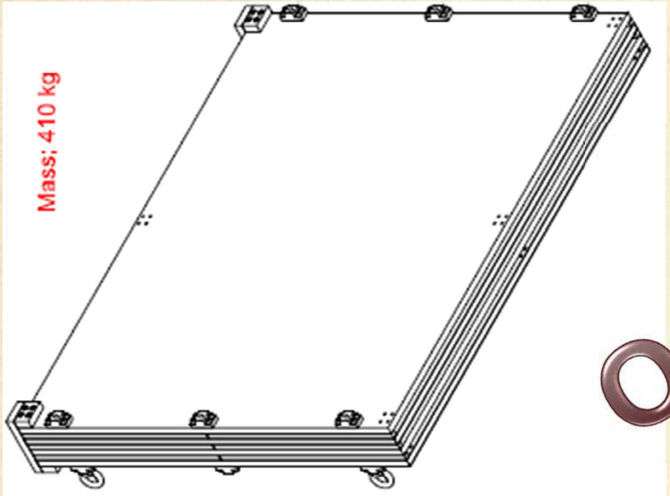


Welding techniques



Made by Electron Beam Welding proccess in Vacuum.
Welding deep of 5 mm.

Electron beam welding tests: Plate machining and verification



Ongoing

Large plates prototype

Ongoing

Conclusions

Very **large detectors** are being conceived and will be shortly build

New **electronics** being developed (**chip** and **readout**)

New **mechanic** design using **welding**

- ➔ Preparation for tests is ongoing
- ➔ A mechanical structure with 4-5 large plates is foreseen.