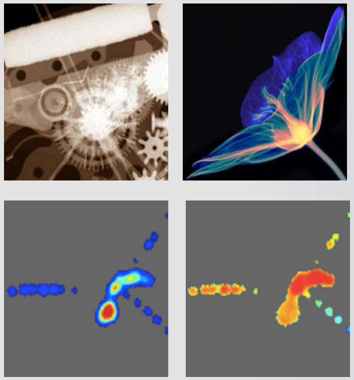


TSV EXPERIENCE WITH MEDIPIX

Jerome Alozy and Michael Campbell
CERN
Geneva, Switzerland

26 March 2014

AIDA Workshop

Outline

Projects and context

LETI process reminder

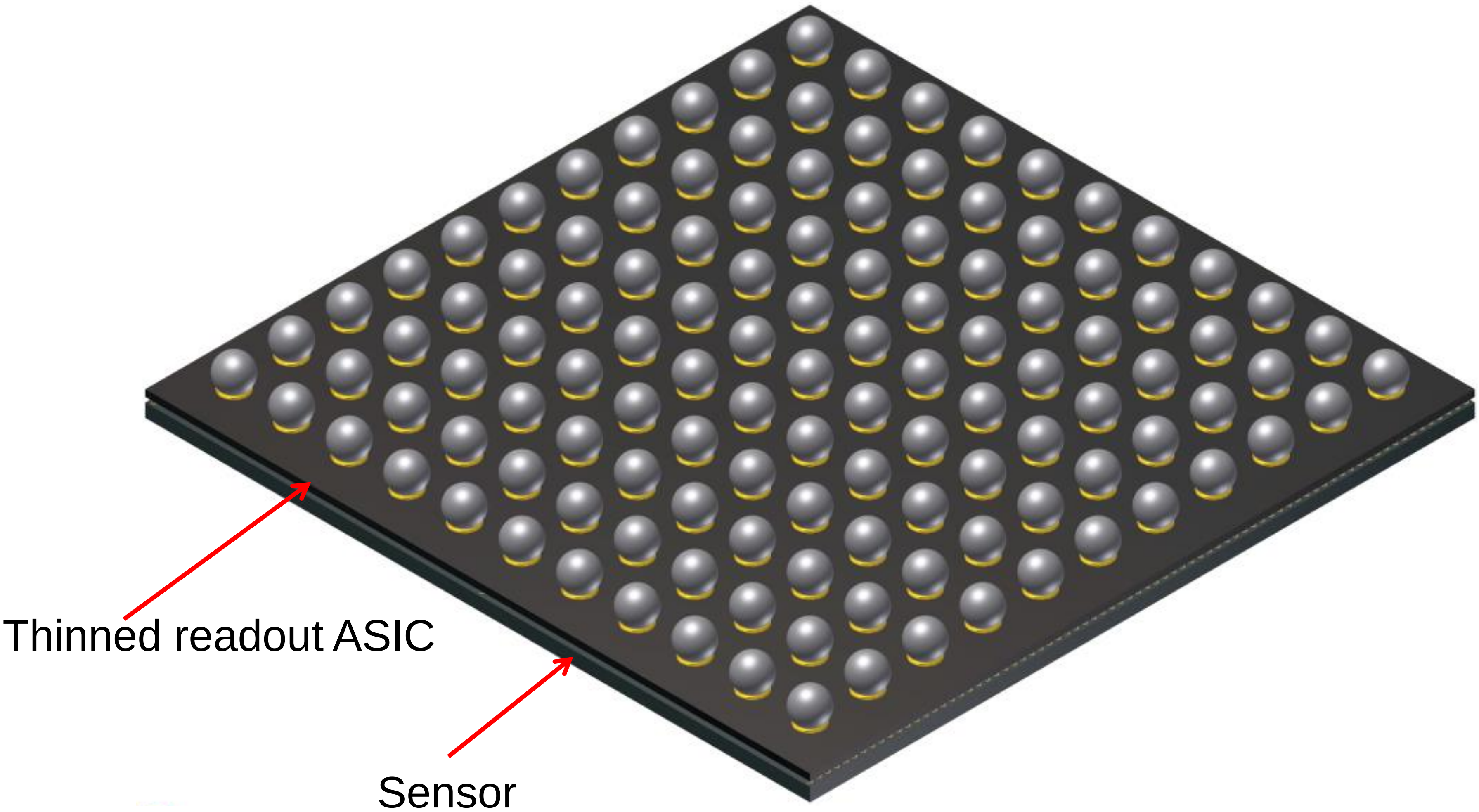
Medipix3 – designed for TSVs

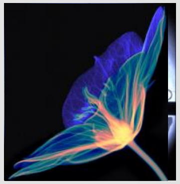
Status of Medipix3 project

First results

Summary and Future plans

Aim - 4 side buttable tile of Hybrid Pixel Detector



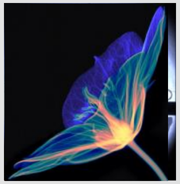


Context

The Medipix3 Collaboration has committed resources to the development of TSV’s to enable seamless large area coverage for imaging

In the context of the AIDA project, CERN seeks to develop the TSV-last concept for vertex detectors – versatile geometry, yield improvement

CLIC-LCD aims to develop technologies suited to ultra low mass vertexing with good timing precision



3 projects with CEA-LETI

1) Demonstrate feasibility of TSV-last processing on Medipix3.1 – completed

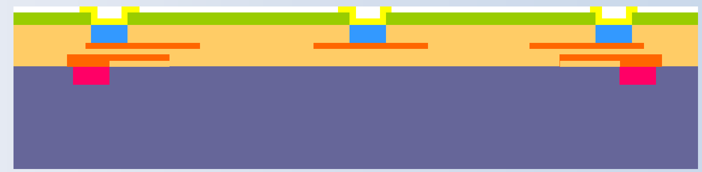
2) Demonstrate mastery of yield using Medipix3RX wafers – on-going

3) Demonstrate feasibility of TSV-last processing on Timepix3 wafers – aim 50μm ASIC on 50μm sensor – order just out

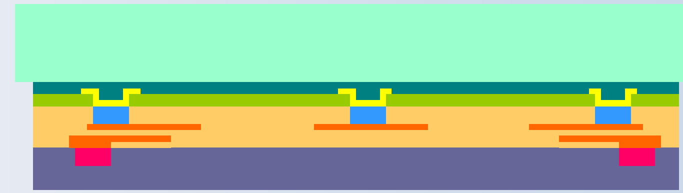
Reminder of LETI Process

- **Front Side UBM**

UBM
  - TiNiAu Deposition
  - Litho UBM
  - UBM etch

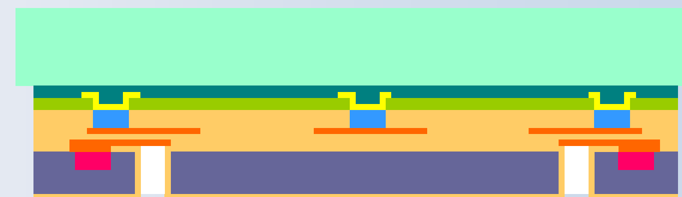


- **Bonding / Thinning**
  - Bonding
  - Grinding/edge dicing
  - CMP Si

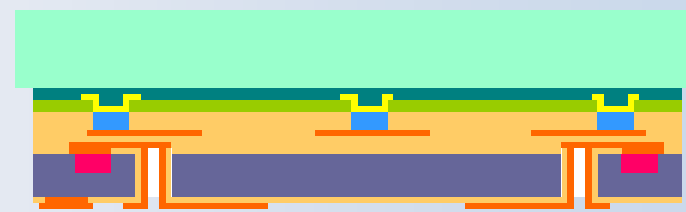


- **Back Side: TSV Last + RDL + Passivation + UBM**

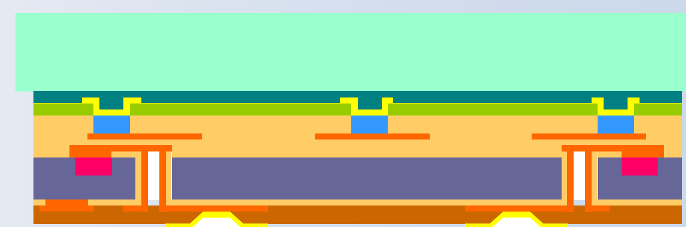
TSV
  - Litho TSV
  - TSV AR2 etch
  - SiON conf deposition
  - Etch back



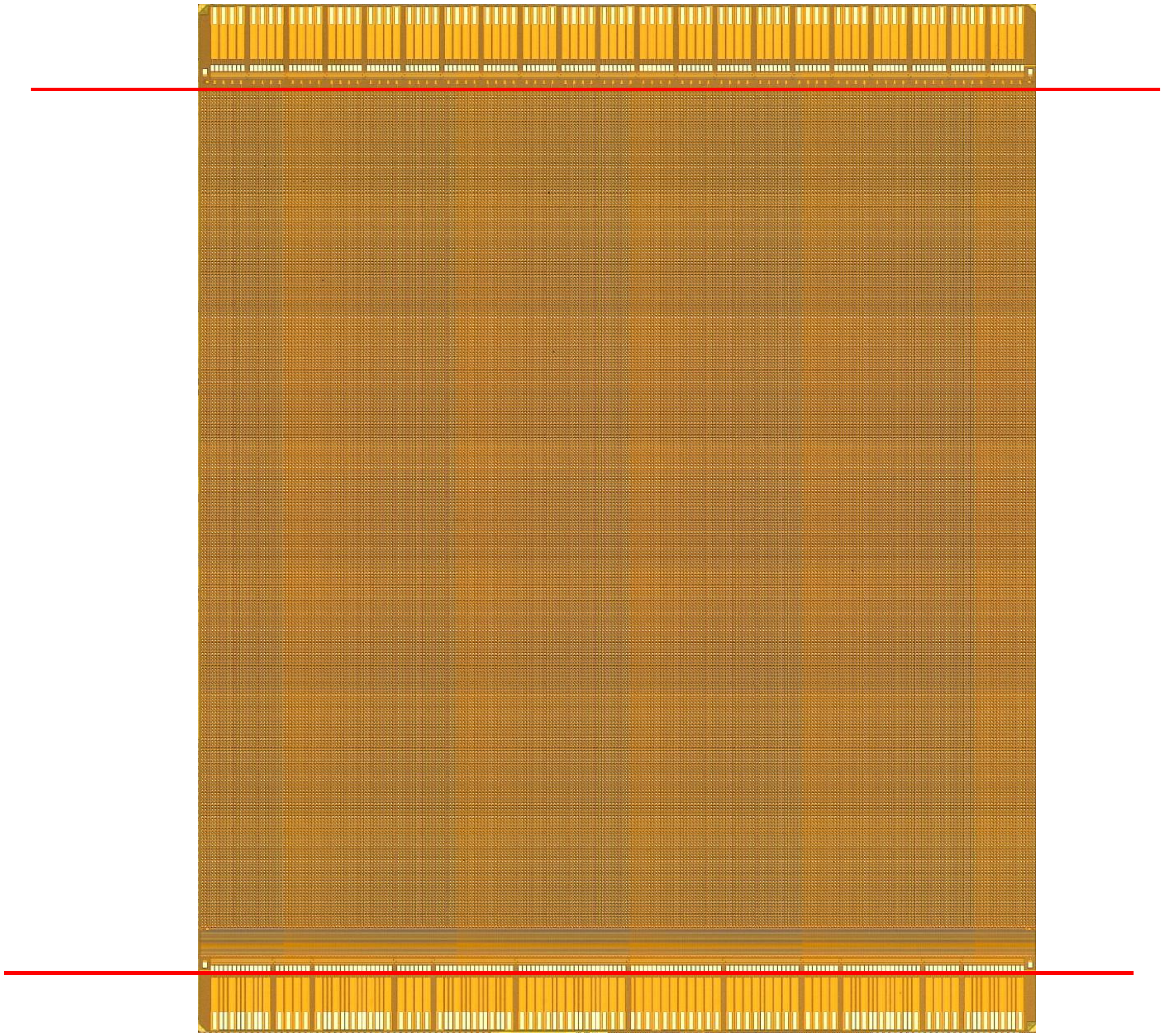
RDL
  - SEED TiCu
  - Litho RDL
  - ECD Cu
  - Litho PASSIV



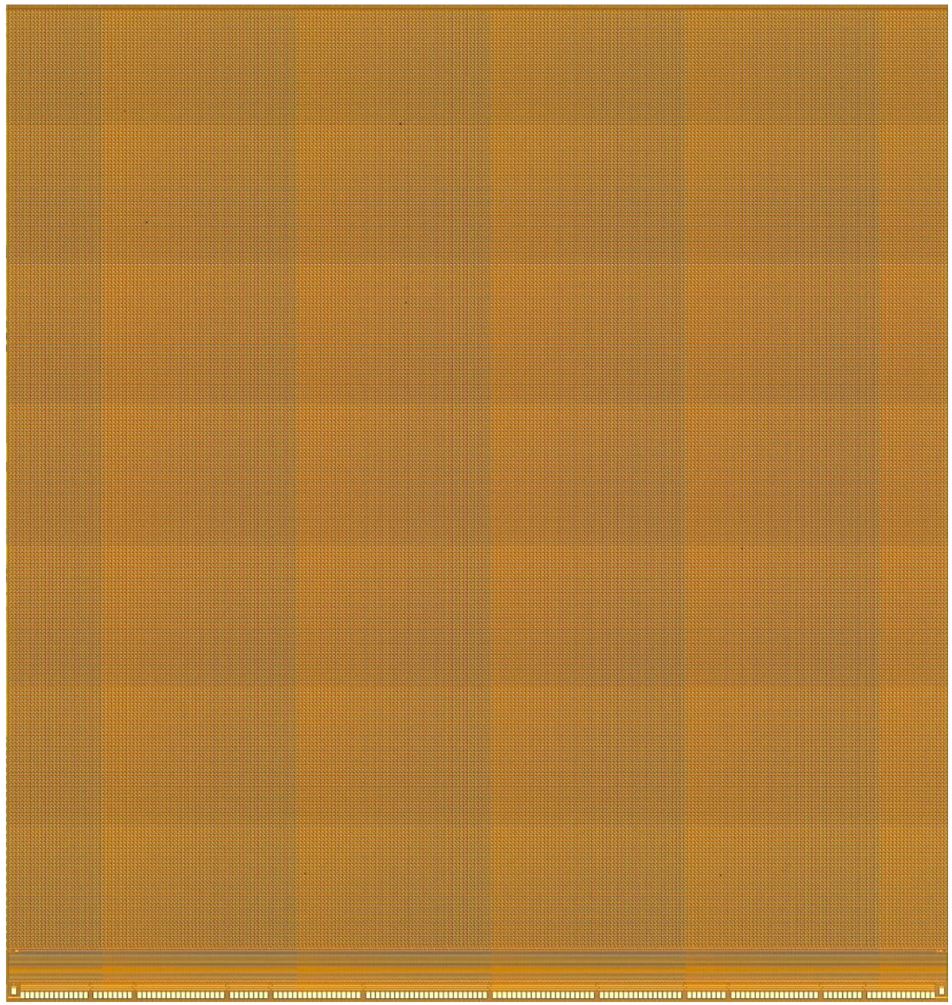
UBM
  - TiNiAu deposition
  - Litho UBM
  - UBM etch
  - Debonding / Dicing



Medipix3 chip photo



Medipix3 ready for Through Silicon Vias



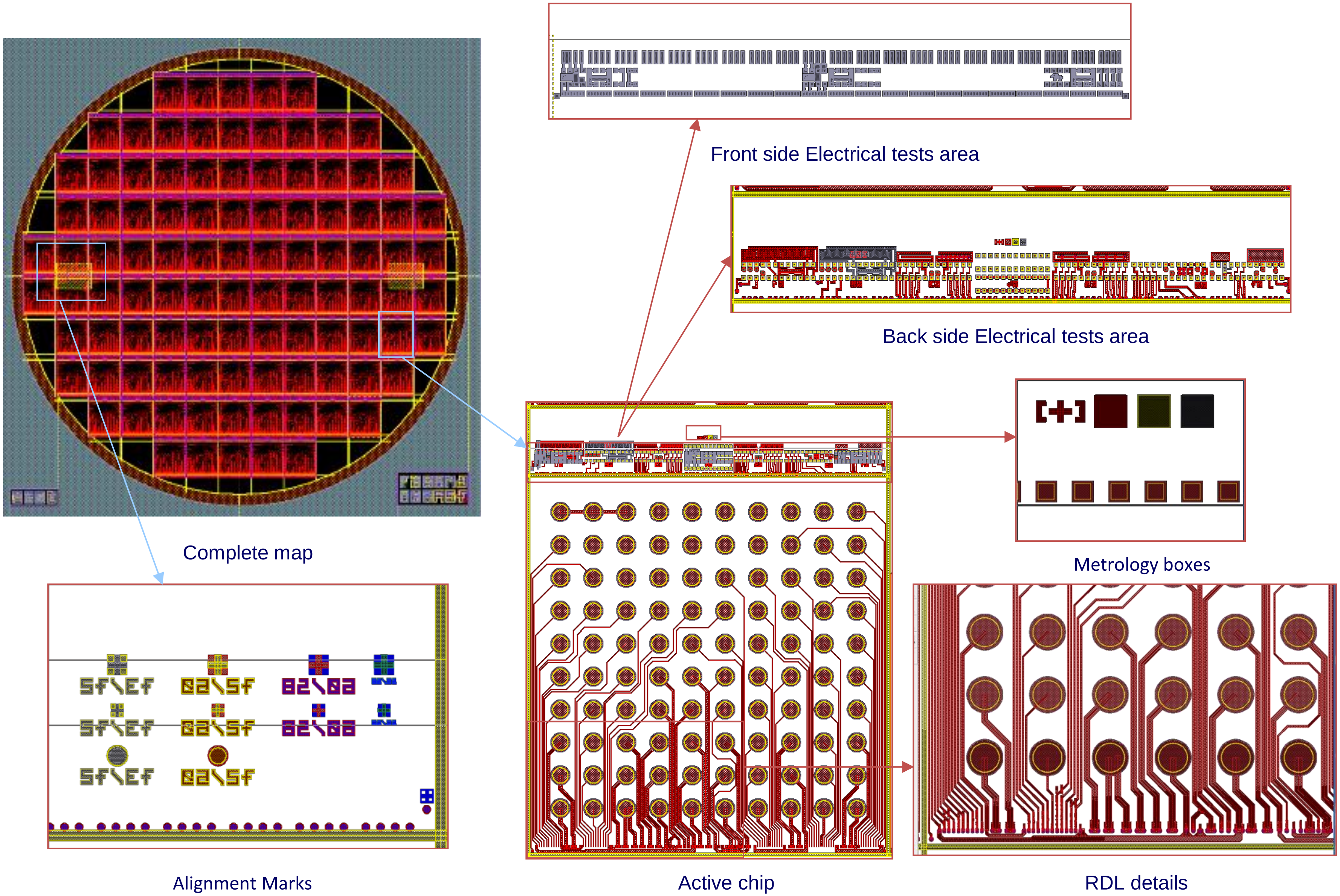
All IO logic and pads contained within one strip of 800μm width

All IO´s have TSV landing pads in place

Permits 4-side butting

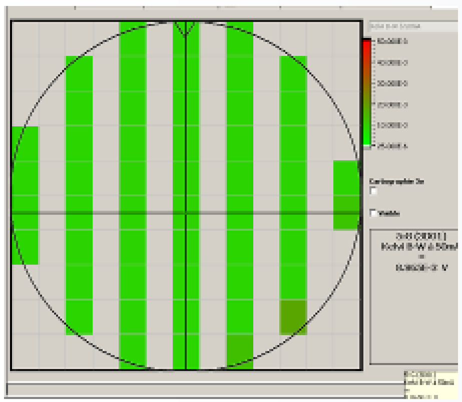
94% sensitive area

RDL design (Timo Tick)

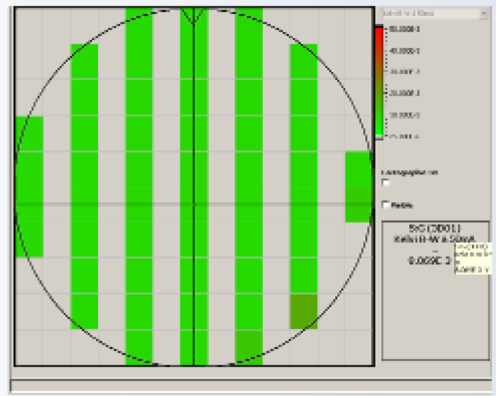


Medipix3.1 project results / electrical tests

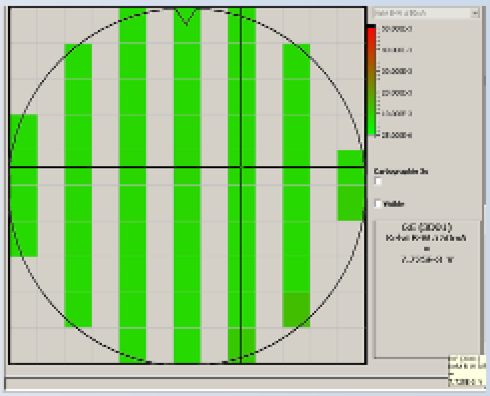
- **UBM/ Al contact resistance**



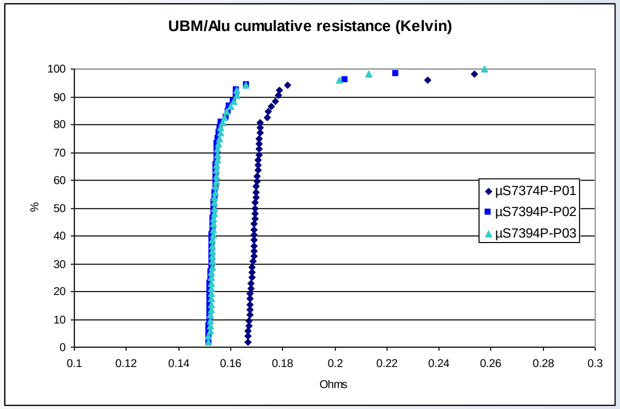
P01



P02



P03

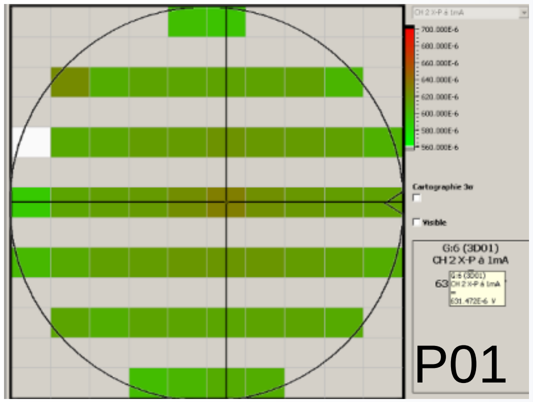


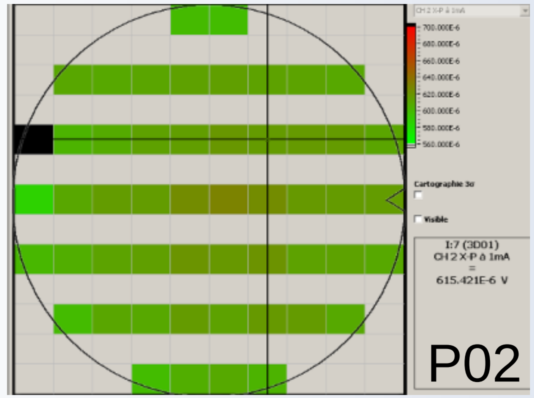
Cumulative resistance UBM/Alu
Mean value : ~ 150 mohms

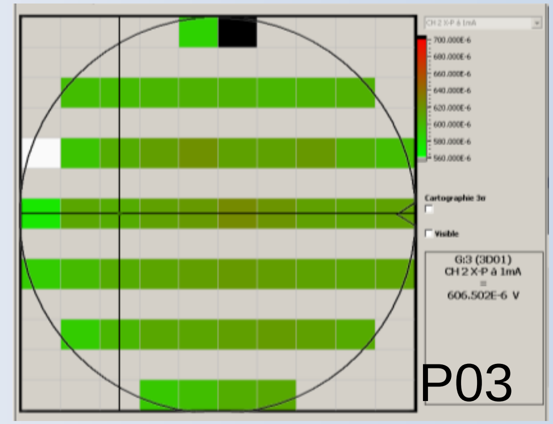
- **Conclusions:**
  - ☺ Isolation between UBM lines OK
  - ☺ Alu/UBM contact resistance is OK

Medipix 3 project results / electrical tests

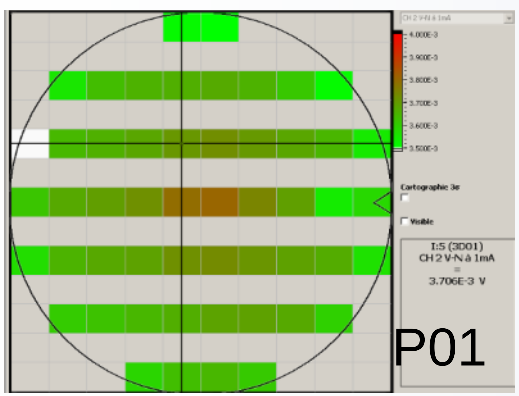
- **2 TSV chain resistance (by Vdd)** **1.23 Ω ± 3.6 % (1σ)**

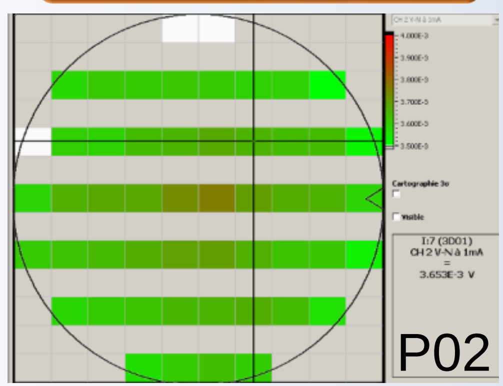


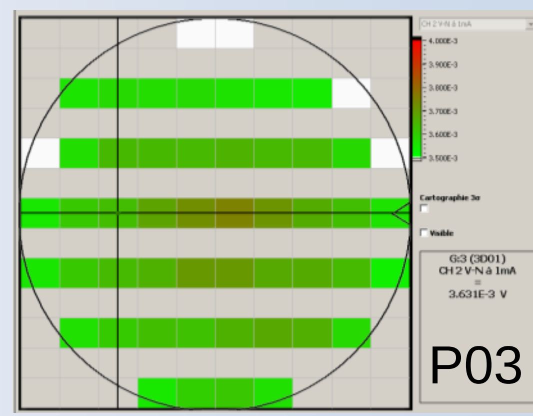




- **2 TSV chain resistance (by Vss)** **3.60 Ω ± 1.9 % (1σ)**





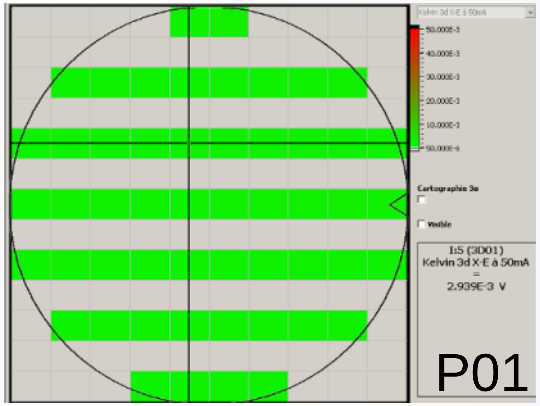


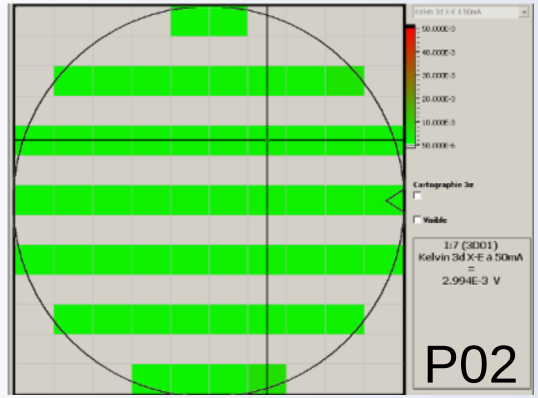
D. Henry, LETI

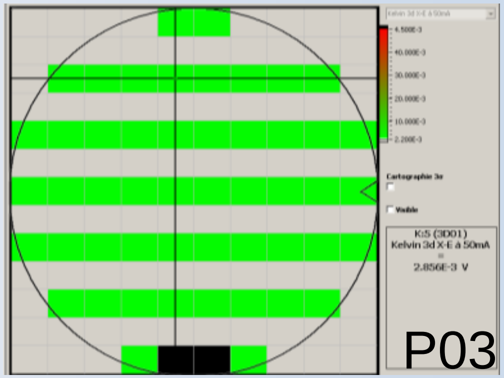
- **Conclusions:**
  ☺ Uniform distribution of values ➔ no comparizon with reference value possible

Medipix 3 project results / electrical tests

- **Kelvin TSV ➔ Mean value** **50 mΩ ± 14 % (1σ)**



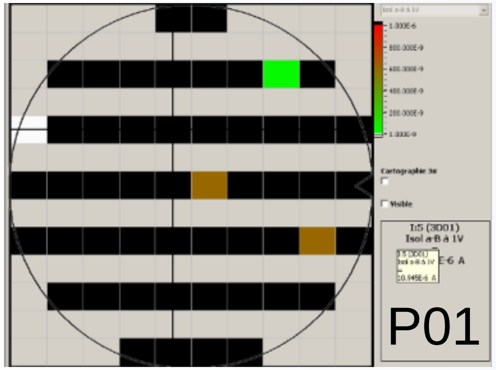


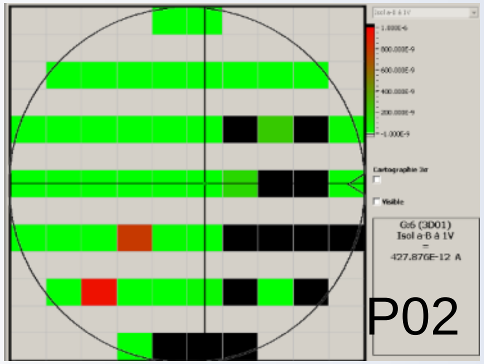


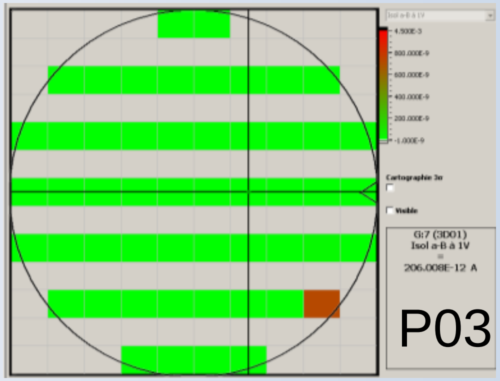
Kelvin3D (Specs < 1 Ohm/TSV) / Yield: 100%

Kelvin3D (Specs < 1 Ohm/TSV) / Yield: 96%

- **Insulation between 2 TSV (1 connected TSV to M1 & 1 non connected) – Applied voltage : 1V**







- **Conclusions:**

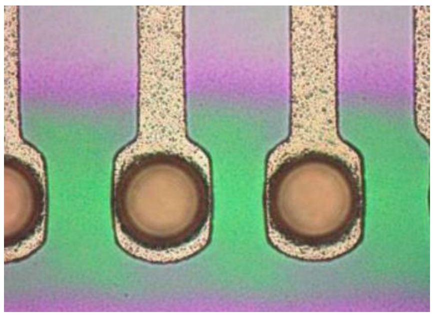
  Insulation issue on P01 & P02 / Root cause identified

  Correction on P03

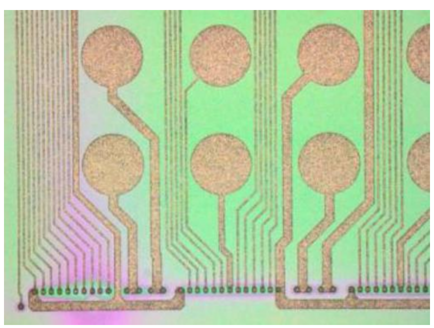
I_{leak} < 1 E^{-06}A

D. Henry, LETI

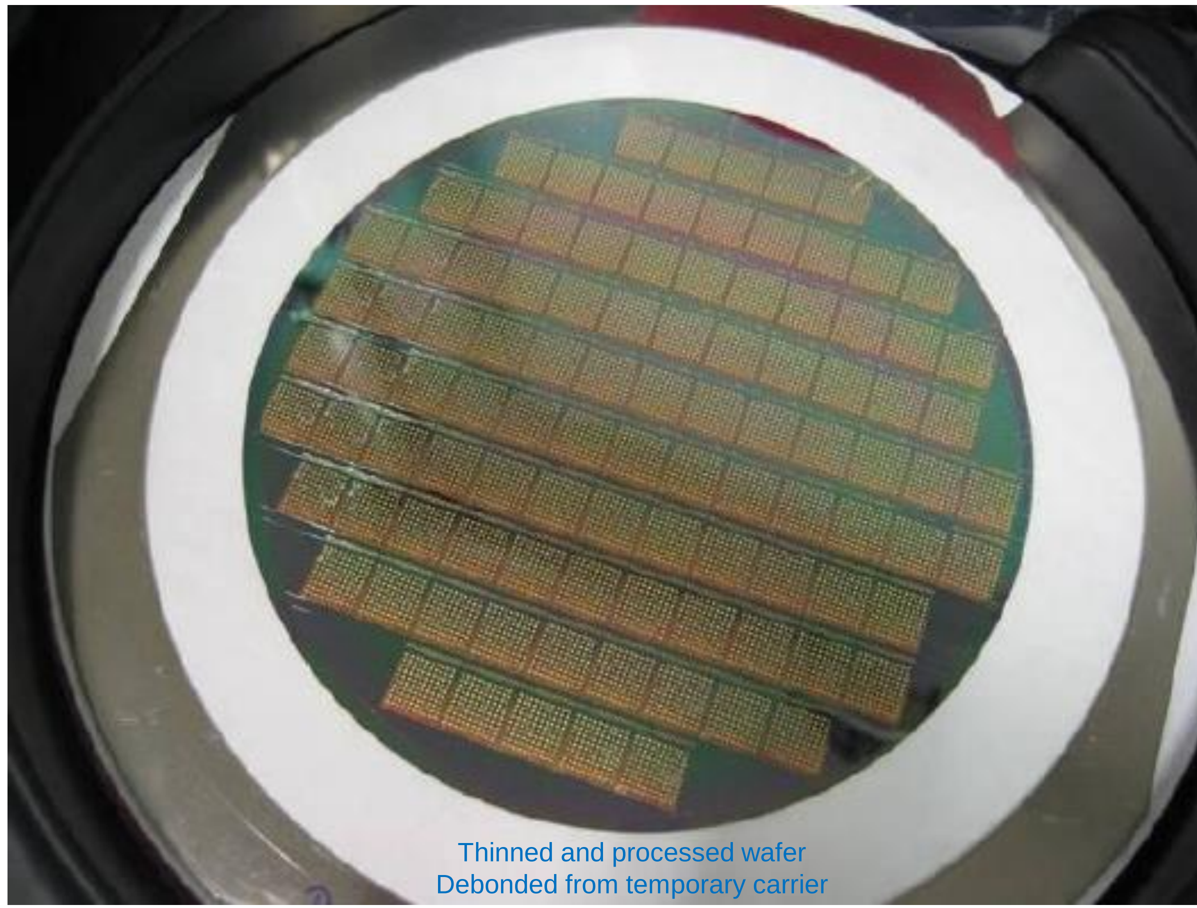
Images of a fully processed wafer



Through Silicon Vias diameter 60 µm
Wafer thinned to 110-120 µm



Redistribution layer
Back side of Medipix3 chip

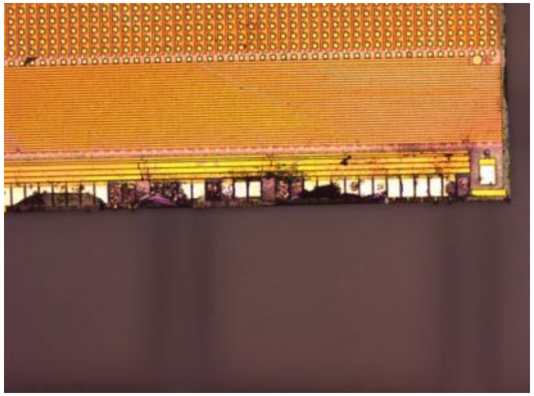


Thinned and processed wafer
Debonded from temporary carrier

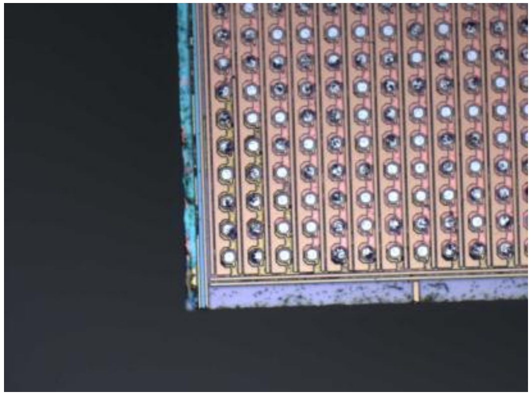
Images courtesy of CEA LETI

Dicing/chip pickup issues

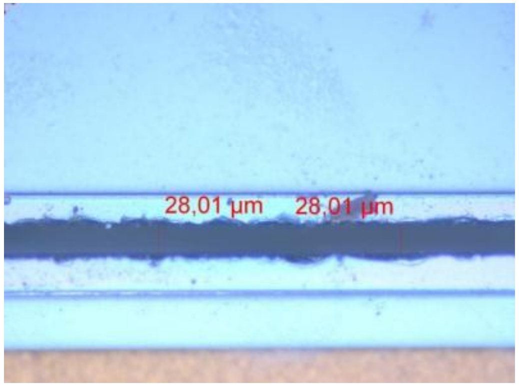
- **Chips Dicing & boxes packaging**
  - First delivered wafers :
    - Metal delaminations on front side
    - High chipping on the edges
    - Chips breaking during pick out process
    - Tape residues on pixel side



High chipping + pad delamination



Tape residues



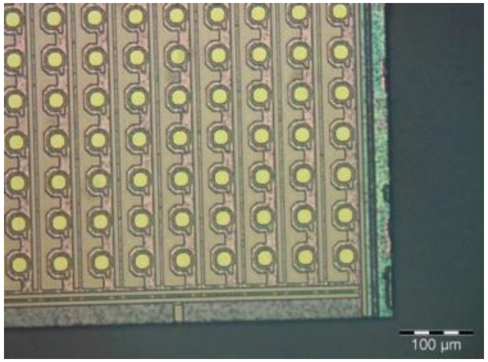
Backside chipping

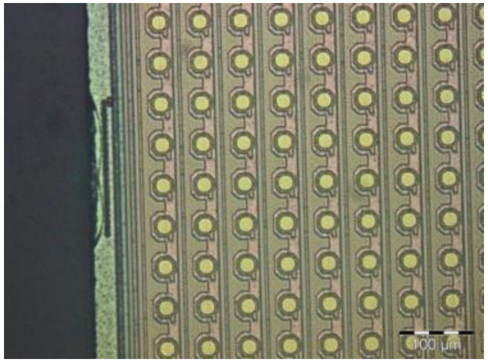
- **Need to develop an optimized dicing process :**
  - DISCO collaboration

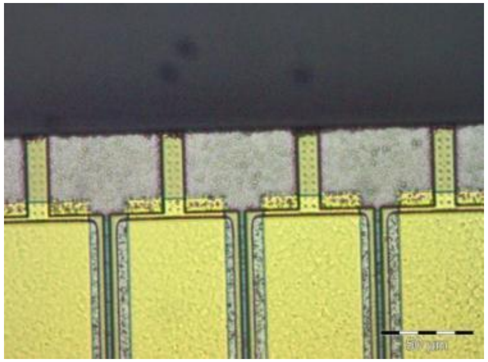
Dicing/chip pickup issues

- **Dicing trials on DISCO plant (Munchen)**
  - Taping of BGA side on the tape
  - UV tape
  - Fine blade
  - High Blade rotation
  - Low Blade speed

- **Pixel side observations**
  - Chip I4



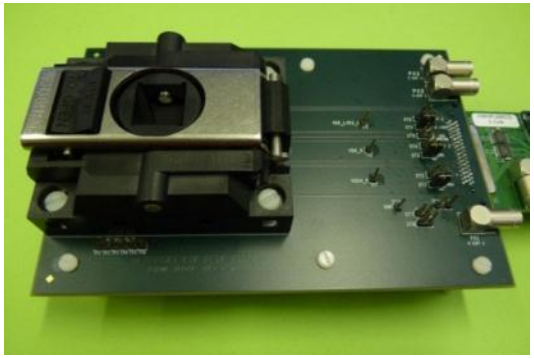




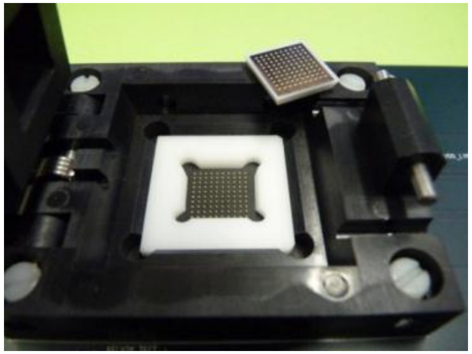
  - Lower chipping compare to previous dicing

Test setup

- Test set-up :
  - Test board realize the interface between Medipix3 chip and readout interface
  - Test socket is embedded on test board to establish contact to the bga pads of the chip
  - We are using a custom readout interface (USB) common to most of MEDIPIX chip family



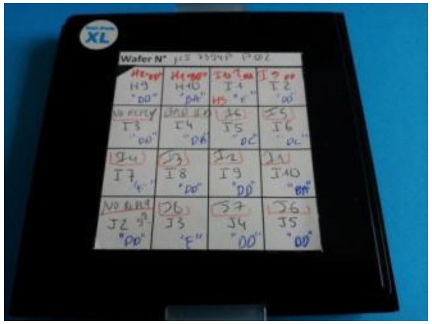
Test board



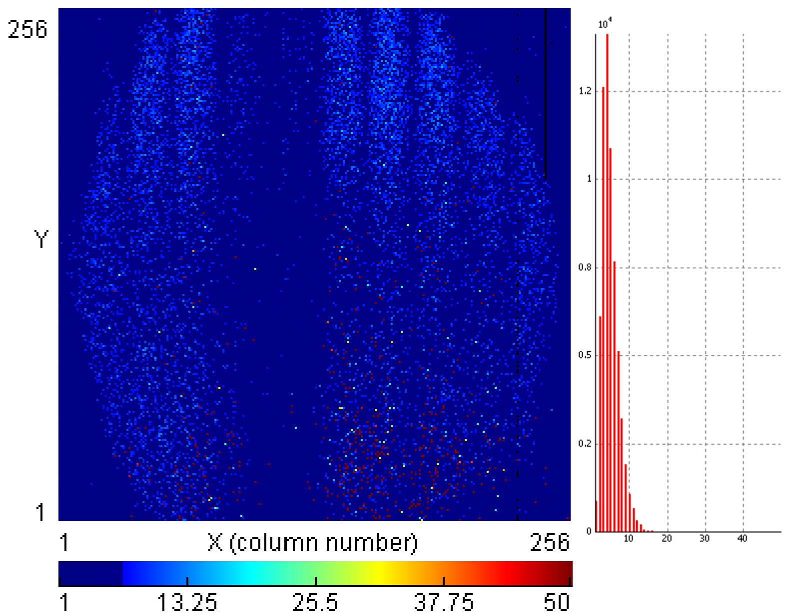
Test socket

Readout interface

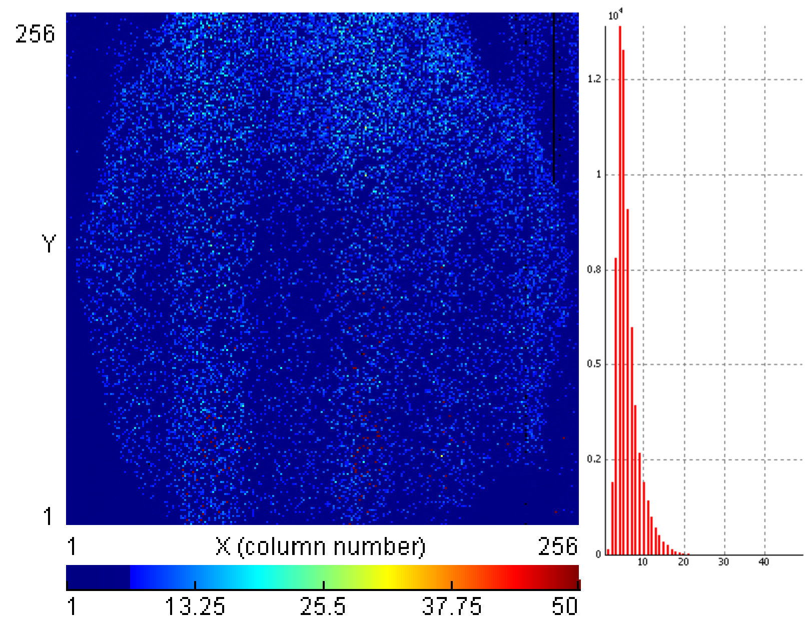
- Test samples
  - LETI sent a complete GELPAK of 16 diced chips. (DISCO dicing)
  - Parts are from IBM wafer # AZNW5VH, at CERN it was identified as Wafer # 24



Noise floor comparison



Before TSV

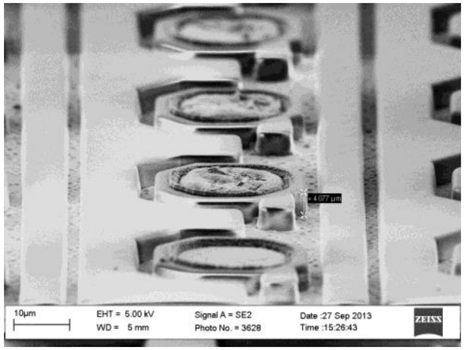


After TSV

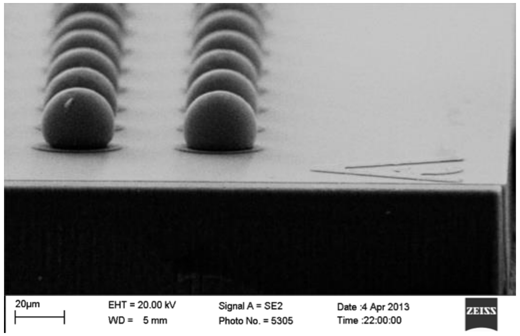
- We could notice only a slight difference

Images of fist assemblies

- One TSV processed wafer was sent to ADVACAM company for :
- Dicing of thinned wafer and selection of “good” chip candidates
- Sn-Pb solder spheres were processed on Edgeless Sensor
- TSV processed wafer already provided with Under Bump Metallurgy on both pixel side and redistribution layer
- μ-Solder bump interconnections. Successfully done

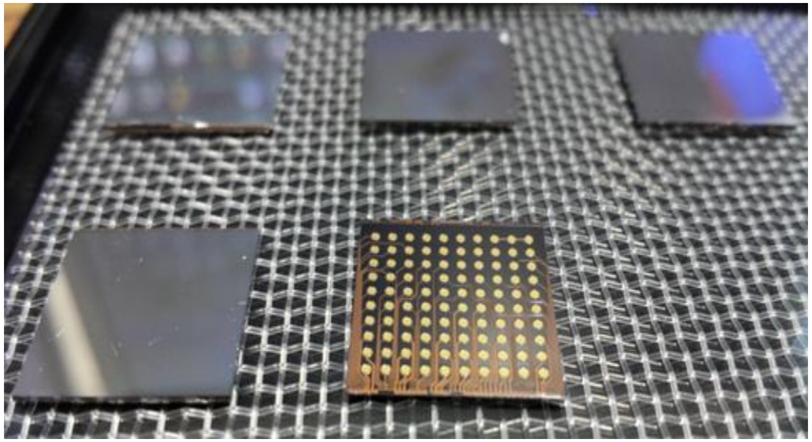


Pixel pad on ROC
(after debonding of previous trials)



Sensor with Sn-Pb solder bumps
After reflow process

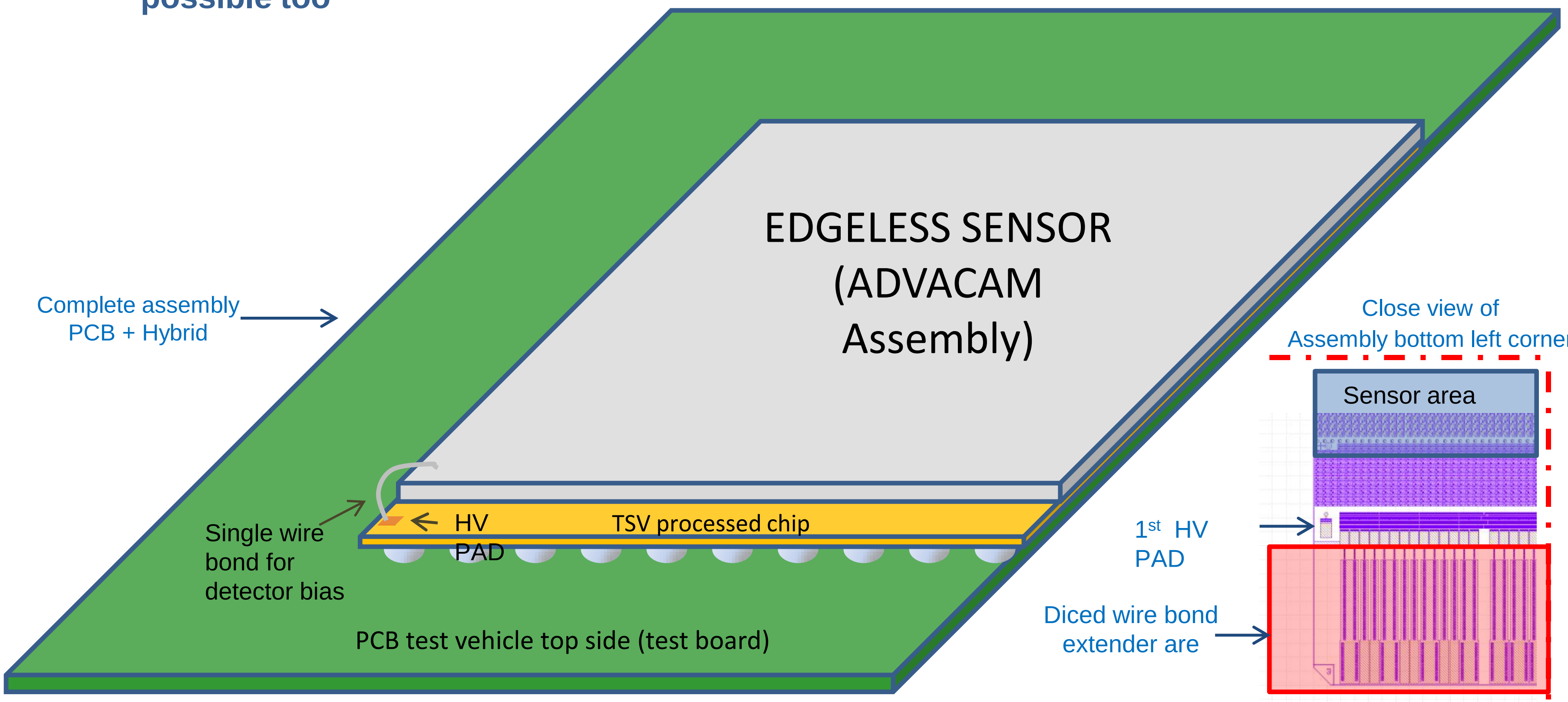
SEM images courtesy of Advacam



First Edgeless-TSV assembly
5 were provided to CERN in October 2013

Mounting on a test board

- A test board without the test socket could be used - footprint matching redistribution layer BGA footprint.
- A single wire bonding interconnect is needed for bias between ROC HV pad connected through TSV to PCB and top of the sensor. Others path for sensor bias are possible too

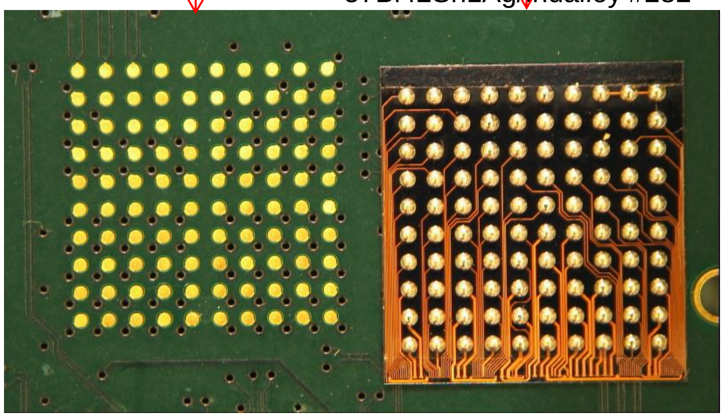


Mounting on a test board

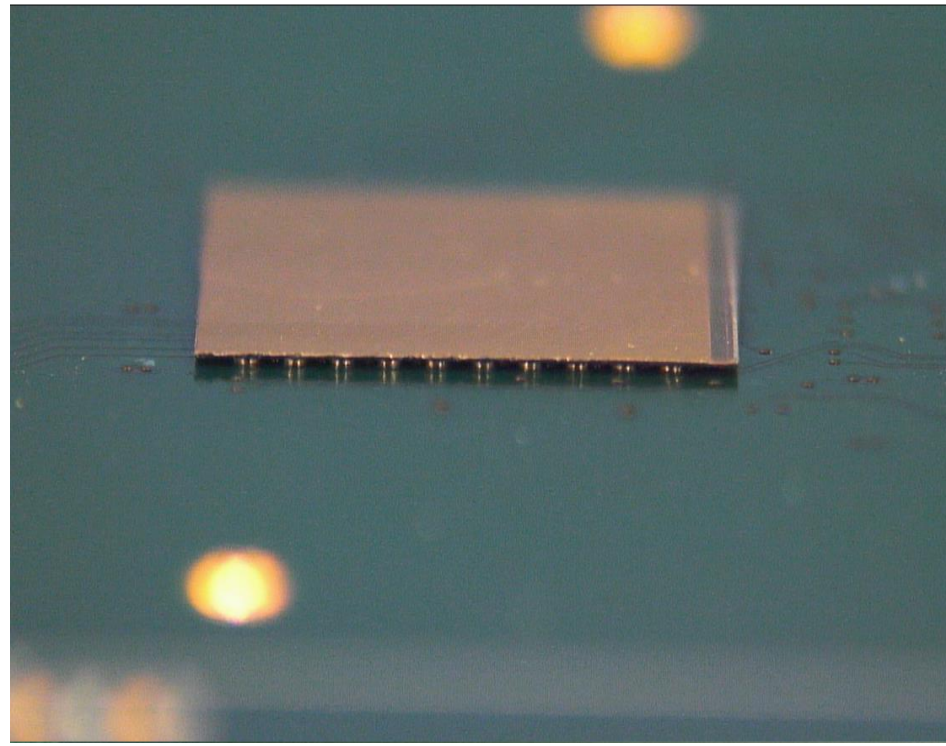
- **BGA pads on the redistribution layer (back side of the chip) have been prepared with low temperature solder spheres**

PCB BGA footprint

Bare chip with solder spheres 57Bi42Sn1Ag/Indalloy #282



First trial with a bare Medipix 3.1 chip

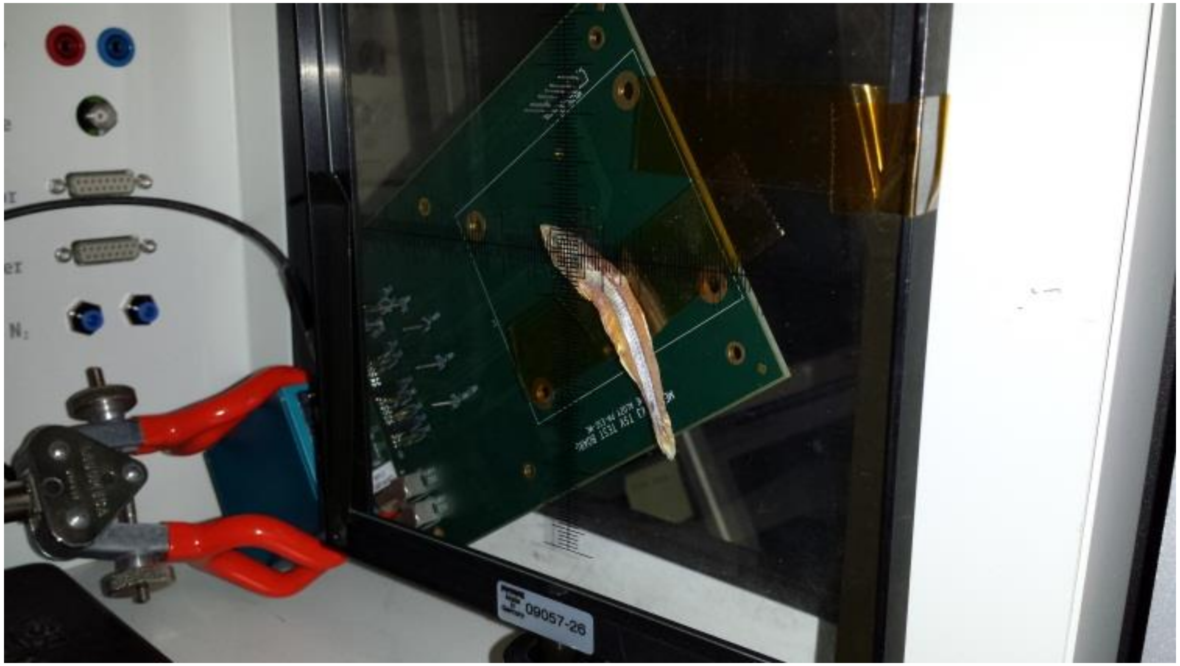


Courtesy of S. Kaufmann

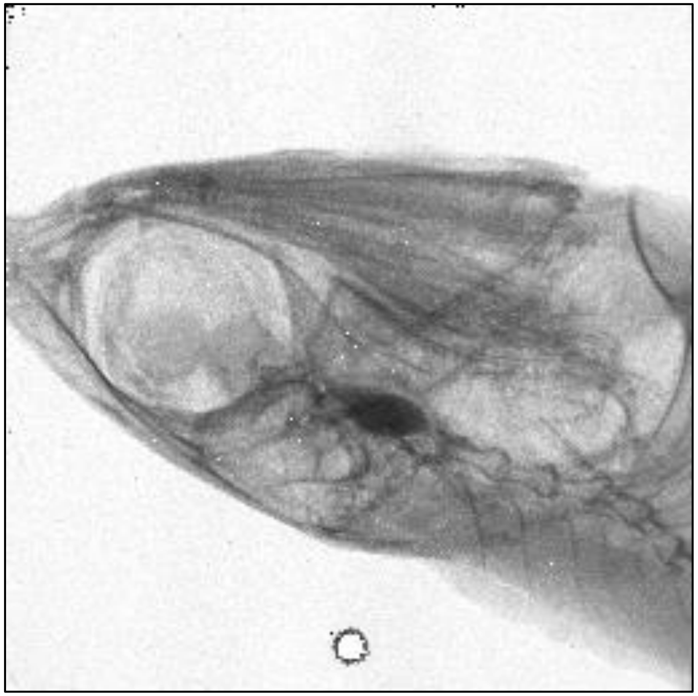
100 solder spheres of 0.635mm (after first reflow to attach them)

Imaging test setup

- X-Ray chamber 35kV, 1mA
- Hybrid Pixel Detector was positioned in front of the X-Ray beam
- A biological sample (fish) placed before the detector



First image with TSV processed hybrid Medipix3



First image obtained with a TSV processed hybrid pixel detector (flat field corrected)

The sensor bias current was high when applied through TSV (tens of μA in full depletion voltage region)

Without sensor bias wire bonding via the TSV it was clearly better (few μA)

The quality of the ADVACAM assemblies is good. Unfortunately assemblies have not been tested before mounting so we cannot yet quantify the impact of chip-on-board integration

Project status and future work

The feasibility of TSV-last processing on Medipix3 chips has been demonstrated.

The process is compatible with bump bonding to edgeless sensors.

A 2nd lot of 6 wafers (this time Medpix3RX) has been launched with the aim of demonstrating reasonable yield

A new lot aimed at producing ultra-thin Si assemblies using the Timepix3 chip has just been ordered.