65nm IP block with a rad-hard DICE SRAM

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Radiation effects on MOS transistors

Cumulative effects

Effects due to long-time exposure to radiation:

- **Total Ionizing Dose (TID)** effects due to electron-hole pairs generated in the oxide layer: the holes remain in the oxide for a long time and channel carriers can be trapped at the Si-SiO_2 interface
  - **Consequences**: threshold voltage shift and parasitic currents increase for thick silicon oxide
- **Displacement Damage Dose (DDD)** effects due to collisions with neutral particles that may create vacancies into the silicon lattice
  - **Consequences**: mobility degradation

Single Event Effects (SEEs)

The interaction with a single particle generates electron-hole pairs in the silicon; in a region crossed by an electric field (reverse-biased junction) a parasitic current can be observed:

- **Soft errors** are non-destructive and temporarily effects (e.g., bit upset)
- **Hard errors** are destructive (e.g., gate rupture)

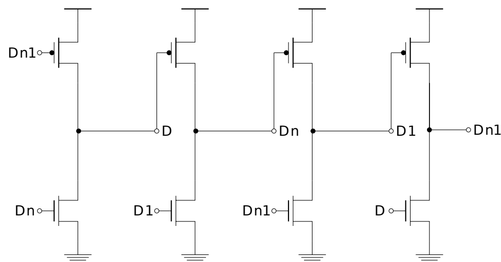
Radiation effect in modern CMOS technologies

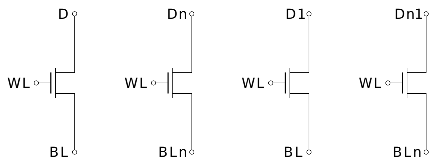
- Some papers demonstrate that 65 nm CMOS can resist to a dose of 200 Mrad
- SEE increases due to a decrease of critical charge

Our goal

Enhance the SEE radiation hardness with Radiation Hard By Design (RHBD) techniques

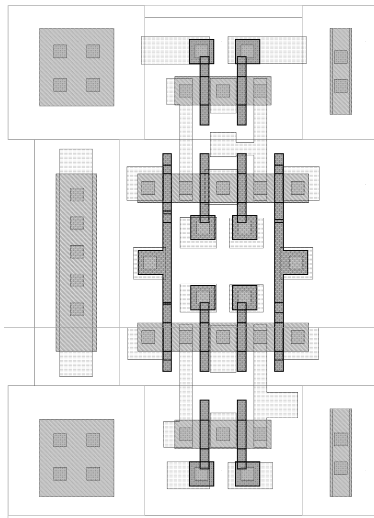
DICE cell schematic





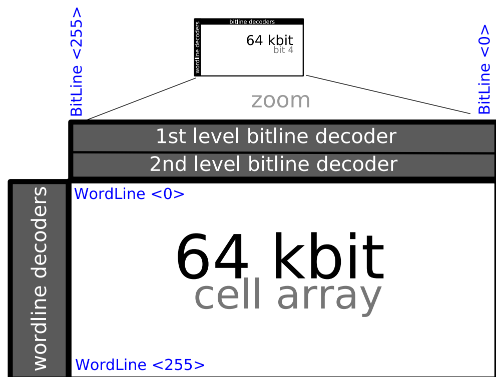
12 MOS transistors: 4 PMOS and 8 NMOS

DICE cell layout

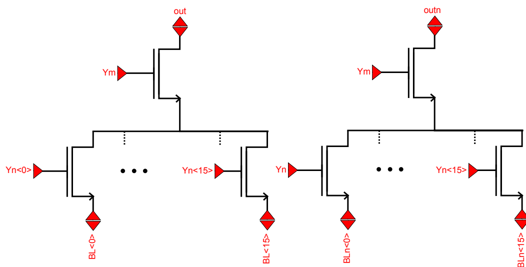


cell size: 1.84 μm $\times$ 3.27 μm

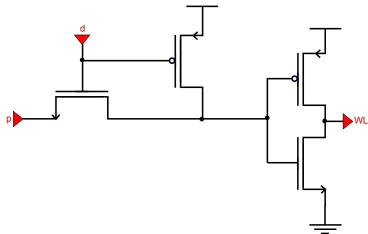
SRAM architecture



SRAM decoders

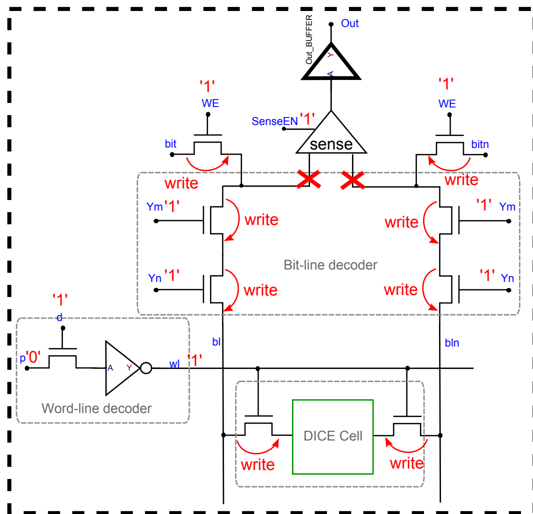


Bitline decoder

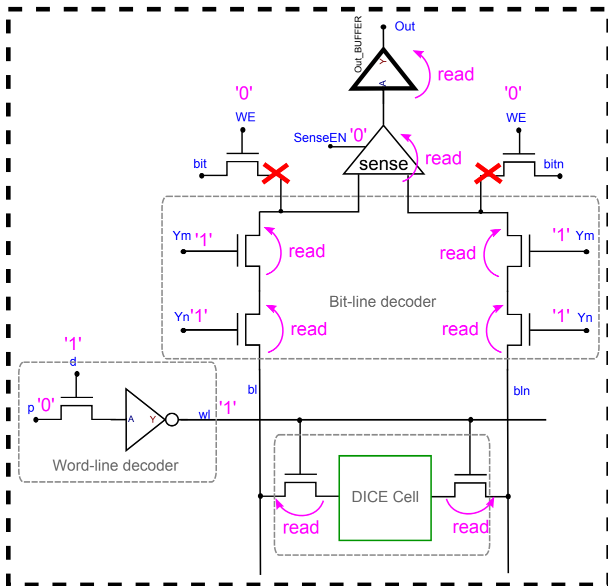


Wordline decoder

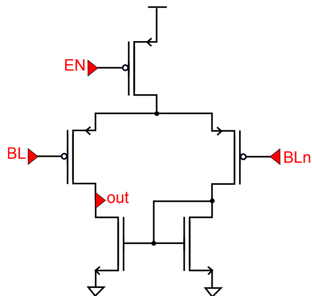
Write mode



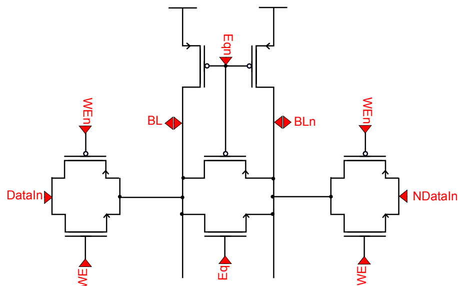
Read mode



Control circuitry

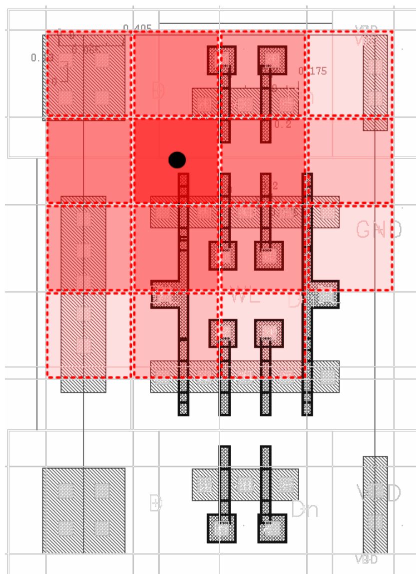


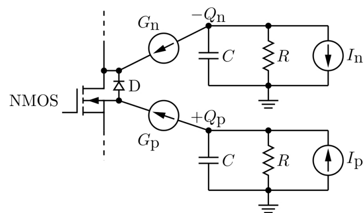
Sense circuit



Equalizer circuit

Fault injection technique for spectre simulation

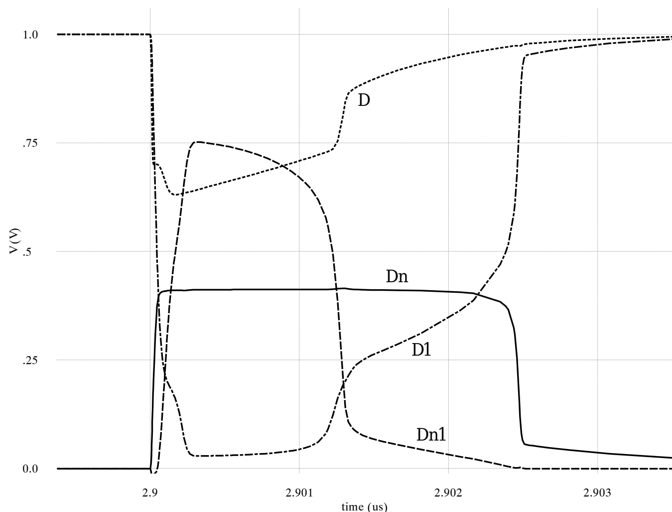




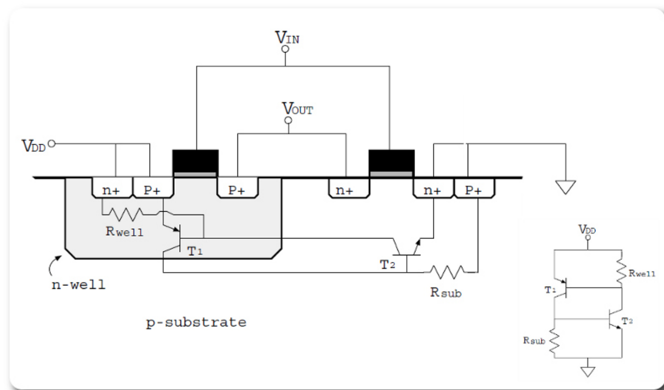
Charge are split in different boxes with different values

For each node, charge calculation depend on the pn junction capacitances

Simulation results

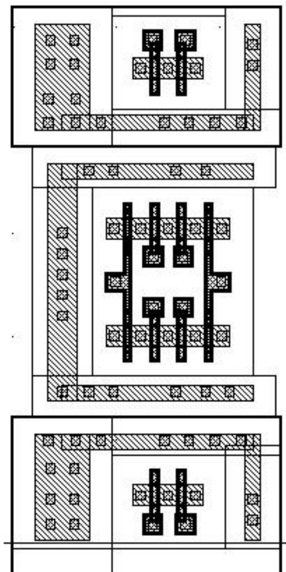


Latch-up at high temperatures (> 80 °C)



Feed-back loop gain with 1 V supply voltage in ambient temperature is less than 1, but it can be higher than 1 at high temperature – greater than 80 °C

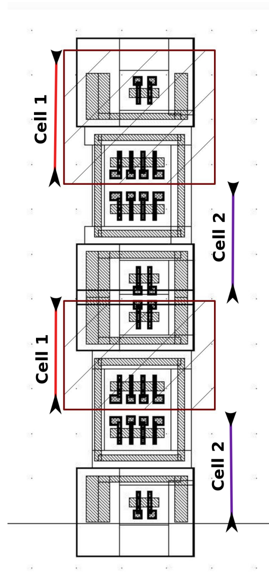
Second version of the DICE cell



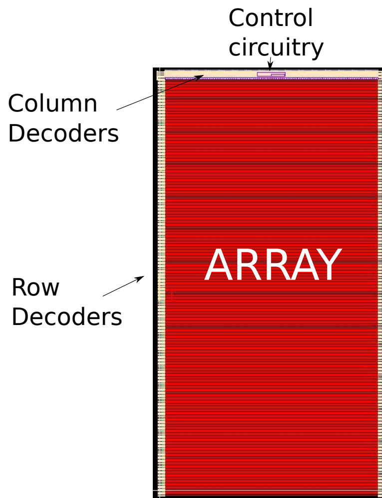
cell size: 1.84 μm $\times$ 5 μm

Third version of the DICE cell

- Inter-leaved DICE cells: first half of DICE1, first half of DICE2, second half of DICE1, second half of DICE2
- Separation between the two halves of the same DICE: 5 μm
- Same area as version 2 (only routing complexity increases)



IP block



Conclusions and future improvements

- The complete block of first DICE cell (not inter-leaved) has been designed in 2013
- Others two versions of DICE cell blocks will be completed in next month
- The whole SRAM blocks have been simulated with fault injection method and with the corner analysis
- The blocks are going to be fabricated at June of 2014 and they will be tested under radiations