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Status of the 3DIC project

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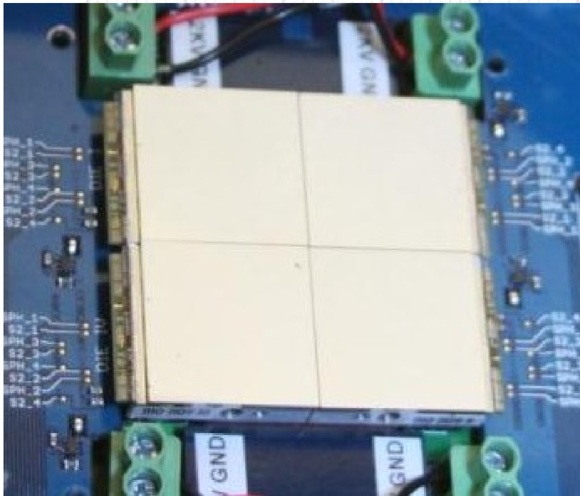
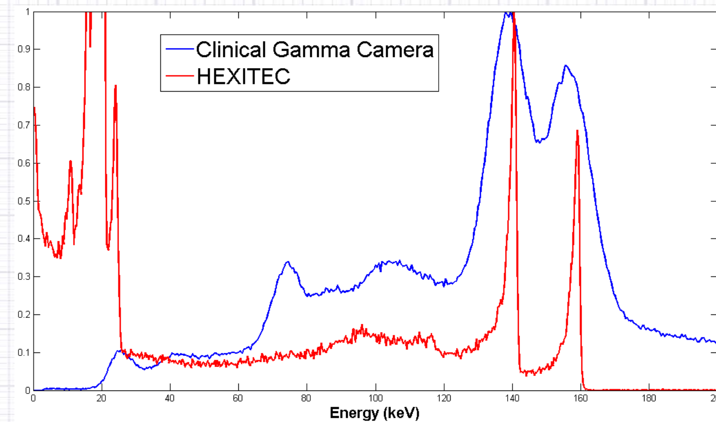
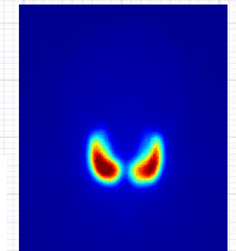
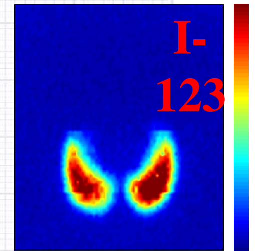
Background

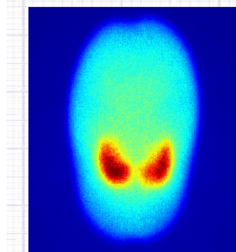
- Demonstrate that 2-tier 3D pixeldetector readout ASIC with vias in every pixels can be done “via last”
  - Analogue tier based on proven Hexitec platform

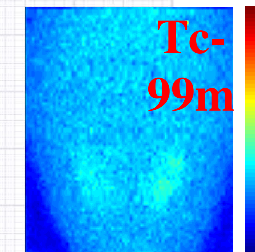












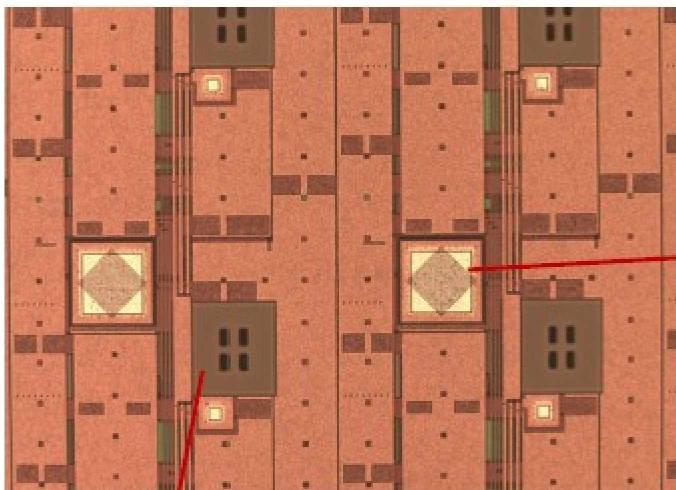
  - Digital tier contains a 12bit (10bit) digitizer in every pixel and readout.

Specifications

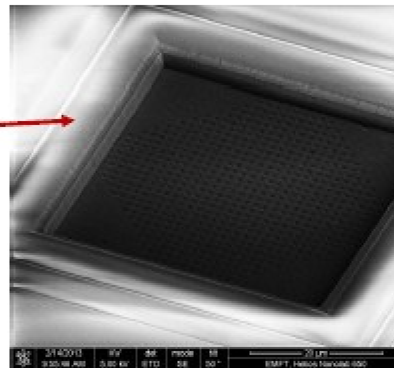
- Technology ASIC: AMS 0.35 μm
- 40x40 pixels
- Effective pixel pitch 250x250 μm
- 4-side buttability
- Digitization modes 12 and 10 bits
- Output of “hit-pixel”
- Each pixel should be able to handle 2 hits/readout (~deadtimeless operation)

Progress

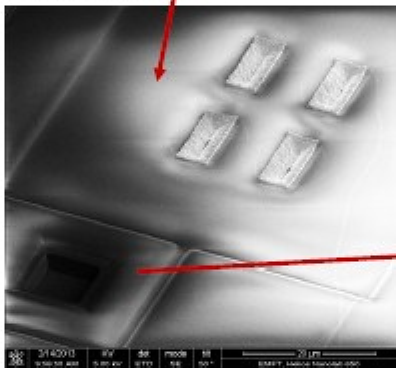
- 12 wafers containing both tiers produced, tested and shown to be well functioning. (pre-AIDA)
- In 2011 EMFT were contracted to thin the “Analogue” wafers
- In 2012 EMFT were contracted to finish the SLID bonding (there was an unfortunate long delay between these two steps because of contract issues)
- The first SLID parts were delivered in Mid 2013 (rather than end 2012)
- The first full wafer of SLID parts were delivered in Oct 2013

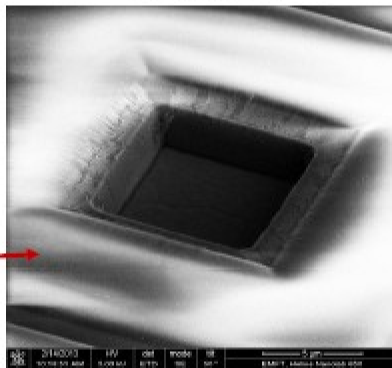


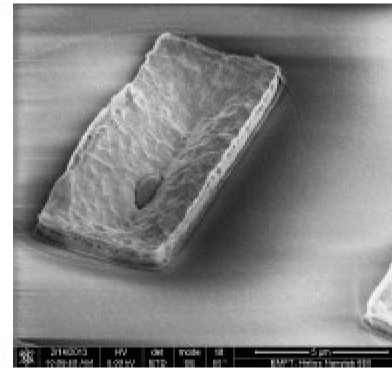
- View of pad and in-chip areas after tungsten etch and oxide opening to device pads;
- Resist is still on top of oxide



- Oxide on device pads is removed





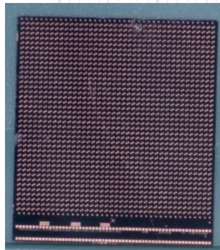


Division Nanomaterials,
Devices and Si Processing – NDS

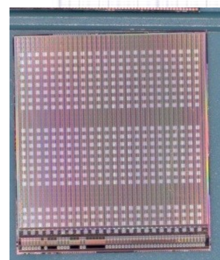
Armin Klumpp
Device and 3D-Integration

Deliverables (& lessons learned)

- TSV processing and contact metalization went generally OK
- Excessive stress induced in the thinning process (to 50 μm) and this had to be modified to stop the wafers cracking
- Back side metalization critical and is one of the main worries.
- EMFT have now delivered a wafer of SLID bonded ASICs and some non-bonded parts
  - 9 proper devices (thin top analogue to thick digital) on the wafer that are properly SLID bonded together
  - 10 thin top digital bonded to thick analogue. The SLID bonds are not functionally and the devices have a non-functional checker-board Al pattern on top surface. These do have good wire bond pads so can be connected to test boards.
  - 5 thin analogue and 5 thin digital ASICs. One analogue AISC went for stress imaging at ANKA.



Analogue (top)



Digital (bottom)

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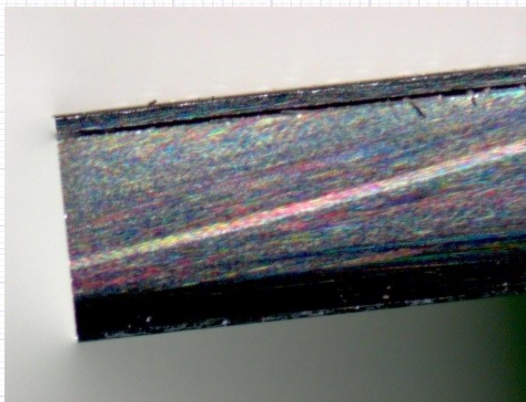
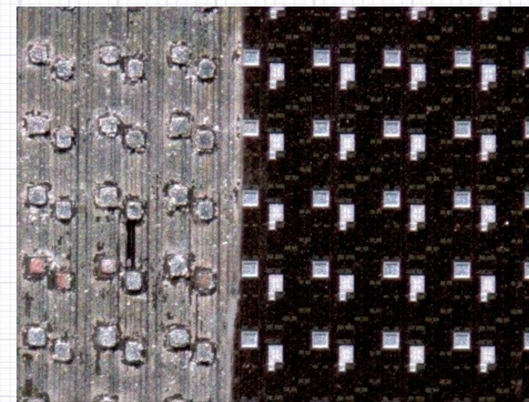
Cont.

The full SLID wafer is visibly very poorly bonded (Fig 2) and we do not expect any good devices but there could be valuable indications by using the new system. We have used some ASICs from the wafer but there were only 6 devices worth taking from the wafer.

Analogue SLID

Digital





Digital (bottom)

Analogue (top)

EMFT agree, that the device SLID looks very poor and there will be very poor yield. 3DIC is still strategically important for them and they have committed to continue the development. They agreed to reprocess devices Free Of Charge if we can provide more wafers.

Plans (AIDA year 4)

- Testing of already delivered devices started and will continue with a PhD student who begin testing at RAL and continue in Uppsala.
- 12 new wafer purchased and delivered to EMFT for processing
- EMFT processing plans (intend to split your 12 wafers into 4 bottom wafers and 8 top wafers):
  - M1: Top wafers thinned on handling substrate by 30.05.14
  - M2: Electroplated copper structures on thinned-Top back side by 13.06.14
  - M3: Electroplated copper/tin structures on bottom wafer by 05.05.14
  - M4: Assembled Top on Bottom by 27.06.14