WP microelectronics and interconnections

- Goal : provide chips and interconnections to the other WPs

- Task 1 : 65 nm chips for trackers (CERN?)
  - Fine pitch, low power, advanced digital processing
- Taks 2 : SiGe 180nm for calorimeters/gaseous (IN2p3)
  - Highly integrated charge and time measurement
- Taks 3 : interconnections between different technologies (INFN)
  - 20 µm TSVs for pixels, TSV post-processing of tasks 1&2, chip to wafer bonding

- The goal of the workpackage is to provide innovative readout chips for the detectors in the other workpackages. It would therefore select a few technologies and provide runs both for R&D designs that advance the state of the art (in speed, low noise, integration...) and also include more mature chips that can be used to advance the detector designs and in particular allow "smart detectors" or highly integrated detectors. This latter goal also includes the interconnection aspects, again both in R&D and applied to detectors. It is thus split into 3 tasks which provide deliverables.

Task 1 : micro electronics for trackers.

- The community is focusing a large fraction of the design work on the 65nm CMOS technology.
- Presently, this mostly addresses mixed-signal integrated circuits for pixel detector readout, but it is likely to extend to more diverse applications.
- For CMOS sensors, purely digital chips (or with a dedicated analog section) may be needed for the readout of a pixel matrix.
- Taking advantage of the growing expertise in 65 nm CMOS, detectors other than silicon ones are also interested in using this technology for new chips.
- The Task will offer 1 or 2 runs in 65 nm, where design know-how and common circuit blocks can be shared in different chips in a collaborative way by the community of IC designers.

Task 2 : micro electronics for calorimeters and gaseous detectors.

- The Task will provide 1 or 2 runs in large dynamic range, low power, high speed technology, such as SiGe 180nm or SOI 130nm.
- The circuits will provide multi-channel readout of charge and time to the accuracy required by these detectors. in particular, the timing properties to the few ten picoseconds level will be explored.

Task 3 : interconnections

- for Task 1 and Task 2, addressing 20um TSVs for pixel sensors and interconnections between different technologies (analog/digital or sensor/chip).
- There is a strong interest for achieving a high-density, reliable and cost-effective interconnection between a readout chip and a sensor, and/or between analog and digital electronic layers.
- This Task will work with industrial partners to qualify interconnection processes with high-density 3D integration features such as small-pitch TSVs and wafer-to-wafer or chip-to-wafer bonding pads. 3D processes will be selected on the basis of specifications that serve the community needs at best.
- The Task will also organize TSV post-processing and other 3D-related technological steps on the CMOS wafers that will be fabricated in the common runs by Task 1 and Task 2. In this way, chips for diverse applications may have access to wafer-level 3D technology in a prototyping stage.

WP partners

- We need one group for organizing the MPWs and paying for the runs, could be CERN for Task 1, IN2P3 for Task 2 and INFN for Task 3.
- Then, the runs are open for participants, we however have to find a way to limit the number of fuzzy designs, either by requesting a financial participation or by selecting at the entrance the partners.
- In the preparation stage of the AIDA-2 proposal, we will ask the community to submit projects for joining the three Tasks. Projects will be admitted to this Workpackage on the basis of their scientific merit (according to the needs of the community) and of their financial contribution to the Workpackage.
- A project may pay its fraction of the costs for a 65 nm prototype run, and ask for support for TSV processing in the wafers.