



3rd ANNUAL AIDA MEETING
WP9.5 FEE status

OMEGA, 26/03/2014

OMEGA microelectronics group

Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

MILESTONES and SCHEDULE



2011-2012: Characterization of the 2nd generation ROC Chips

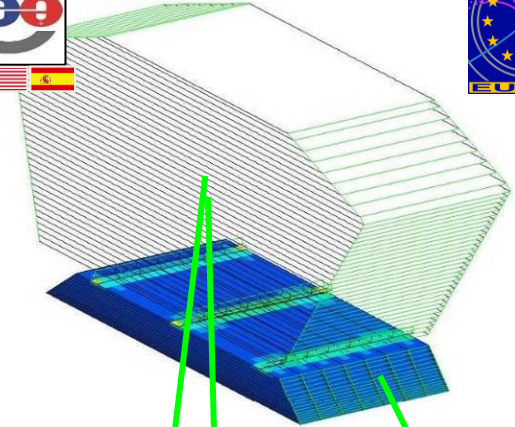
- Dedicated run produced in March 2010
 - 25 wafers received in June
 - 20 000 chips packaged in the US

2013: AIDA Milestone = Submission and test of one of the 3rd generation chips (hradroc3)

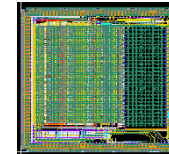
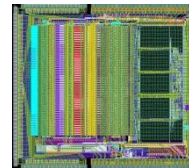
- Report submitted in August 2013

End of 2014: Engineering run

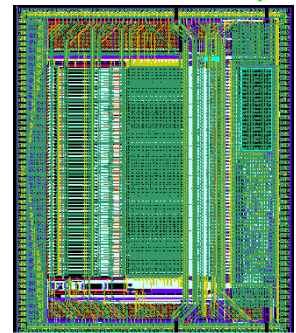
- Budget for 3rd generation of electronics:
 - 81k€ (40k spent so far)
 - 30 ppm (19 ppm used so far)
- Cost:
 - Multi Project runs (MPW): 1k€/mm²
 - Packaging: \$3500
 - Testboard: 1500 €



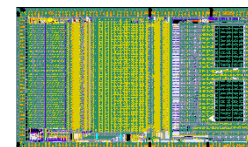
HARDROC2/MICROROC
SDHCAL RPC/ μ MEGAS
64 ch 20 mm²



SKIROC2
ECAL Si
64 ch. 65 mm²



SPIROC2
AHCAL SiPM
36 ch 32 mm²

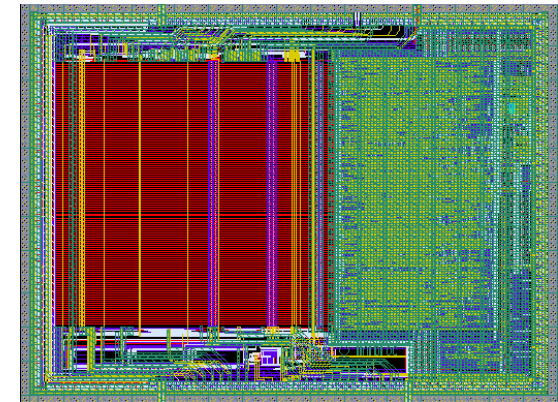


0.35 μ m SiGe AMS technology

❑ 3rd generation chip for ILD

❑ Independent channels (zero suppress)

❑ I2C link (@IPNL) for Slow Control parameters and **triple voting**

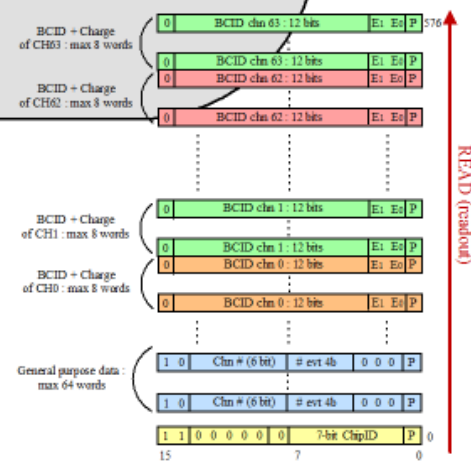
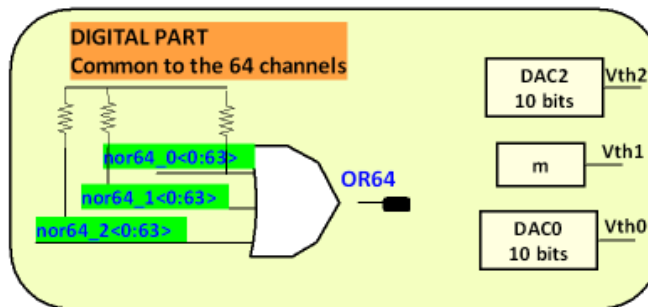
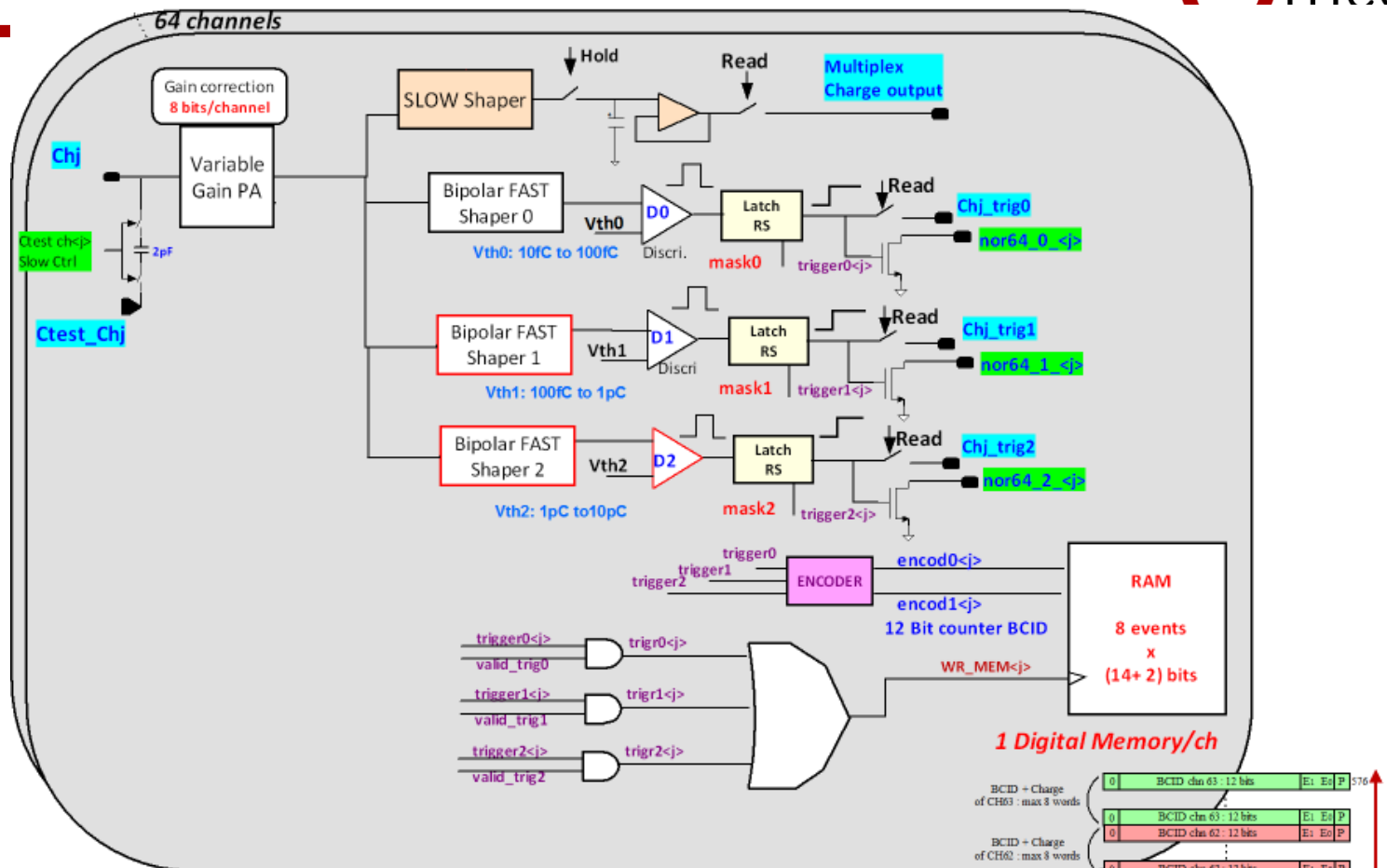


❑ HARDROC3: 1st of the 3rd generation chip to be submitted

- analog part: extension of the dynamic
- Complex digital part to handle the channels independently
- Submitted in Feb 2013 (SiGe 0.35 μ m), funded by AIDA, received end of June 2013
- Die size $\sim 30 \text{ mm}^2$ (6.3 x 4.7 mm²)
- Packaged in a QFP208
- HR3: tests at system level should be performed on 2-3m chambers



SIMPLIFIED SCHEMATICS

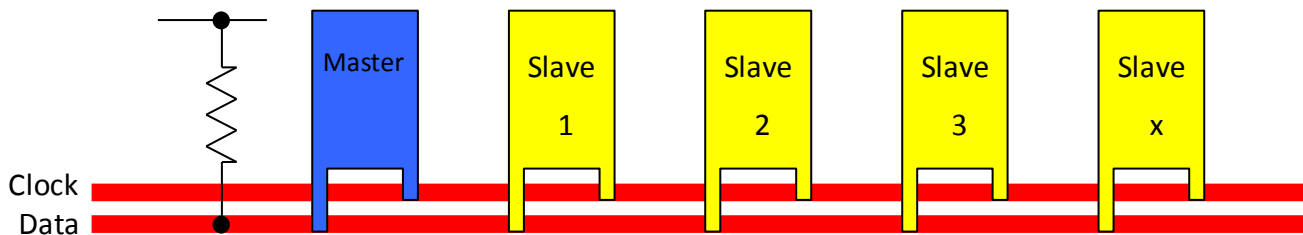


Slow Control

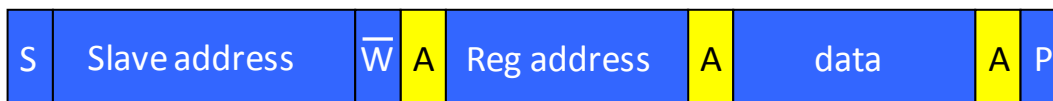
- Slow control common features:
 - Triple voting
 - Read back of control bit (also when chip running)

} Test OK

- Slow control access:
 - Classical shift register → Test OK
 - I2C serial link → See below



Write frame:



Read frame:



Pb: Data stuck to 0 inside the chip

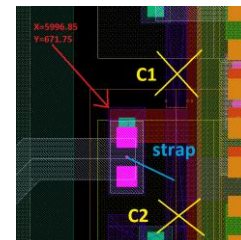
Due to a buffer added by OMEGA to output the data

⇒ Chip modification (Focused Ion Beam) necessary to test the I2C link

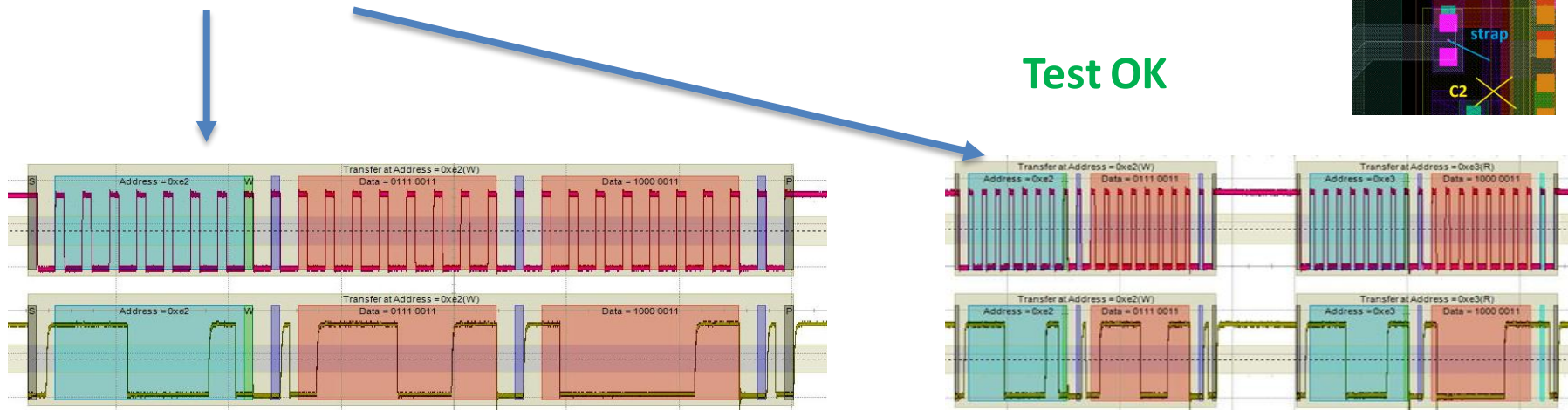
I2C Tests on FIB chips

“Complete” FIB (2 cuts + 1 strap) to bypass buffer on board HR3_01:

⇒ Write and Read access with Chip ID: 0xE2 / Reg @: 0x73 / WrData: 0x83



Test OK



Simplified FIB (1 cut) to isolate buffer HR3_03:

Test OK

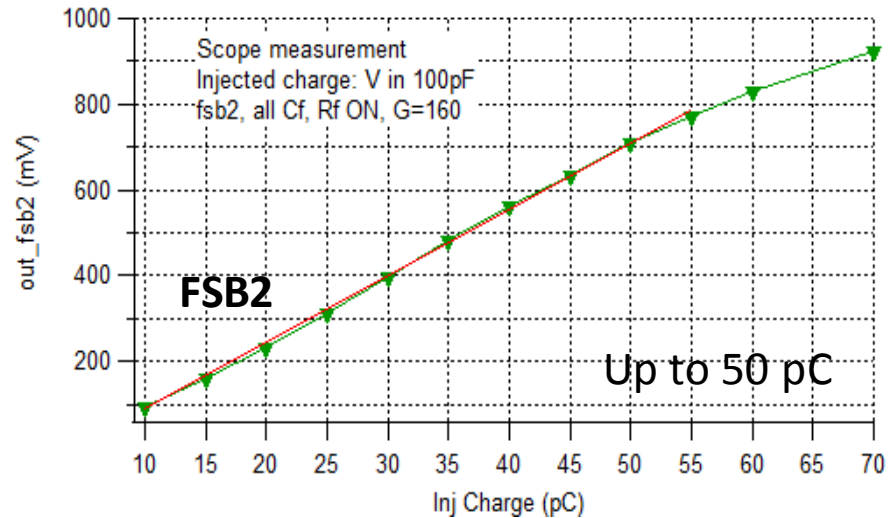
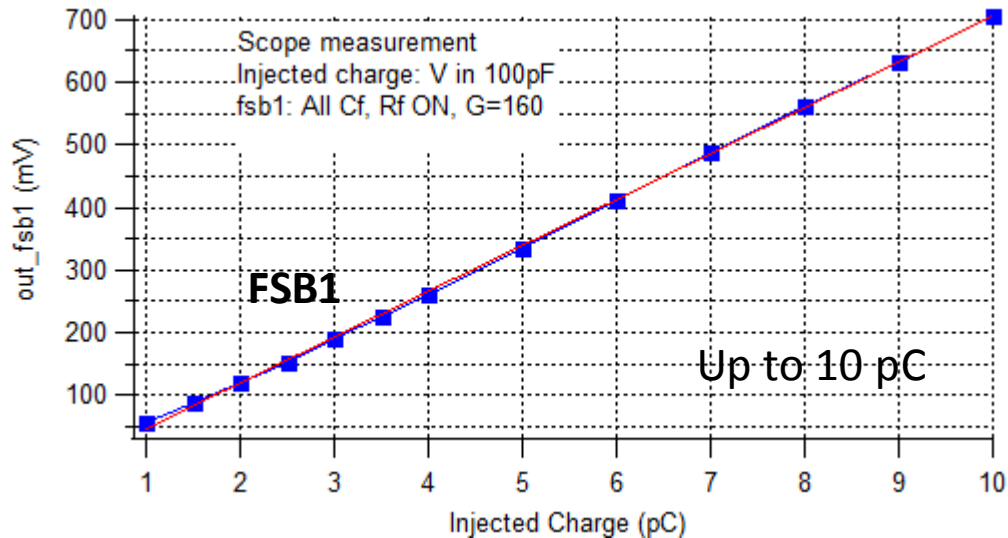
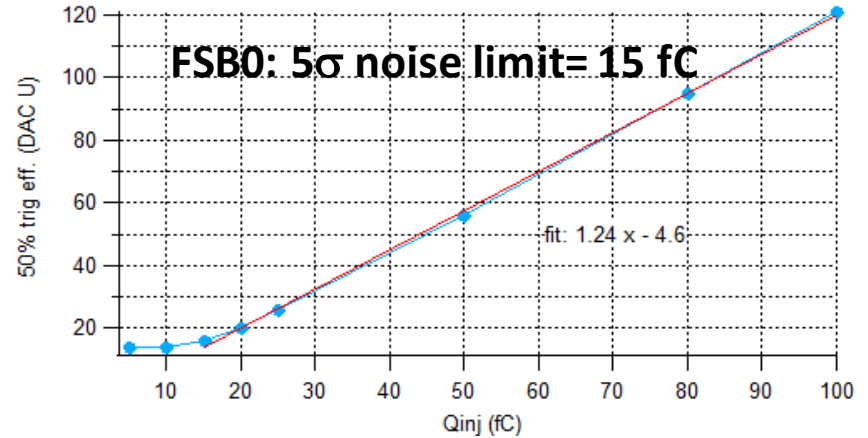
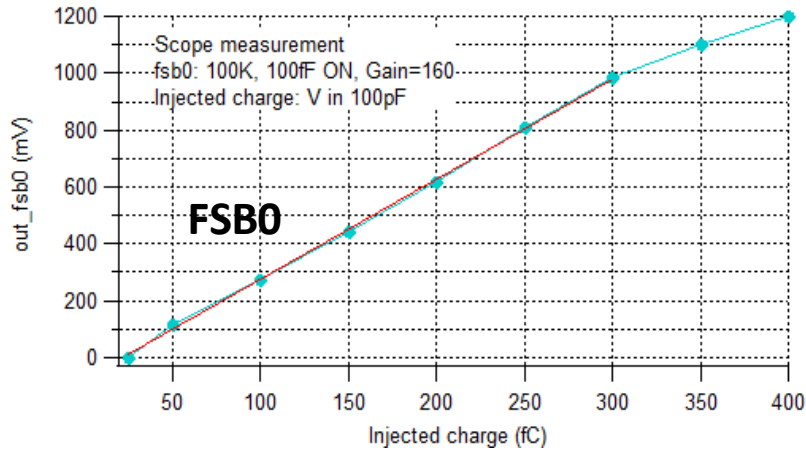
⇒ Only Write access possible (no acknowledge)



Other I2C tests:

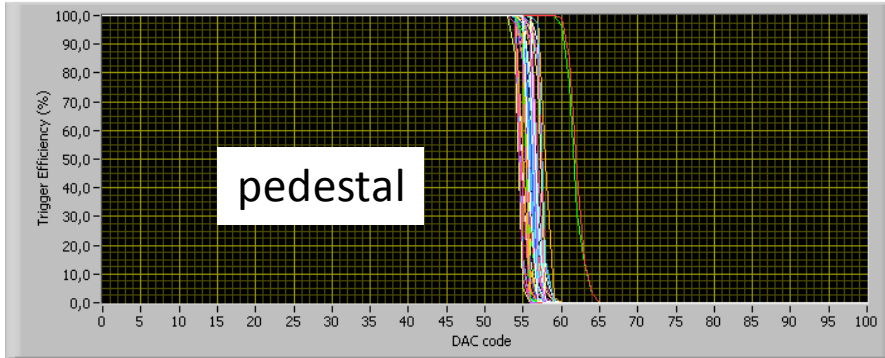
- ⇒ Tests @ High/Low temperature
- ⇒ I2C @ 400Khz with 500pF on Bidir data port

Analog Part: FSB Linearity

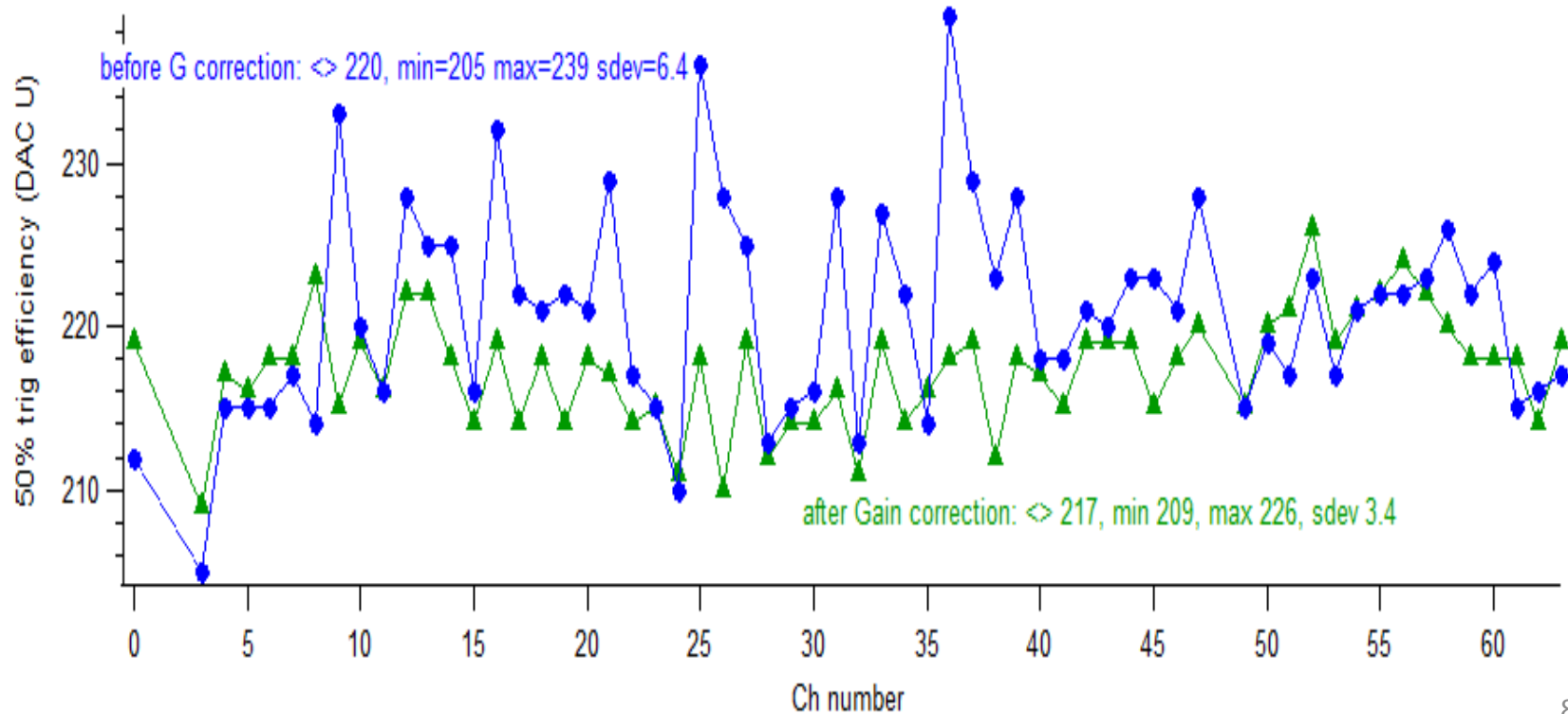
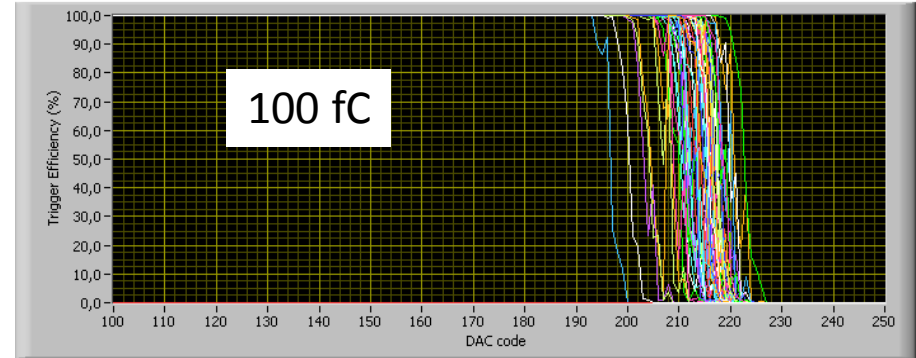


SCURVE measurements

Test S-Curve vs Threshold (all ch.)



Test S-Curve vs Threshold (all ch.)

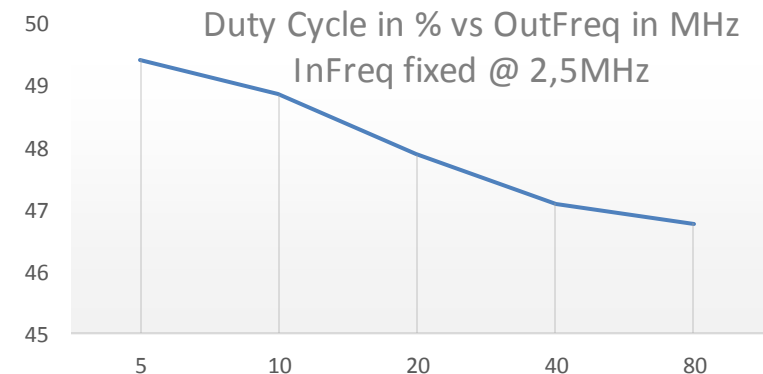
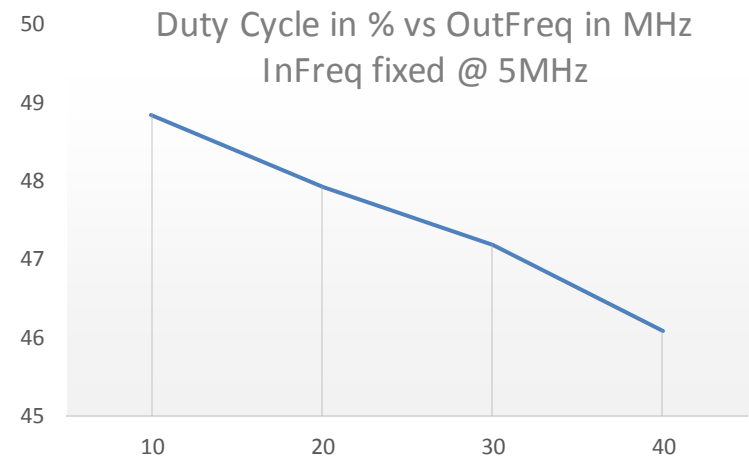
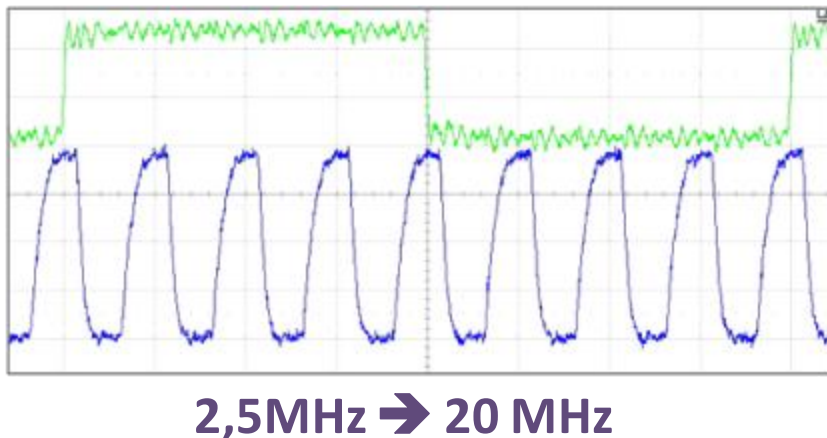


PLL measurements

PLL can generate fast clock internally (40 MHz):

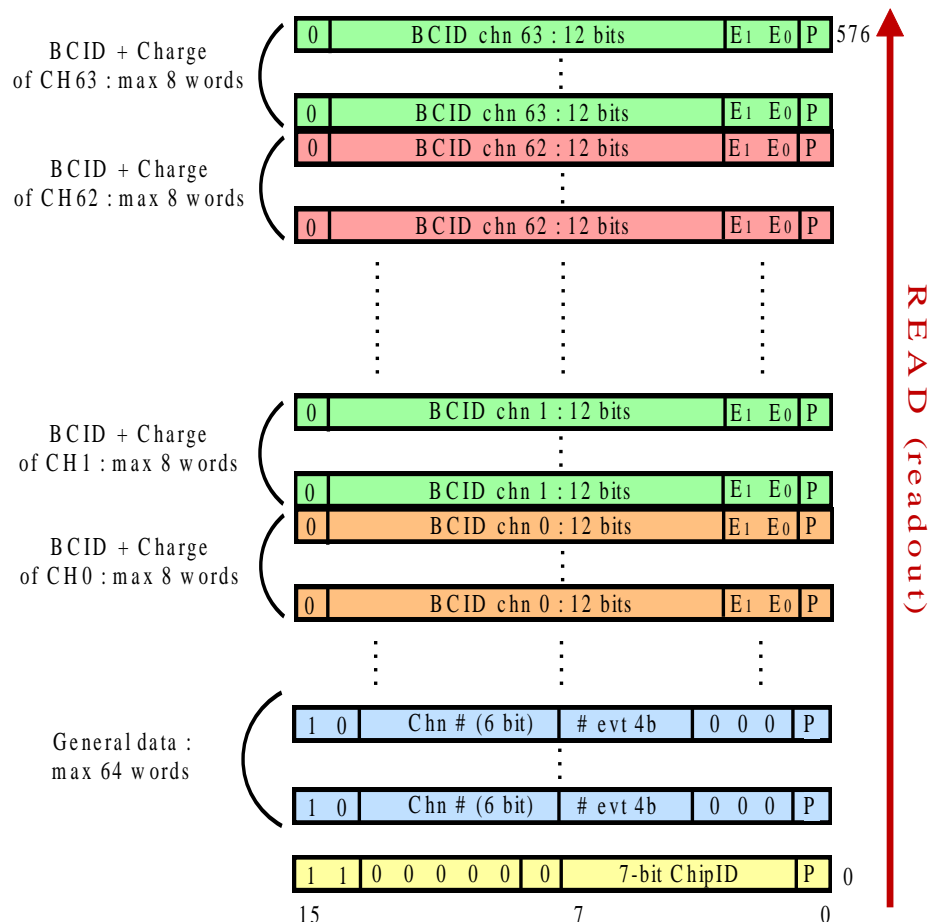
- ⇒ Multiplication factor is $(N+1)$ / N is a SC parameter (1 to 31)
- ⇒ Output freq of PLL can go up to 80MHz (needed is 40-50 MHz)
- ⇒ Full chain tested with charge injected on one and readout

} Tests OK



Digital: Memory mapping

- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
 - “1”: general data (Hit ch number and number of events)
 - “0”: BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:



	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336

- Zero suppress (only hit channels are readout): **test OK**

The screenshot shows the Omega DAQ software interface with several panels:

- Step by Step DAQ:** Includes buttons for 'Reset ASIC Digital', 'Start Acquisition', 'FPGA External Trigger', 'Start ReadOut1', and 'Start ReadOut2'. It also shows 'ChipSat' and 'End ReadOut1' status indicators.
- Automatic DAQ:** Includes 'Automatic DAQ', 'Start Acq. Sequence', and a 'Nb of Acquisitions' field set to 10. A note states 'ChipSatb must be enabled SlowClock -> CLK_GENE_EXT'. The 'TimeOut for 1 Acq/Conv/RO' is set to 10ms (Slow Clock @ 5MHz).
- Data Analysis:** Includes 'Clean DAQ data folder' and 'Analyze saved data now!' buttons.
- Frame received OK ?** shows 'OK' with a green indicator.
- Nb of bits read in ASIC RAM** is 304.
- Chip ID 2** is 100111.
- Current Acquisition** is 0 and **# files found** is 0.
- ASIC Memory (Raw Data) / Decoded Data:** A table showing 'HR3 Decoded Data' with columns for Channel #, BCID, and E1 / EO. A callout box says 'Signal injected only in ch 20 and 43'.

Channel #	20	20	20	20	20	20	20	20	43	43	43	43	43	43	43	43	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BCID	3753	3253	2753	2253	1753	1253	753	253	3753	3253	2753	2253	1753	1253	753	253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
E1 / EO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

- Roll mode SC : **test OK**
 - If RollMode = “0” → Backward compatibility with 2Gen ROC chips behavior
 - Only the N first events are stored
 - If RollMode = “1” → 3Gen ROC chips behaviour
 - Use the circular memory mode
 - Only the N last events are stored
- “Noisy Evt” SC: 64 triggers => Noisy event => no data stored : **test OK**
- “ARCID” SC (Always Read Chip ID): **test OK**
 - If ARCID = 0 → Backward compatibility: No event → No readout
 - If ARCID = 1 → New behavior: No event → Read CHIP ID

Power consumption in ILC mode:

- ⇒ Power measured on AlimChip over 1 Ohm resistor
- ⇒ Buffer/SSH/ Widlar/OtaQ/OtaFSB/Temperature OFF
- ⇒ Pll/FastClock LVDS = 0/1 if clocks from LVDS else 1/0
- ⇒ EnPllOut / testOtaQ / ValdSS are disabled
- ⇒ StartAcq On

Power supply	HR3 With Clk from LVDS (Slow clock 5M + 40M) Consumption in μW / channel	HR2 With Clk from LVDS (Slow clock 5M + 40M) Consumption in μW / channel
PowerOnA (Analog)	1650	1325
Only PowerOnADC (OTA)	0	0
Only PowerOnDAC	55	50
Only PowerOn D	725	50
Power-On-All	2430	1425
Power-On-All @ 0,5% duty cycle	12,2	7,5

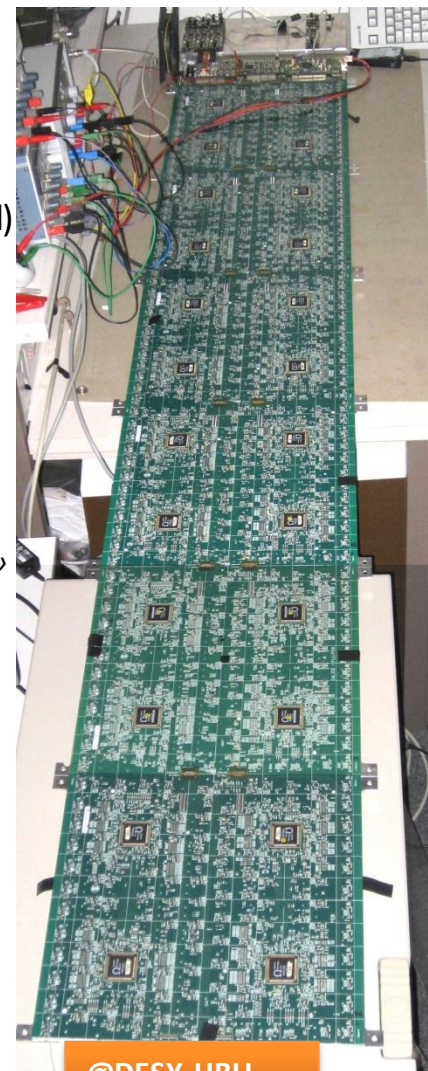
Notes:

- ⇒ Analog: increase due to extended dynamic range
- ⇒ Digital: increase due to zero suppress
- ⇒ If the PLL is activated, +3% on the power consumption

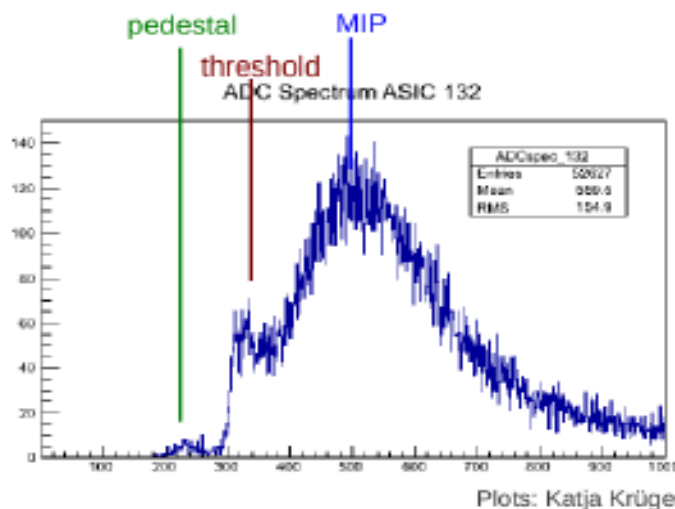
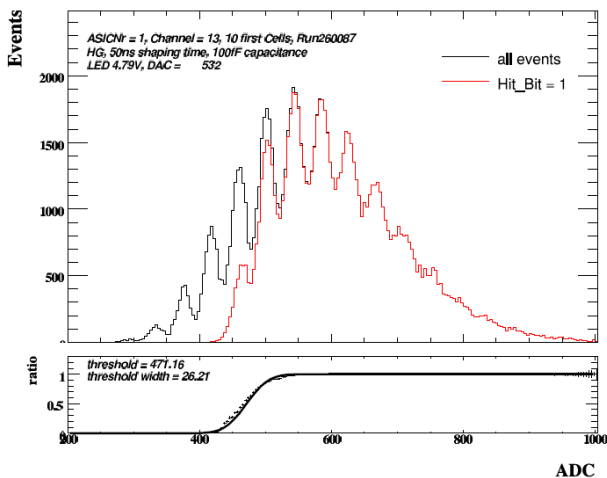
36 channel chip to readout the SIPM of the AHCAL

- Autotrigger on 1 spe (150 fC), 16 depth SCA for charge measurements (up to 300 pC) and time measurement (< 1 ns)
- 2 memories of 2K bytes to store charge and time measurements from the internal 12 bits ADC
- Many measurements on testbench and at system level with Spiroc2b (referred to vdd)
 - Pedestal shift when large pulses (> 1000 pe-) are sent in one channel
 - pb solved in spiroc2c (preamp referred to gnd) but digital coupling through the substrate....
- New HBU (HBU3): decoupling capacitors of SiPm and of the ASIC bias points to vdd (instead of gnd)
- Klaus chip (Heidelberg): Alternative of spiroc2

See Aliakbar EBRAHIMI's talk, « AHCAL devolpments »



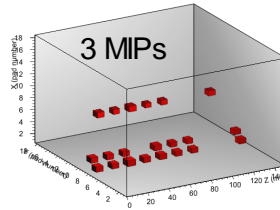
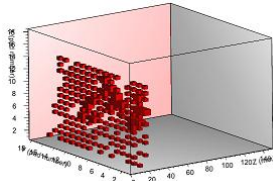
@DESY, HBU



SPIROC3 is technically feasible after HARDROC3 tests, but

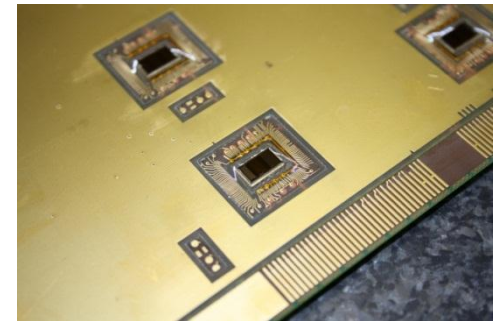
- expensive chip: area 32 mm² for spiroc2/ ~50 mm² for spiroc3
- difficult testbeam tests: independent channels, zero suppress
- Slow control: I2C link difficult to integrate with the existing setup (DIF, DAQ) + need to keep the same pinout to use existing HBU
- **Engineering run with SPIROC2D** -end of 2014- taking account the following points listed by DESY
 - > Pedestal shift when too many channels have a high signal: ~understood
 - > Memory cell dependent amplitude decay: Fixed (*compensation caps*)
 - > Slow-Control configuration is problematic for long slabs: ?
 - > Feedback of channel-wise trigger thresholds on the global threshold. Fixed
 - > Random zero events and zero-results for the first trigger: Fixed
 - > Poor uniformity of the input DACs: Fixed
 - > Holdscan is different for HG/LG: Fixed
 - > Trigger threshold width increases with threshold height: Fixed
 - > Amplitude-to-threshold relation depends on preamp setting and pulse shape
 - > TDC: to be redone using blocks from other chips
 - Amplitude dependent time-shifts and channel-to-channel spread
 - Result depends on which ramp is used and the memory cell.
 - big chip-to-chip spread of ramp slopes.

- ❑ 64 channels for ECAL (Si pin diodes)
 - Autotrigger on 0.5 MIP (2 fC), 15 depth SCA for Charge measurement (1/2 MIP-2500 MIPs) and Time measurement (< 1 ns), 1 memory of 4K bytes to store the digitized measurements of Charge and Time by the internal 12 bits ADC
 - Testbench measurements: very good performance, much more difficult on FEVs
- ❑ Successful test beams @ DESY in 2012 (1 to 6 layers) and 2013 (10 layers), power pulsing mode, autotrigger mode, e⁻ (1 to 5GeV)



❑ BUT

- Plane events
 - Input PA referred to vdd (= Spiroc2b) and power supply common to the ASICs
 - Depend of the number of ASIC with hits and of the number of channels that triggered
 - Number of plane events reduced from 80% down to 10% using decoupling capacitors and separating vdda and vddd_delay
- FEV boards: difficult design, special care is needed to avoid couplings and retriggering
 - Vdd handled as a “ground” plane, decoupling capacitors connected to vdd



- ❑ Submission of SKIROC2B in the engineering run (end of 2014)
- ❑ *Submission of building blocks using 180nm Silicon On Insulator or 180nm SiGe technology* (Phd student LLR/Weeroc and AIDA WP3.3/AIDA2)



FEV with skiroc2 in BGA₁₅

- Good performance of HARDROC3 (AIDA Milestone):
 - dynamic range extended up to 50 pC
 - PLL: alternative for fast clock
 - Zero suppress, roll mode, ARCID mode, Noisy evt mode tested successfully on testboard
 - External trigger available to be able to check the status of each channel
 - I2C link (after the buffer bug correction) tested and validated

- Next steps
 - Hardroc3:
 - More intensive tests to be done on hardroc3: zero suppress and analog part (multiple channels)
 - 2-3m long RPC chambers to be built and equipped with HR3 in 2015. TESTBEAM tests to be done
 - Spiroc2d and skiroc2b
 - Conservative modifications and correction of known bugs, same pinout
 - Study of building blocks in 180 nm SOI/SiGe technology (see WP3.3)

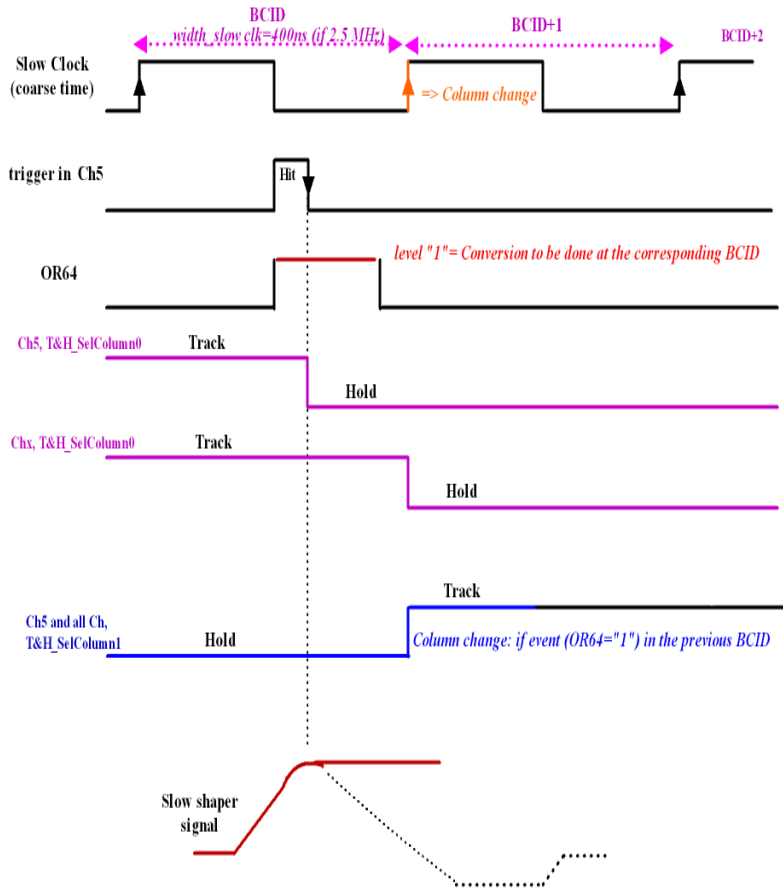
 - **Engineering run end of 2014**
 - HARDROC3b (I2C bug corrected), SPIROC2d, SKIROC2b and chips for other applications
 - 6 wafers => ~300 ASICs/each type of ASIC
 - ~200 k€ for the run, packaging, testboards: 40k€ left from AIDA, other users to complete

Backup slides

SK2: BCID + 1 wo hit

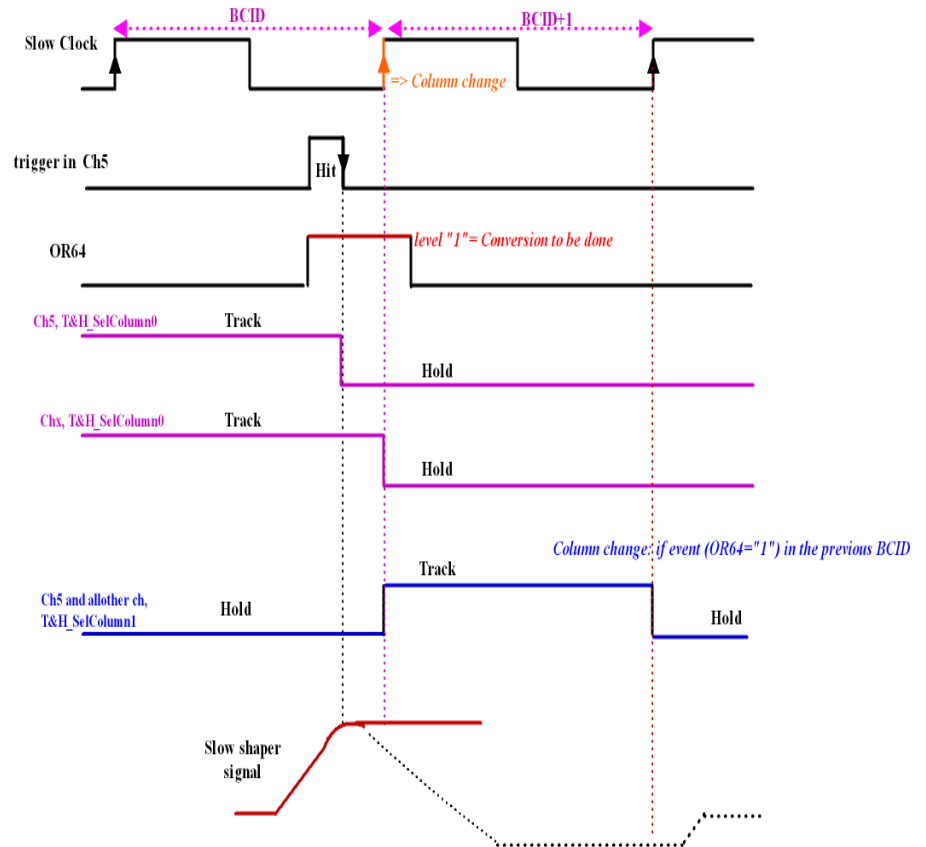
Probability of such events= Width OR/width clk

CASE 1: BCID with Hit



Conversion: BCID with one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal, other SCAi=ped
 BCID+1: No conversion because OR64 level=0 during this BCID+1

CASE 2: BCID+1 without Hit



Conversion: BCID, one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal
 BCID+1, no hit, SCA1 ch5 holded value=value < pedestal or pedestal, other SCA1 holded value=ped.