65nm IC technology access, support and IP Blocks

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Foundry Services News

- Contract with TSMC
  - Foundry access via IMEC
  - Long procedures for negotiating technology information disclosure legal terms and contractual pricing conditions for prototyping and production services
    - Signature of NDA is imminent
  - Contract covers a period of 5 years (2013-2017)

PDK and Mixed Signal Design kit

- **Development of a "Design Kit" for Mixed Signal environments.**
    - With integrated standard cell libraries.
    - Establish well defined Analog & Mixed Signal design workflows.
    - Implemented on modern versions of CAE Tools (Europractice distribution)
    - Physical Layout views available.
   - Suitable for analog, digital and mixed design

- **Foundry database not made for full M/S interoperability**
    - Technology library and PDK in OA (and CDB)
    - Digital libraries delivered in CDB only

- **Integration work done by VCAD (Cadence)**
    - Many modifications in the technology file
    - Ported digital libraries to OA for full M/S flow
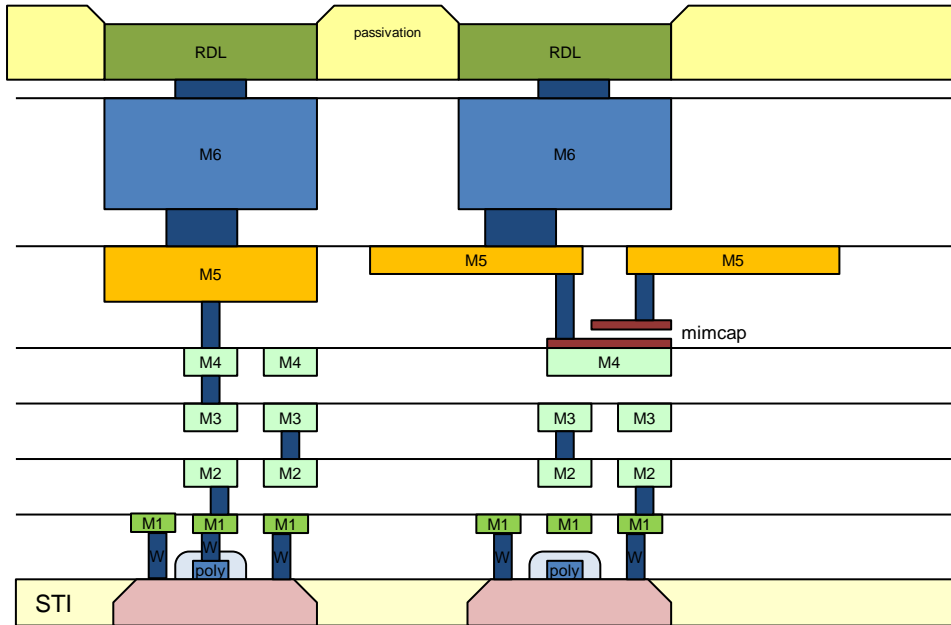   - Validated by CERN
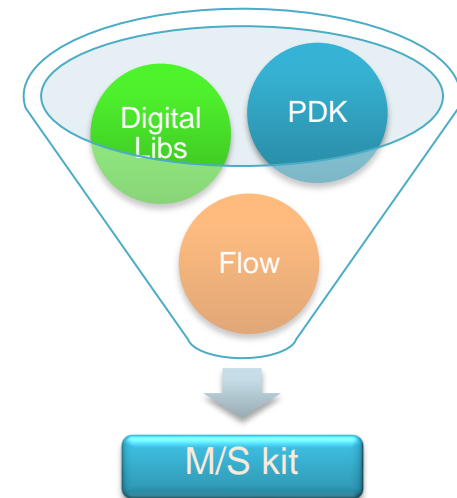
TSMC 65nm M/S flow distribution

- **M/S flow ready for distribution**
  - Waiting for NDA to be signed
- **Distribution of package to institutes done by IMEC**
  - Sign NDA with institutes
  - Distribute the M/S design kit and workflows
  - Provide maintenance and updates in collaboration with VCAD
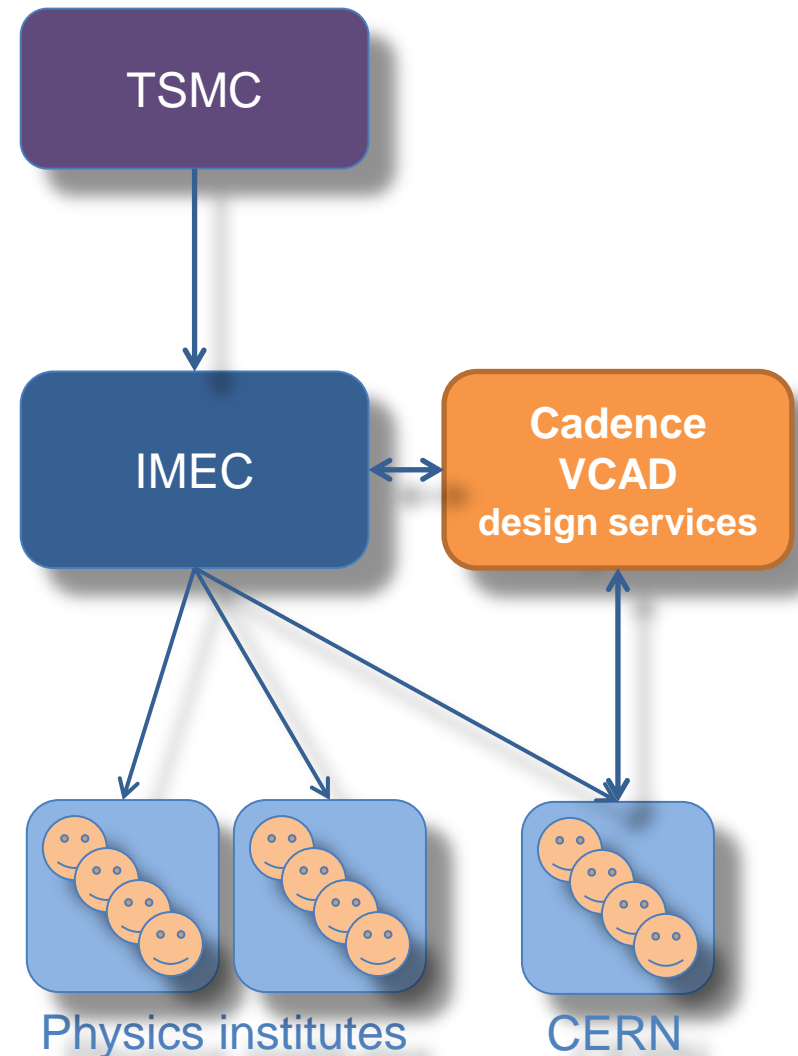
- Access to layout views & modification allowed by foundry
  - Clause of no-redistribution except to signatories of NDA (list to be updated annually)
  - Discharge of any foundry liability for modified libraries
  - Modified library is still foundry property
 - Libraries can only be used with TSMC via IMEC

- **CERN 65nm mixed signal (M/S) kit supports**
  - 2 metal stacks
    - 6+1 metals ("base metal stack")
      - 4-thin, 1-thick, 1-UTM , RDL
    - 9+1 metals (compatible with IMEC mini@sic)
  - Optional: (fees apply)
    - 7+1 metals
      - 5-thin, 1-thick, 1-UTM , RDL
  - 2 choices of std. cell libraries
    - 9-tracks, standard-Vt
    - 7-tracks, high-Vt
  - Standard I/O library
    - Limited radiation performance

Training: M/S kit Workshops

- A series of Training Workshops for 65nm CMOS will be organized
  - To present the Mixed Signal Kit.
  - To present Analog, Digital and Mixed Signal design Workflows.

  - 1st CERN-internal workshop took place in February 2014
    - 13 participants

  - Cadence (VCAD) design services team:
    - Prepared the training lectures and the accompanying documentation
    - Will provide engineers to lecture in the courses.

  - 3 days training with lectures and hands-on design exercises

  - Workshop modules based on a realistic Mixed Signal Design

  - Training material (scripts, design examples and documentation) made available to participants.

  - All participants must have signed the NDA

Example Mixed Signal ASIC:
"8-bit DAC with I^2C serial interface"
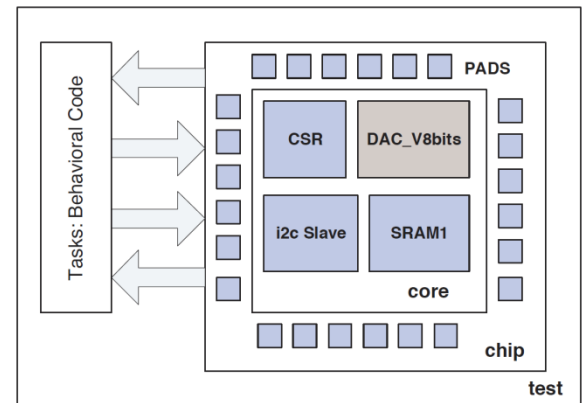
Rad-hard IP Blocks in 65nm

- SRAM compiler

- I/O pad library

- Monitoring ADC

- Bandgap

- Rad-hard to 200Mrad according to specifications

SRAM Compiler

- Pseudo-dual-port (one read + one write in one clock cycle)
- 80 MHz operation
- Minimum size: 128 words of 8 bit
- Max size: 1k words of 256 bits
- Specifications on minimum W of transistors for radiation hardness
  - WPMOS>500nm, WNMOS>200nm
  - Cell size: 1.450 x 2.535 um2
- Part of the blocks are SET tolerant (in green in the figure)
  - If Hamming or other coding is used, SRAM becomes fully SEU tolerant
- Power consumption (simulated for a 1024x32 SRAM)
  - Read+write: 30 uW/MHz
  - Only read: 16 uW/MHz
  - Only write: 17 uW/MHz
  - Idle/static: 3 uW
- Delivery expected May 2014, radiation tests will follow

# ESD structures and I/O pads
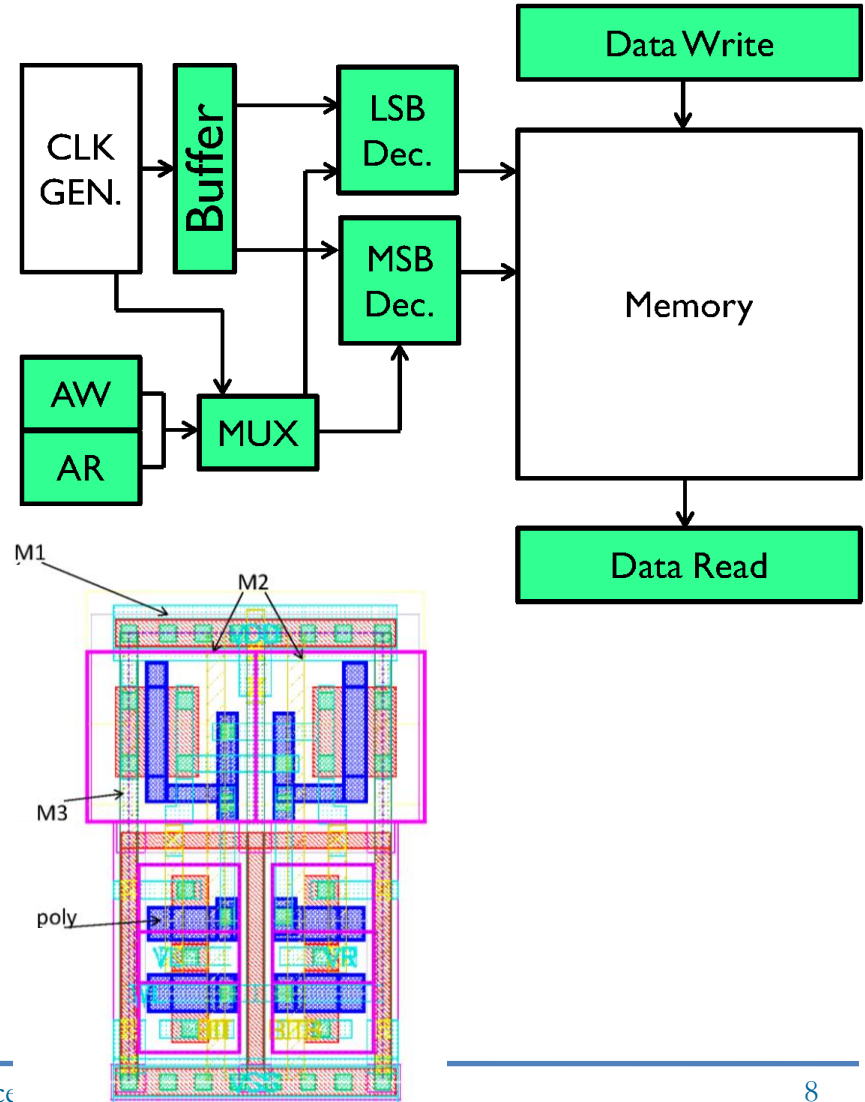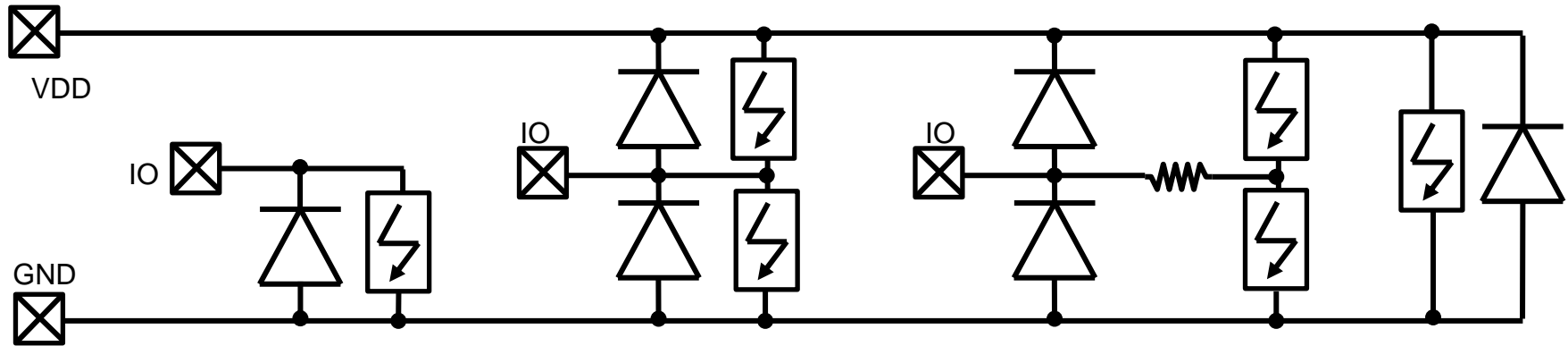
- Rated for 1.2V
- Only core devices, thin gate oxide
- Subcontract the development work for rad-hard ESD circuitry
  - Power clamps
  - Low-capacitance analog I/O
  - HBM+CDM ESD-protected I/O for digital
  - Purchase order sent March 2014

- I/O drivers and receivers to be designed at CERN

- ADC
  - 12 bit, 32 channels
  - Sampling rate 5 kS/s
  - 0.8 V full scale
  - power <500uW
  - input max slew rate 1 V/s
- Delivery expected by end 2014,Q2, tests will follow
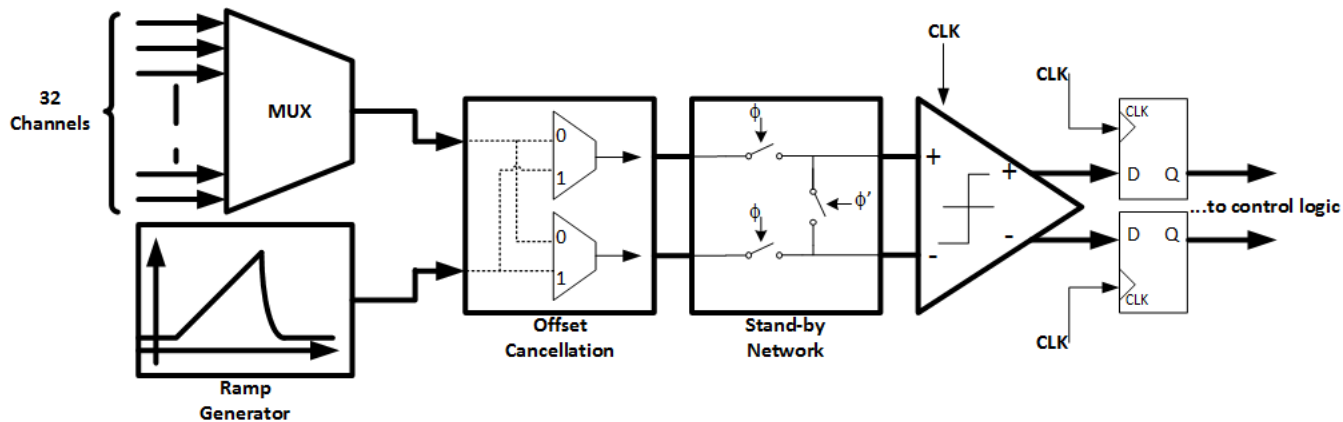
- Current-mode
- 300mV ± 1% output
  - over p,V,T
  - (T from -10 to 50 °C)
- power cons. <240uW
- Delivery expected by end 2014,Q2, tests will follow
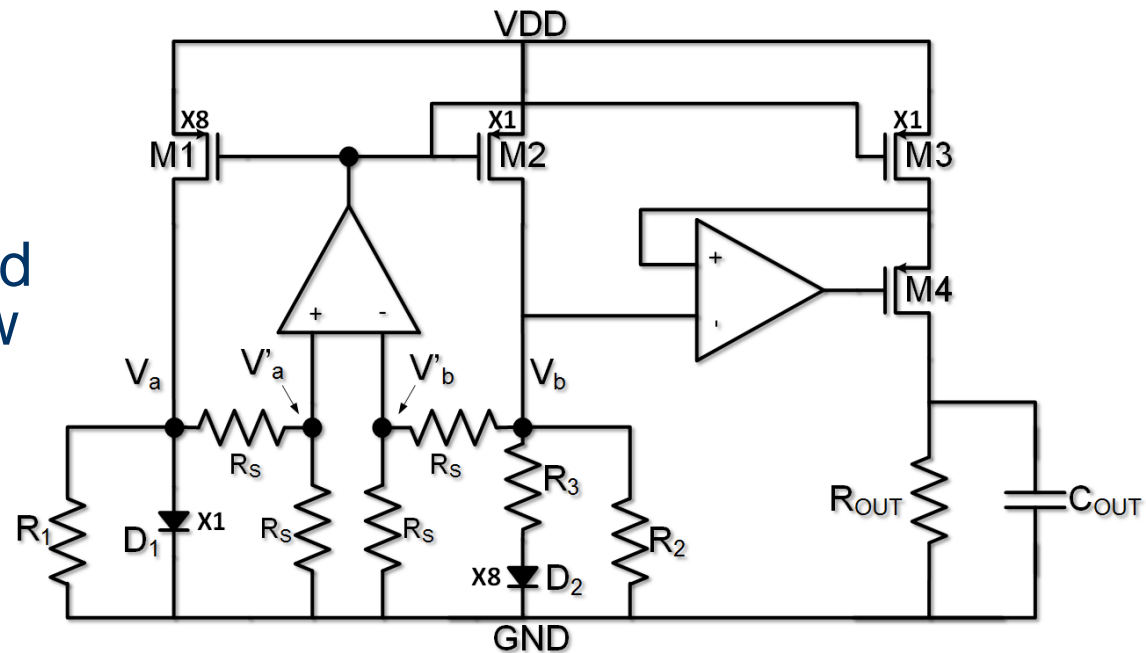
Foundry IP

- **Foundry provides a wide range of IP blocks**
  - Electrical fuse blocks / NVM
  - PLLs
    - 100MHz – 1600MHz
    - Jitter enhancement
  - Specialty I/O
    - USB 2.0 / UTMI+
    - DDR2 (up to 800Mpbs), DDR1 (up to 533 Mbps)
    - Crystal oscillator, 32kHz
  - ROM compiler
  - Register File compiler
    - Single- and dual-port
  - SRAM compiler
    - Single-port and dual-port
    - Low-power and low-leakage

- **Radiation performance not tested**

Foundry access to TSMC 65nm

- Physics institutes to send the purchase order via CERN
- GDS will be submitted directly to IMEC

- MPW as scheduled from IMEC and foundry
  - Foundry MPW
    - every 4 weeks (for qualified fab)
    - area > 12 mm2
  - mini@sic
    - Twice a year
    - Min. area ~ 4 mm2
    - 7-thin, 1-thick, 1-UTM, RDL
- Additional runs for HEP
  - Metal stack 4-thin, 1-thick, 1-UTM, RDL
  - Possibly every 4 months?

- Engineering/production runs
- CERN will handle logistics (shipping and distribution)
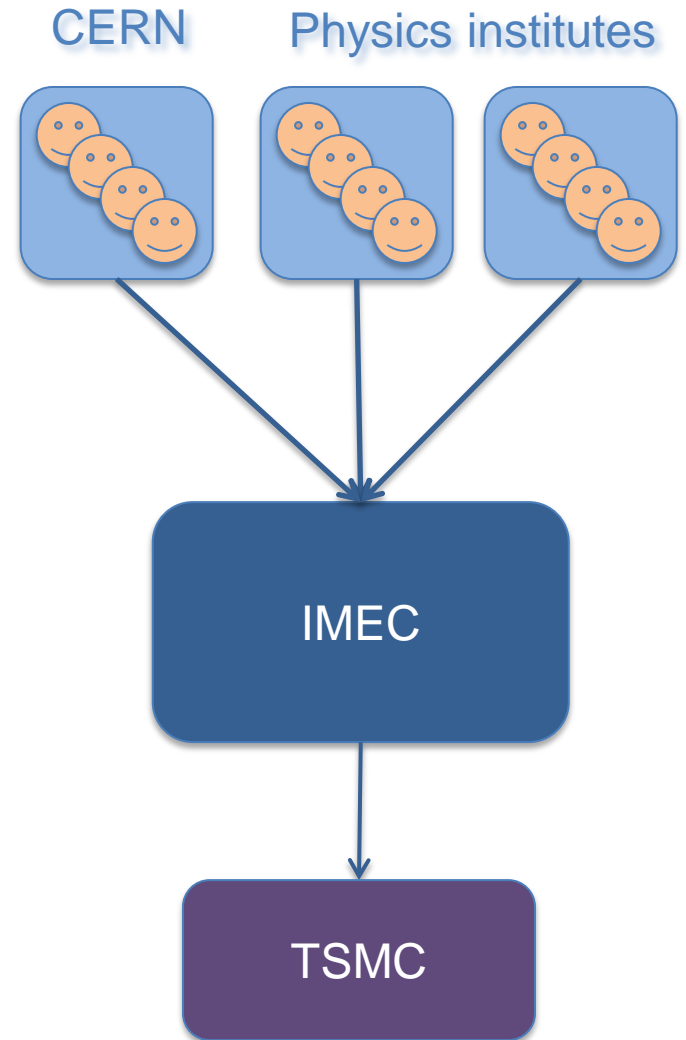
Soft-IP blocks

- **I2C slave**
  - 7- and 10-bit addressing

- **HDLC communication protocol**
  - Variable bit-rate
  - Average 7% bandwidth overhead

- **7b8b communication protocol**
  - DC balanced
  - Fixed latency
  - Control characters available

Thank You