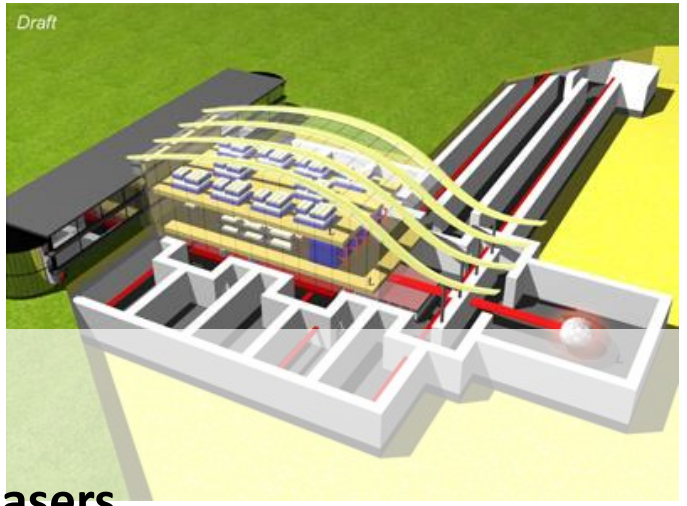
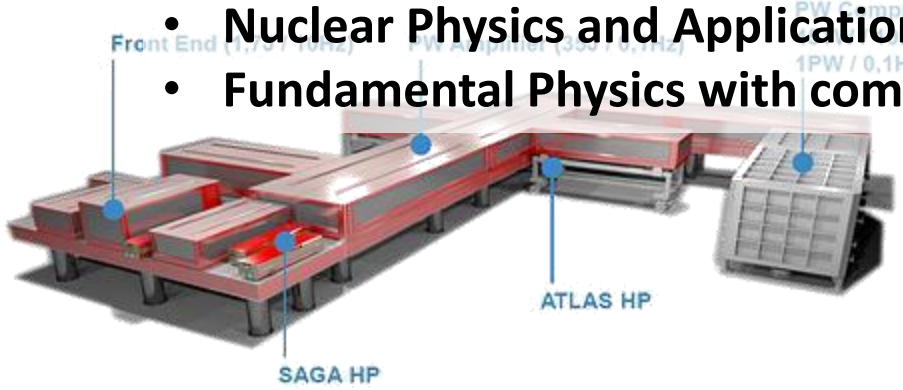
Integrating High-Speed ADCs in the SRS System for Scintillating Detectors in PW-laser Driven Physics Experiments

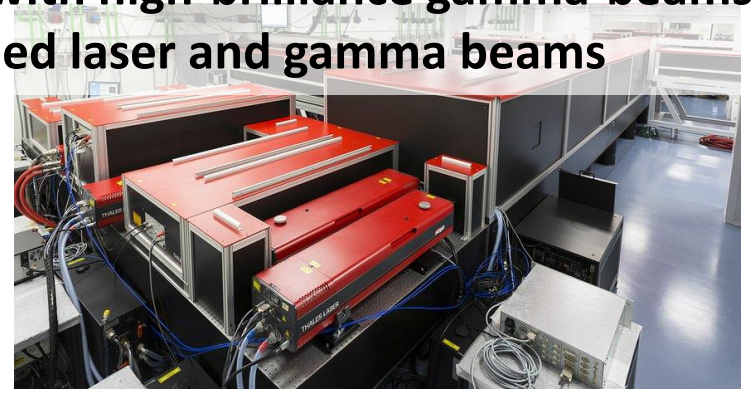
Sorin Martoiu (IFIN-HH, Bucharest)

ELI-NP and CETAL



- High-Power Laser System
- High-Brilliance Gamma Beam
- Nuclear Physics with High-Power Lasers
- Nuclear Physics and Applications with high-brilliance gamma-beams
- Fundamental Physics with combined laser and gamma beams



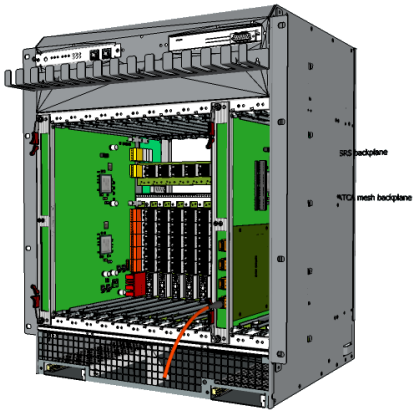


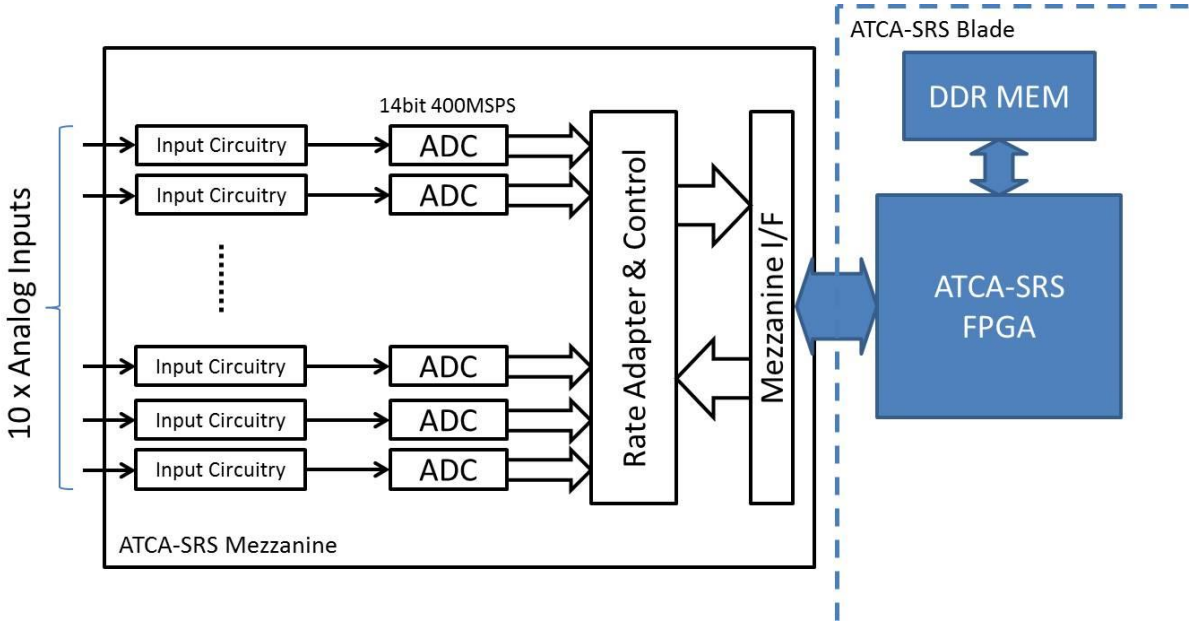
Requirements

Detector type	Front-end	Data size MB/pulse/detector	Number of detectors	Laser Rep. Rate	Throughput (MB/s)	Trigger	Trigger jitter
1) gated CCD 4 Mpixels	USB	8	< 5	0.01 - 10 Hz	< 400	External, synchronized with laser pulse	0.1 ns
2) LaBr3 with PMT	Digitizer w/o PSA: >400 MS/s, 14 bits (trace of few ms)	1	10	0.01 - 10 Hz	< 100	External, synchronized with laser pulse	0.1 ns
	Digitizer with PSA: >400 MS/s, 14 bits (gamma time and energy in-between laser pulses)	n/a	10	n/a	< 0.4	Internal: threshold on amplitude, OR External: from a CFD	
3) plastic scintillator with PMT	Digitizer w/o PSA: >1 GS/s, 12 bits (trace of few µs)	0.01	10	0.01 - 10 Hz	< 0.1	External, synchronized with laser pulse	0.1 ns
4) Ge or $LaBr_3$ detectors for Decay Station	Digitizer with PSA: 100 MS/s, 14 bits	n/a	8	n/a	< 0.1	Internal: threshold on amplitude, OR External from a CFD	
	TDCs (for fast-timing experiments)	See requirements from gamma spectrometry with gamma-beam					

400 MSPS ADC Mezzanine

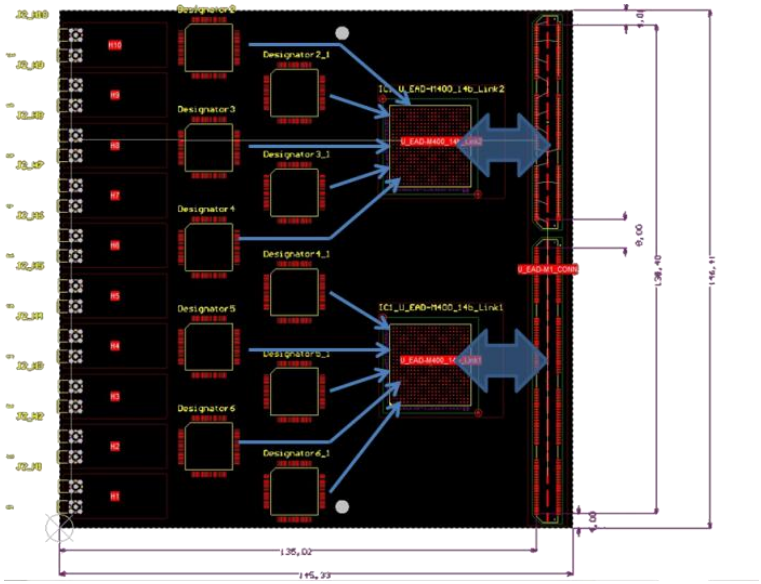
ATCA-SRS

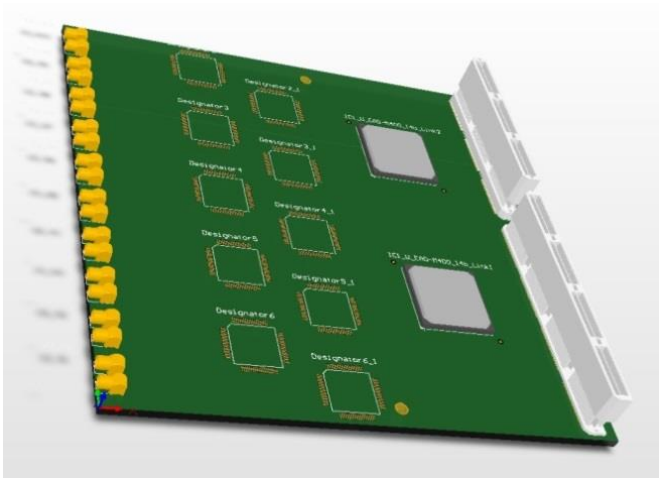




- 10 x analog signal processors
  - Differentiale/single-ended input
  - Variable attenuation, equalization,…
- 10x 14 bit 400MSPS ADC
  - ADS5474 (Texas Instruments)

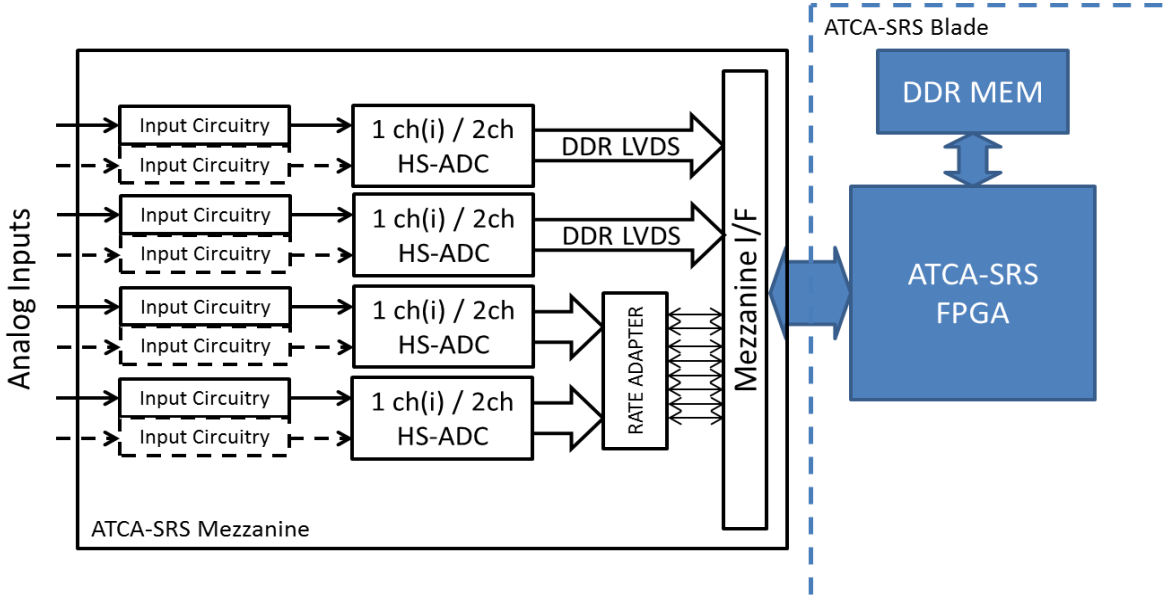
400 MSPS ADC Mezzanine

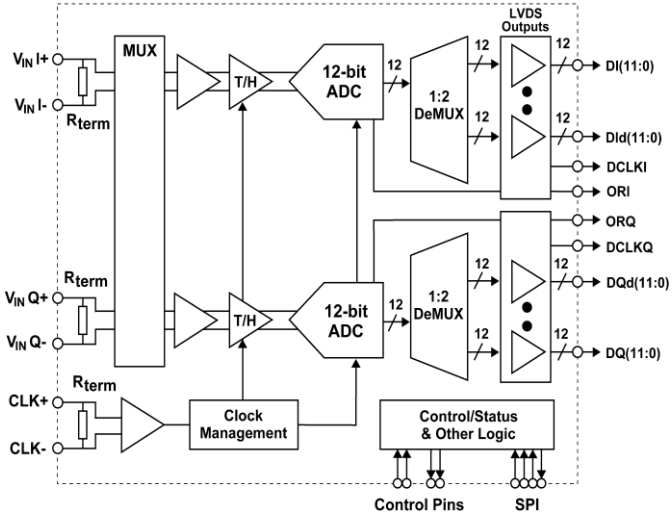




- Bandwidth Adapter circuit
  - Implementation with low-end FPGA
  - Input: 160 bit @ 400 Mbps (LVDS)
  - Output: 40 lanes @ 1600 Mbps (800 MHz DDR ; LVDS)

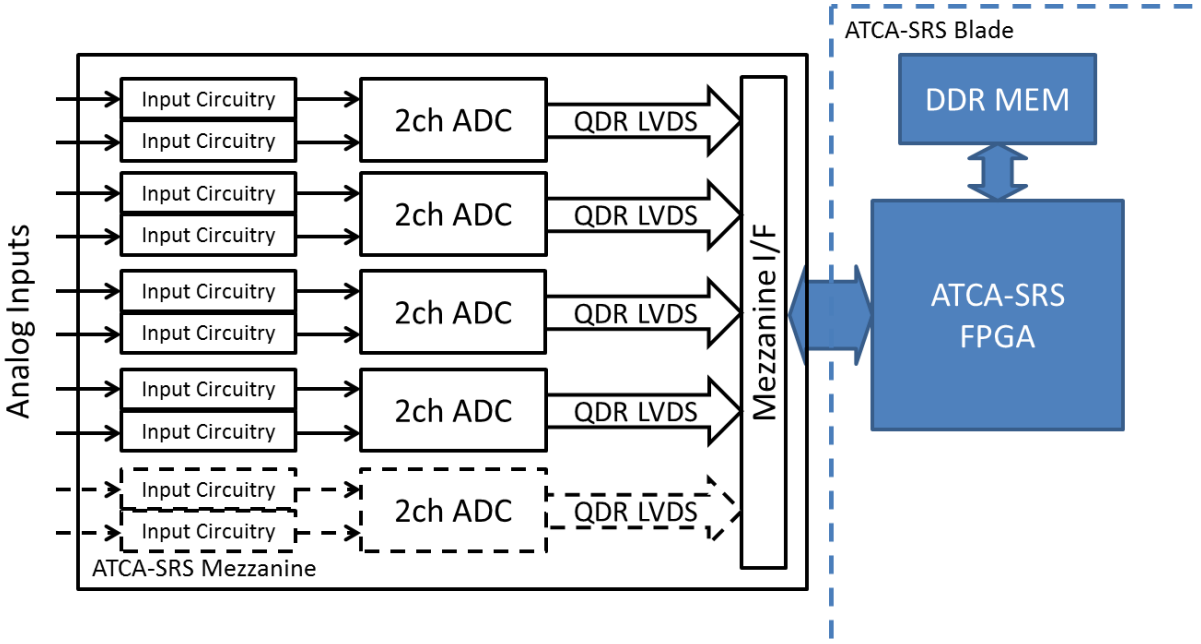
1GSPS ADC Mezzanine





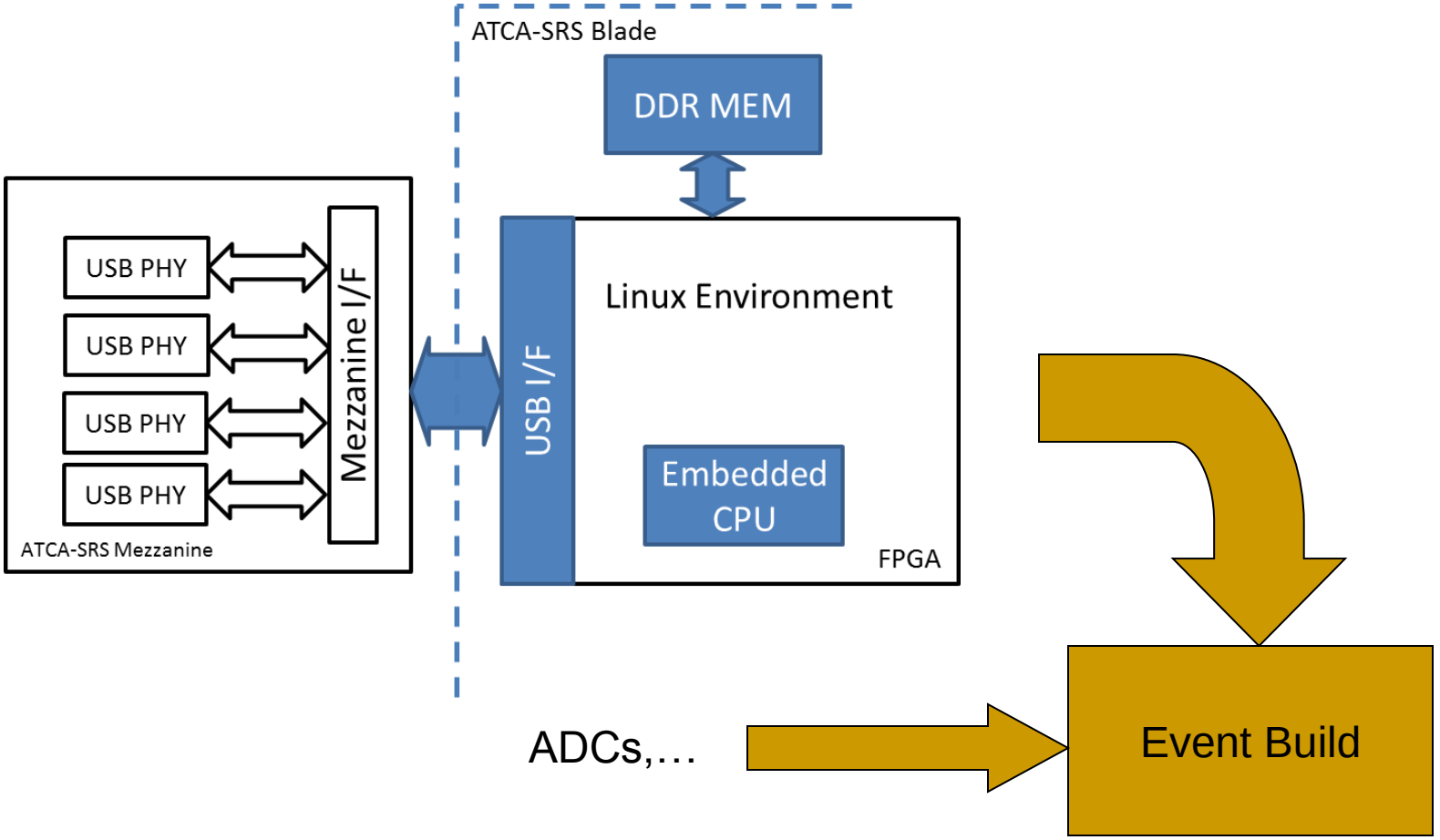
- 4 High-Speed Dual 12-bit ADC
  - ADC12D500RF (TI) – 500MSPS dual / 1000MSPS interleaved (1ch)
  - ADC12D800RF (TI) – 800MSPS dual / 1600MSPS interleaved (1ch)
  - ADC12D1000RF (TI) – 1000MSPS dual / 2000MSPS interleaved (1ch)

250MSPS ADC Mezzanine



- 4(5) duap ADC circuits, up to 250 MSPS
  - ADS42LB49 – 14 bit (Texas Instruments)
  - ADS42LB69 – 16 bit (Texas Instruments)

USB Mezzanine for CCD interface



Project Status

- Feasibility study completed
- Next steps
  - Prototype production
  - Functional and performance tests
  - Possibility to implement first laser driven experimental setup at CETAL, Bucharest
- Other applications of high-speed ADC in RD51?