Resistive Micromegas for the SDHCAL

Status of on-going analysis of charge-up effects

M. Chefdeville, LAPP, Annecy

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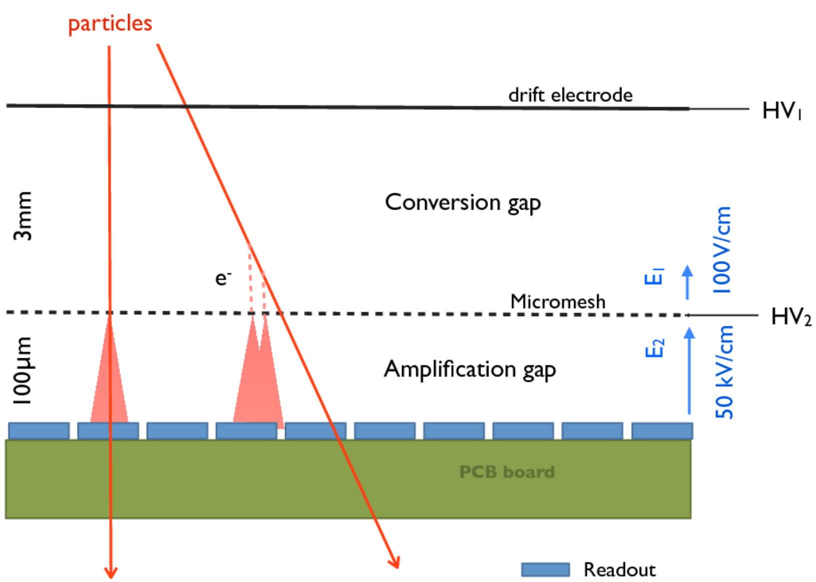
Overview

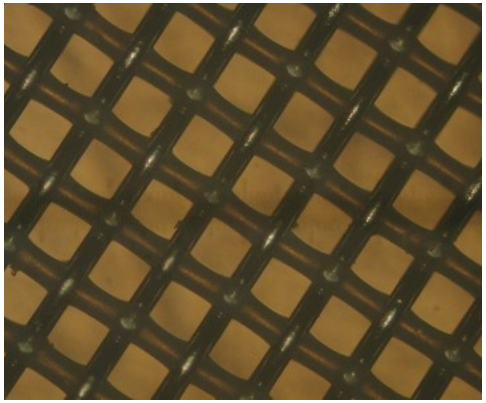
- ✗ Micromegas calorimetry at a LC
- ✗ Resistive prototypes
- ✗ Test beam results
- ✗ Charge-up effects

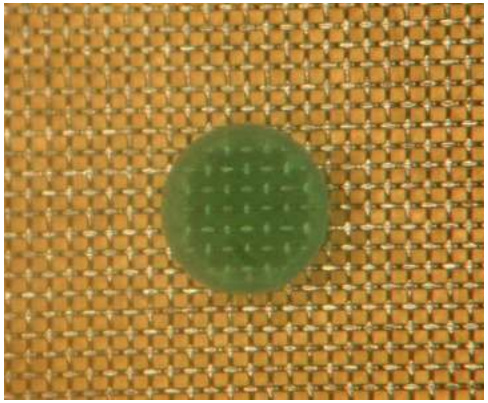
Micromegas & gaseous calorimetry

Low multiplication factor – Narrow avalanche – Fast ion collection → Space charge field ~ 0

→ Signal are proportional to the energy deposited in the gas ↔ ***linear response***







Mesh lies on pillars (1% dead zone) → uniform E-field → *Small constant term & easy calibration*

High rate capability of tens of MHz/cm^2 → *Barrel/endcap/forward region-compatible*

Simple gas (e.g. Ar/CO_2) & low voltages (500 V, 40 kV/cm) → *No ageing*

Gas gain dependence on P/T/V well known → *Response stable with time*

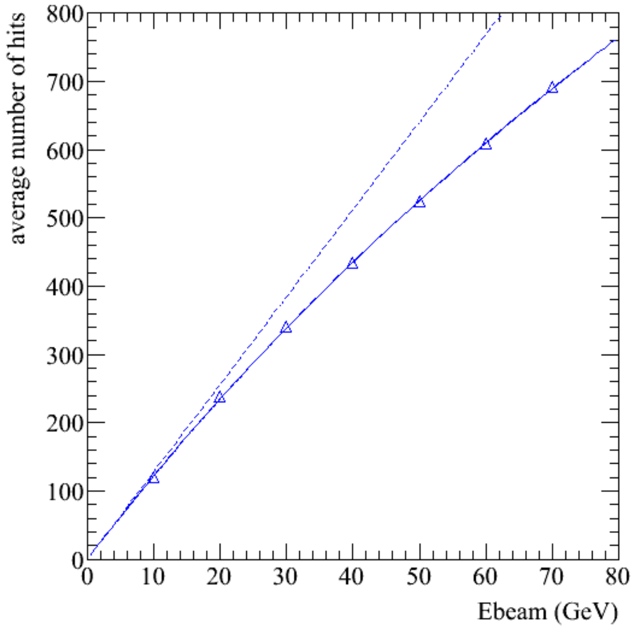
Semi-digital hadron calorimetry

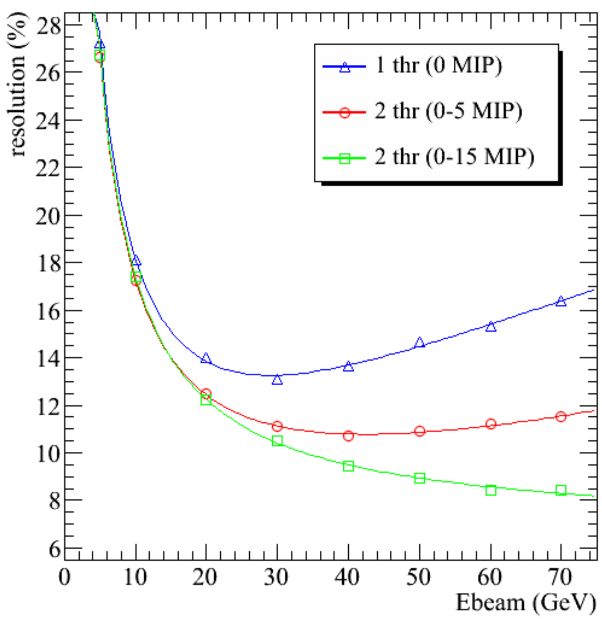
Micromegas suitable for EM & H calorimetry. In the case of Particle-Flow calorimetry:

✗ Alternative to Si for W-ECAL but with larger Molière radius & worse energy resolution;

✗ *Candidate for a Fe-DHCAL (ILC)* and W-DHCAL (CLIC).

Expected response & resolution to pions of an 11 λ_{int} HCAL with 1-bit & 2-bit readout (Geant4)

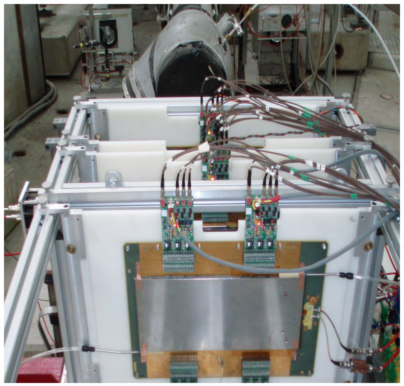


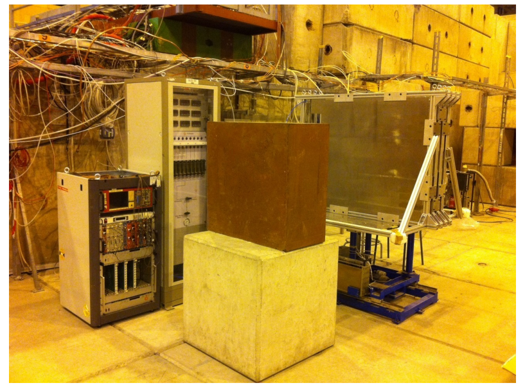


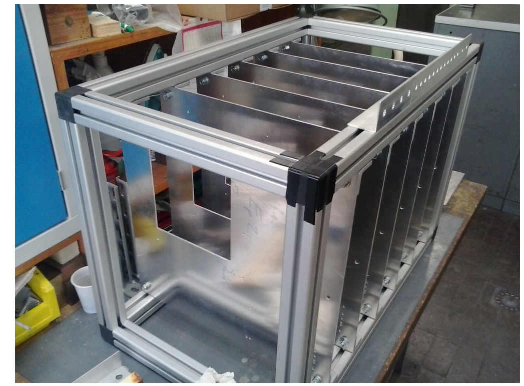
The response of a DHCAL is saturated (cell size VS R_M) with consequences on the energy resolution.

But off-line compensation techniques can be used to correct for it, e.g. 2- bit readout.

Chronology





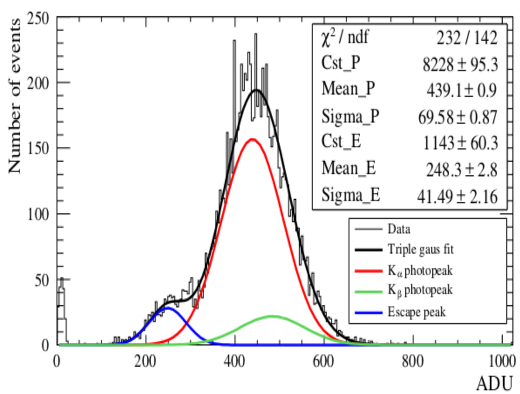


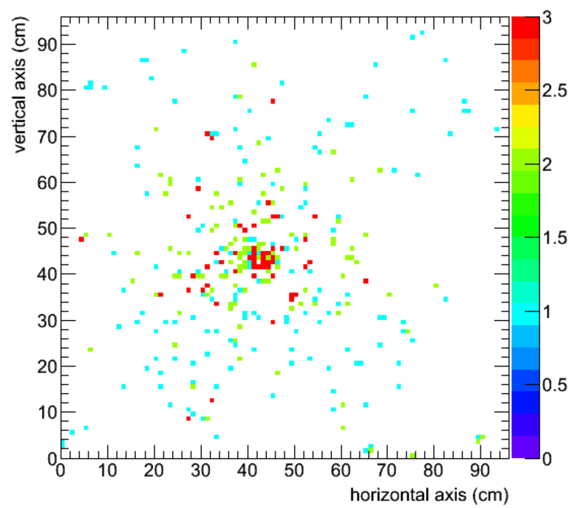
2006-2009 | 2009-2012 | 2012-2013

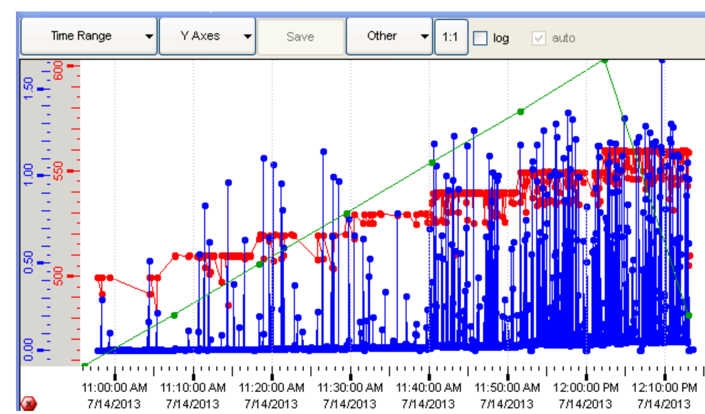
Proof-of-principle

Large area (SDHCAL)

Spark protection (SPLAM)







Resistive prototypes, motivation and challenges

At shower max (in 1x1 m^2 layer), for 150 GeV pions, spark probability/pion ~ 10^{-6}

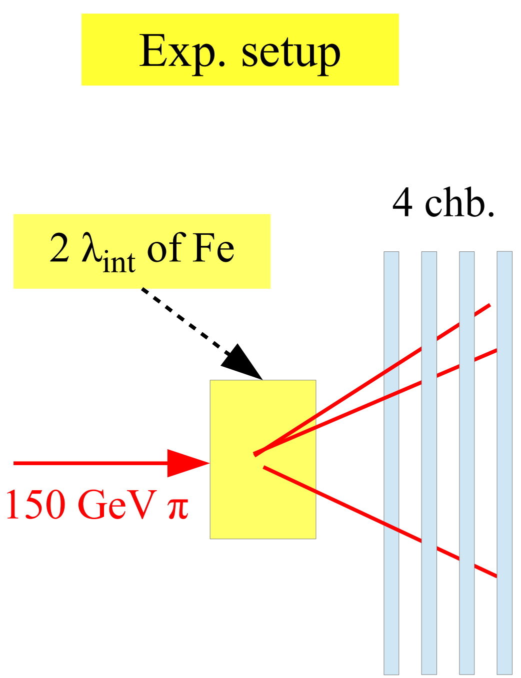
Small but a calorimeter will have 40 layers → Avoid discharges

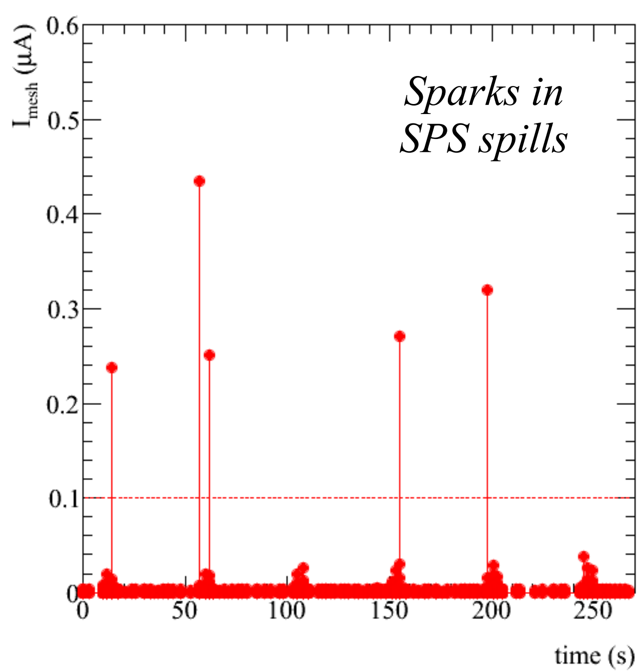
+ Simplify PCB by removing current-limiting diodes

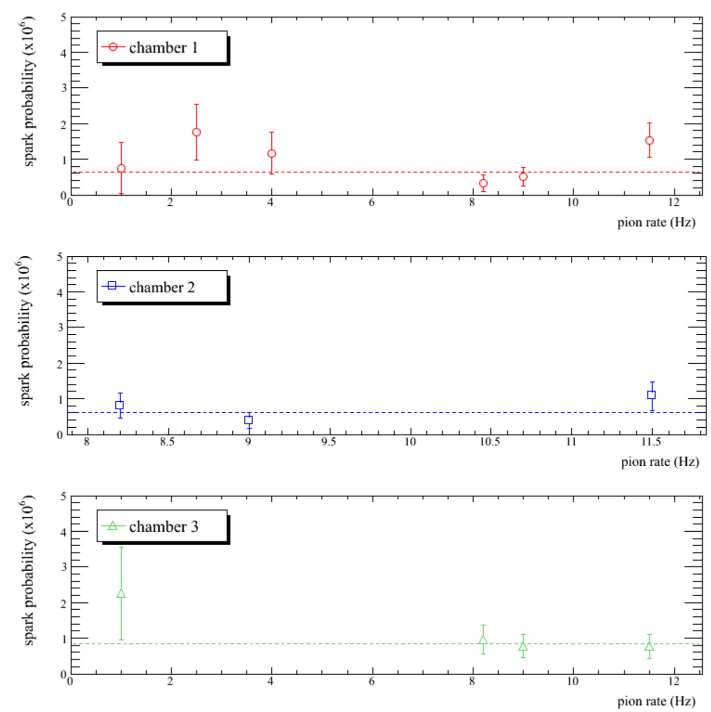
Effects to minimise

Lateral spread of charge to maintain imaging capability (multiplicity ~ 1.1)

Loss of linearity (= rate capability) for "large" charge density, like in shower core







Resistive prototypes, designs

Resistive pad + via

Insulating layer, 64 µm thick

The R-layer (a few MΩ/□) is segmented into pads of same size as readout pads

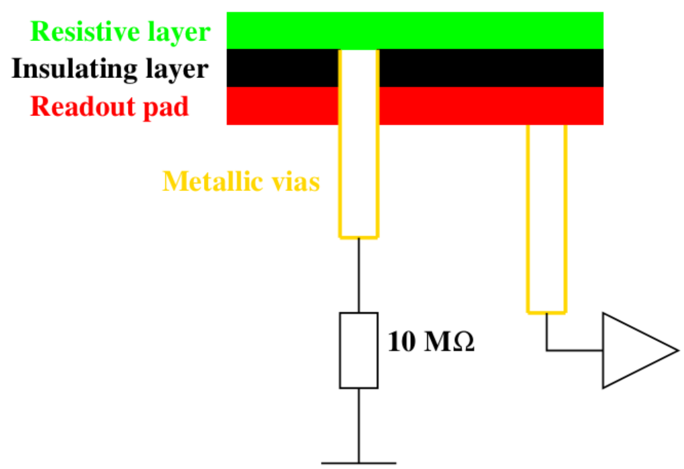
The charge is evacuated to ground through a via

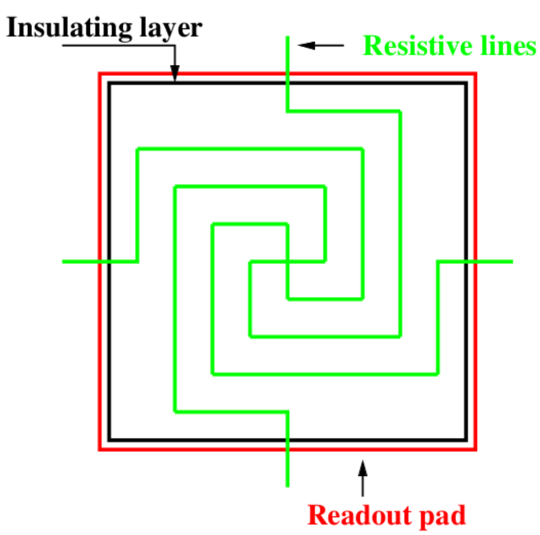
Resistive line

Insulating layer, 64 µm thick

The R-layer (a few MΩ/□) is patterned into strips that run over all pads

The charge is evacuated to ground on one pad board side





Resistive prototypes, Active Sensor Unit (ASU)

ASU = Bulk + pad (with or w/o R-layer) + ASIC

Bulk + R-layer made @ CERN

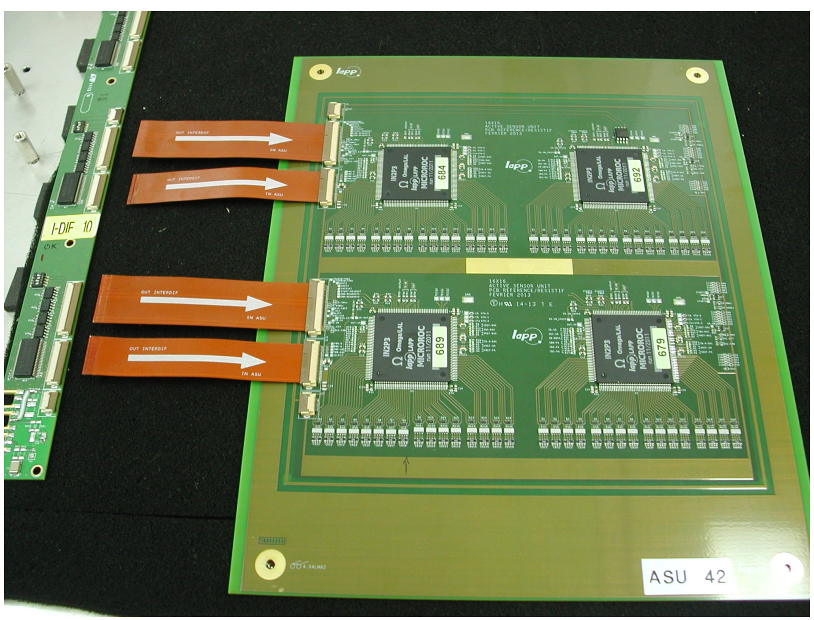
4 ASIC = 4 MICROROC → 4*64 = 256 channels with preamp./shaper/3 discri./RAM

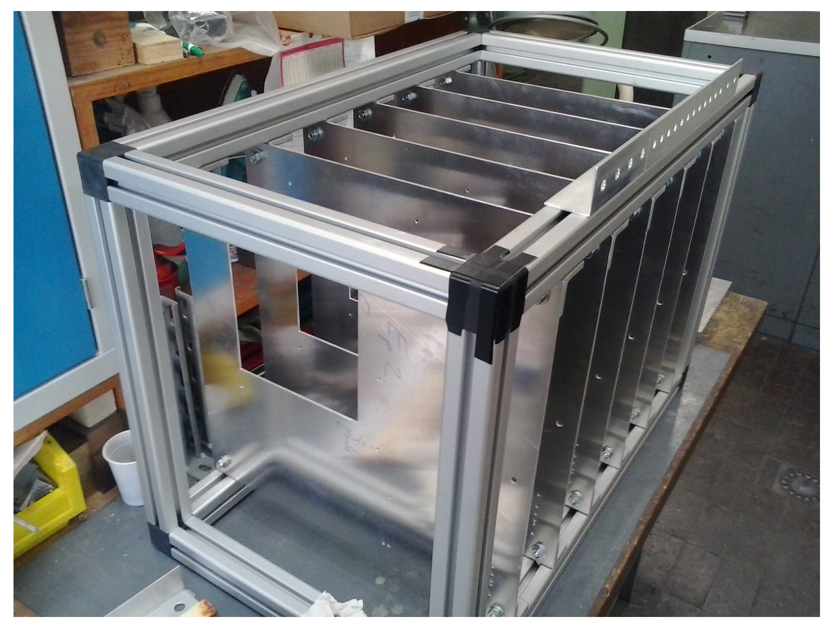
Testbeam air stack

Drift gap of 3 mm, ~10 cm between prototypes

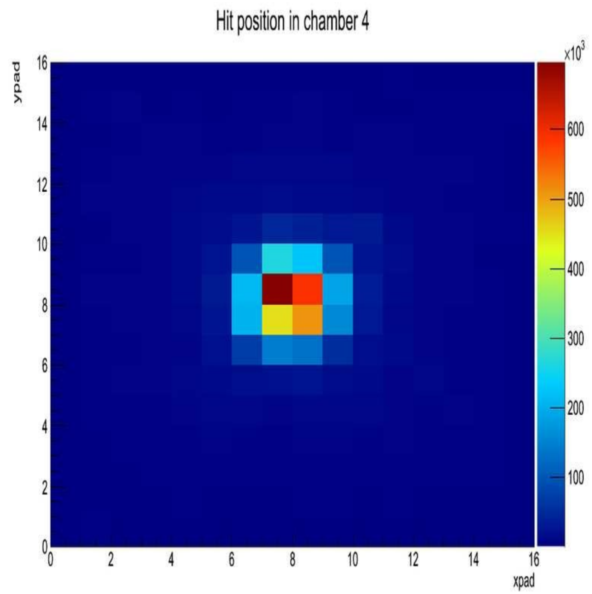
2 resistive ASU sandwiched between 3 non-resistive *(or standard)*

Standard prototypes have diodes on PCB, resistive ones do not.

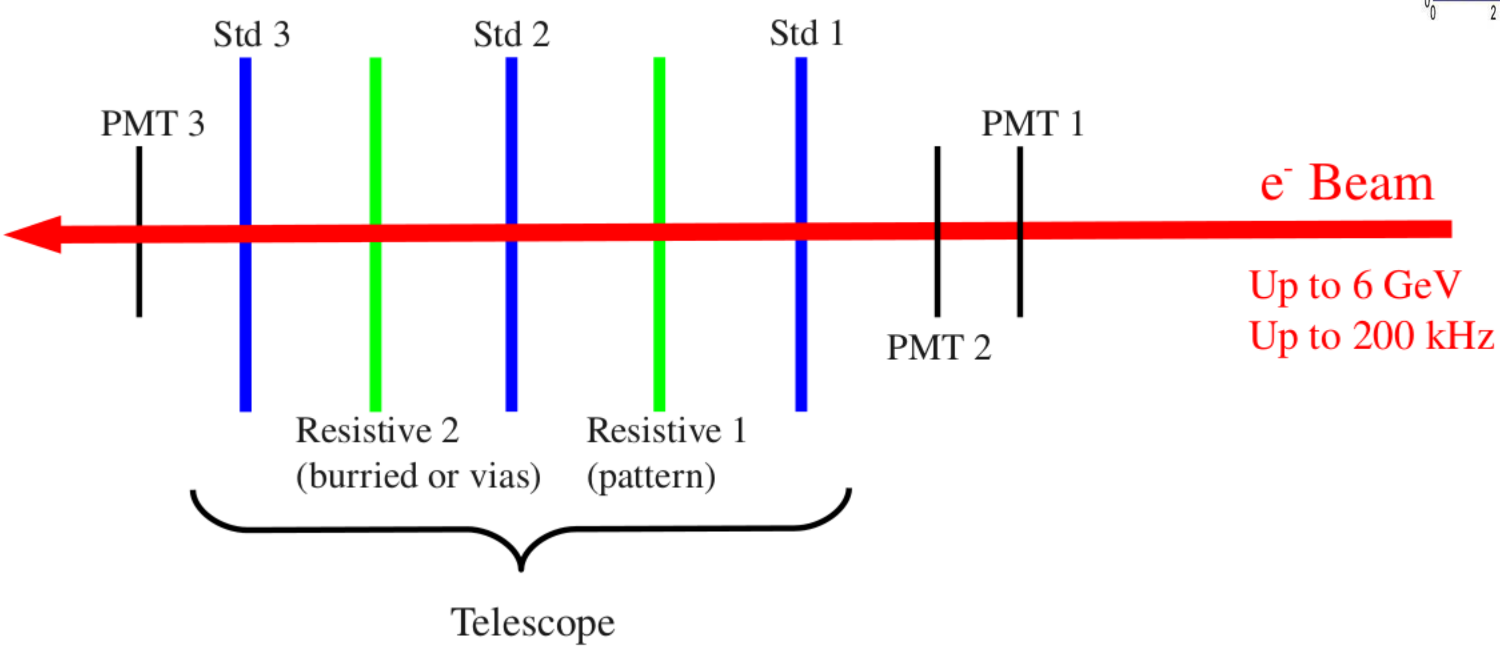




Testbeam setup @ DESY



Setup :
3 standards & 3 resistive chambers
Ar/CO_2 gas mixture
Intermediate CALICE DAQ system
Software : LAPP based (Labview, C++ framework)



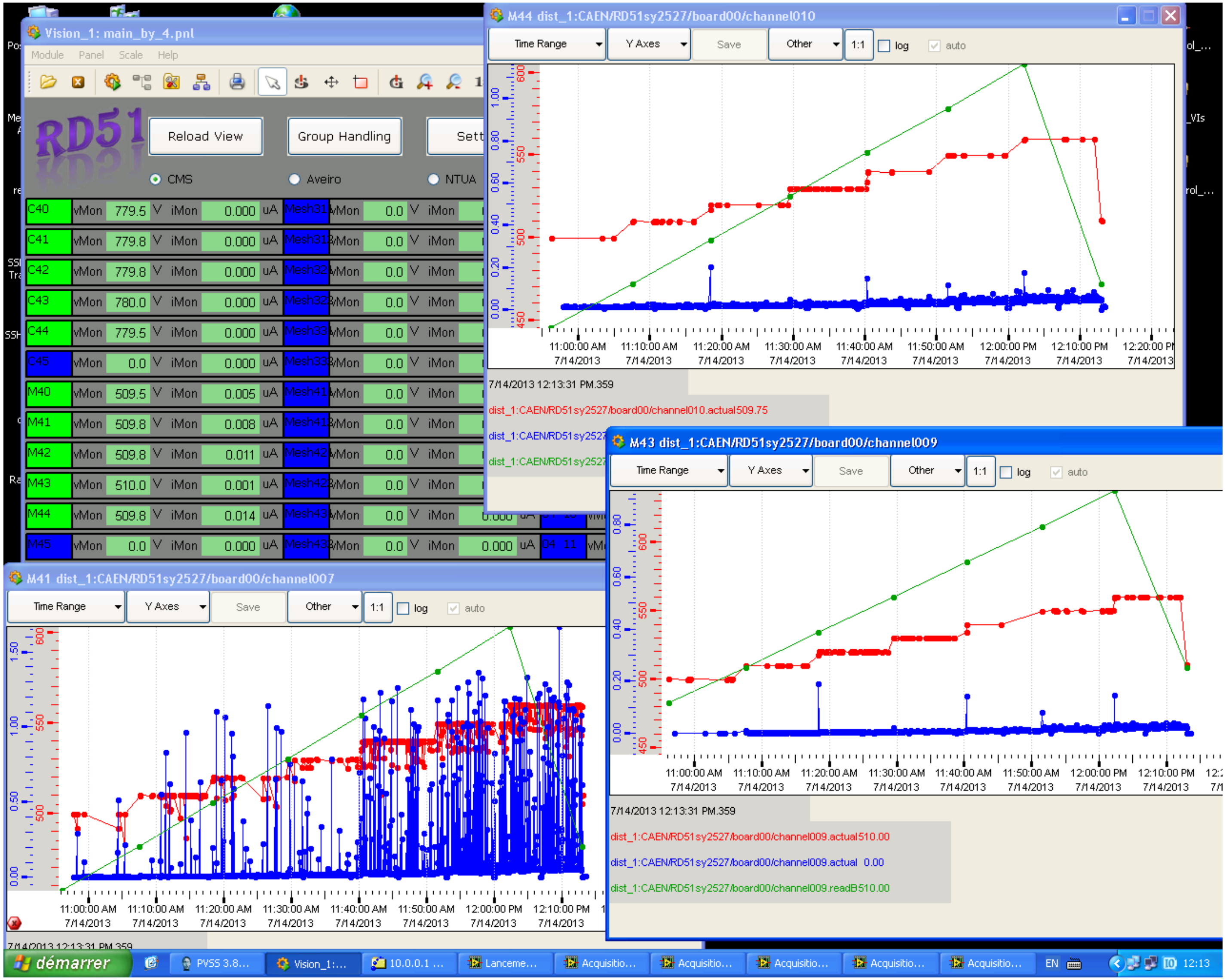
MICROROC data = hits above 1 of the 3 readout thresholds

Possibility of a slow analogue readout (digitisation on readout board)

Mesh current VS voltage at high rate, no sparks in R-prototypes

Gas gain varies between 1000 to 5000 (500-560 V)

Erratum previous RD51 presentation: the rate is not 5 kHz but ~ 180 kHz (over 4 cm^2)



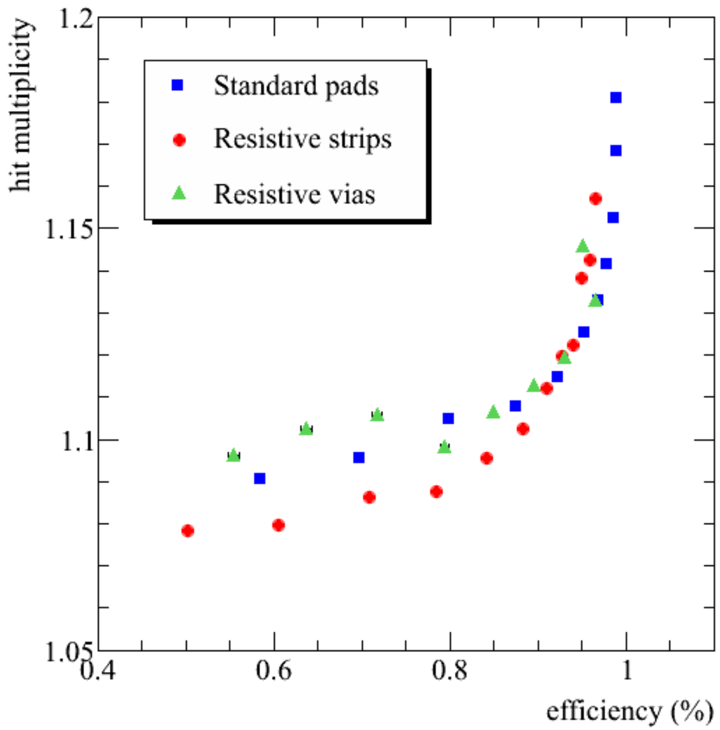
Digital response: efficiency & hit multiplicity

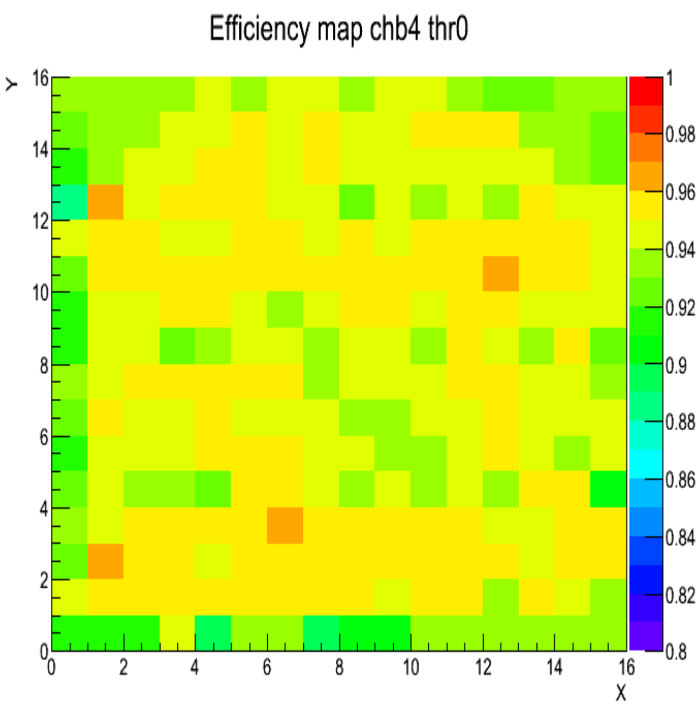
Find tracks in first & last (standard) prototypes

Measure N_{hit} distribution (for every pad) in 2 resistive & 1 standard

→ Standard prototype has largest gas gain (10-20 V more in R-prototypes)
→ *(adjusting V_{mesh}) efficiency & multiplicity are comparable in all prototypes*

→ *Good spatial uniformity (1-2 % RMS)*





Charge-up effects & rate scan (reminder)

Set V_{mesh} to equalise the efficiency (95% efficiency) of R-prototypes

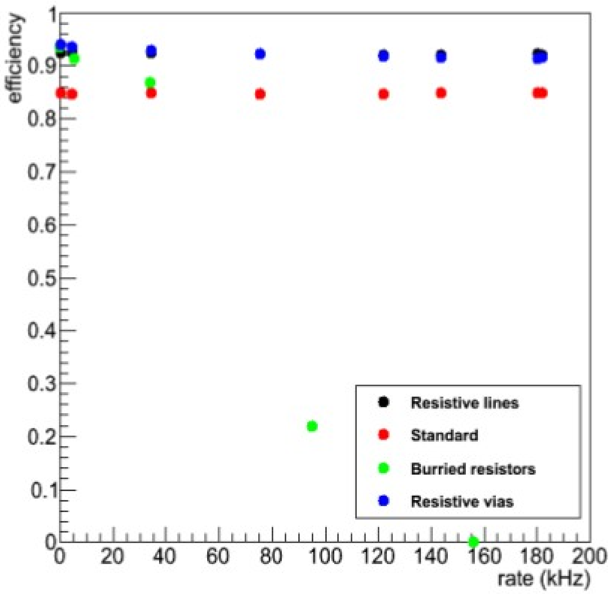
Standard prototypes operated @ lower efficiency (85%) to avoid sparking
(can cause crashes the DAQ because of a modification of slow control inside ASIC)

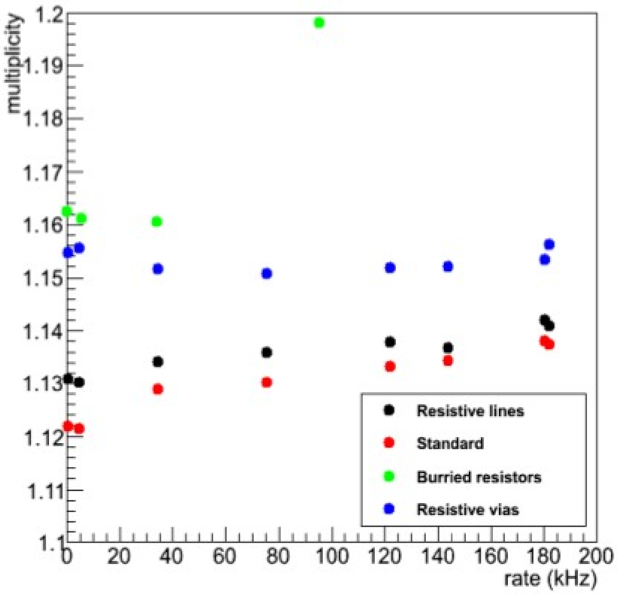
Beam rate is varried between 1-200 kHz (4 cm^2)

→ measure efficiency & multiplicity VS rate

Previous RD51 meeting

Efficiency & multiplicity for low threshold are ~ constant with rate

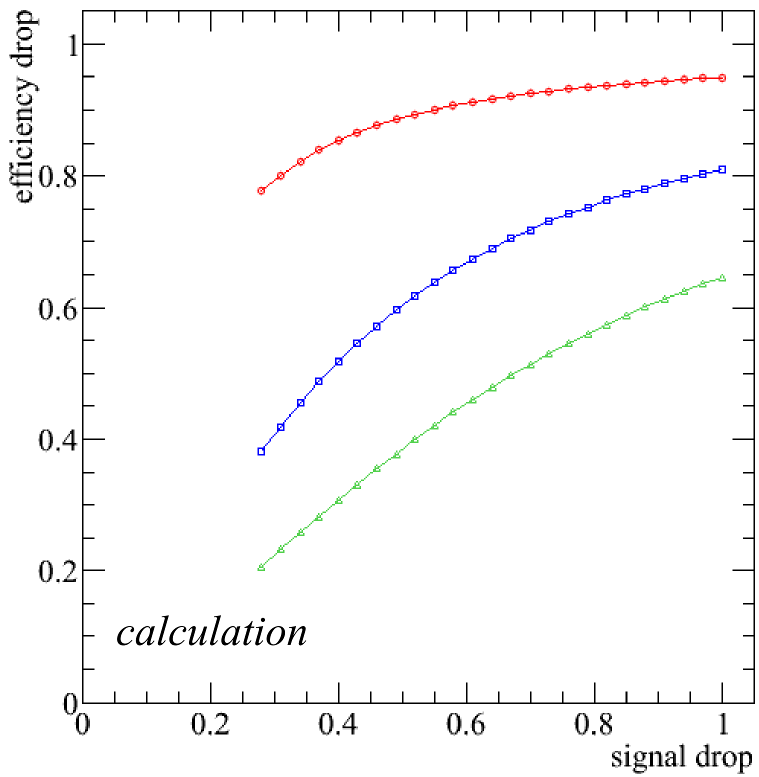




Charge-up effects & rate scan, on-going analysis

For a given variation of signal,

the resulting variation of efficiency depends on the threshold value



Thr = 0.25 MIP

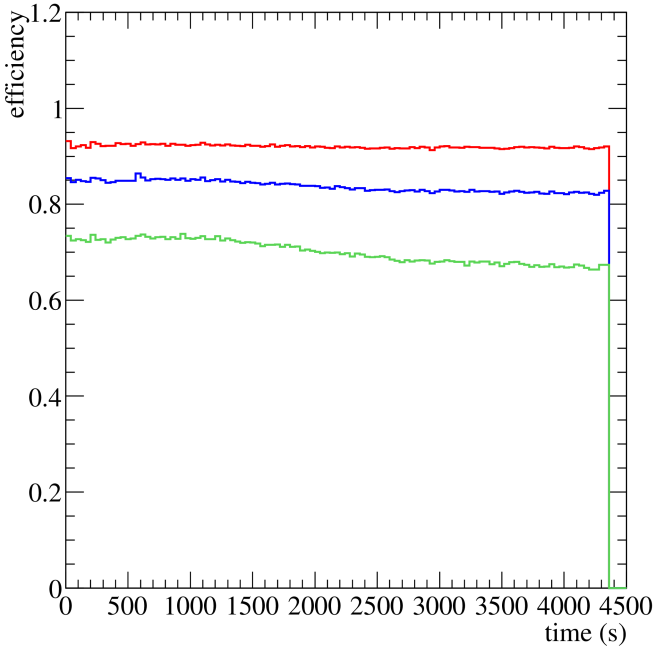
Thr = 0.75 MIP

Thr = 1.3 MIP

→ Look at higher thresholds

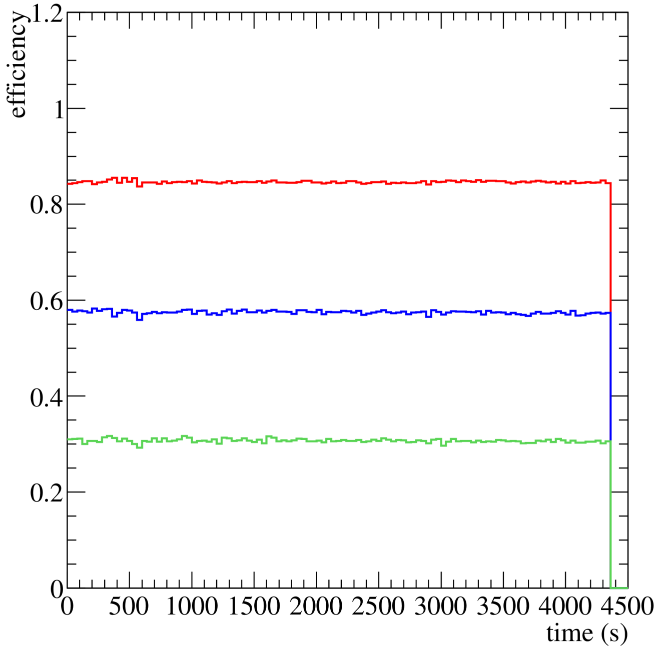
Efficiency versus time for 3 thresholds

Resistive strips



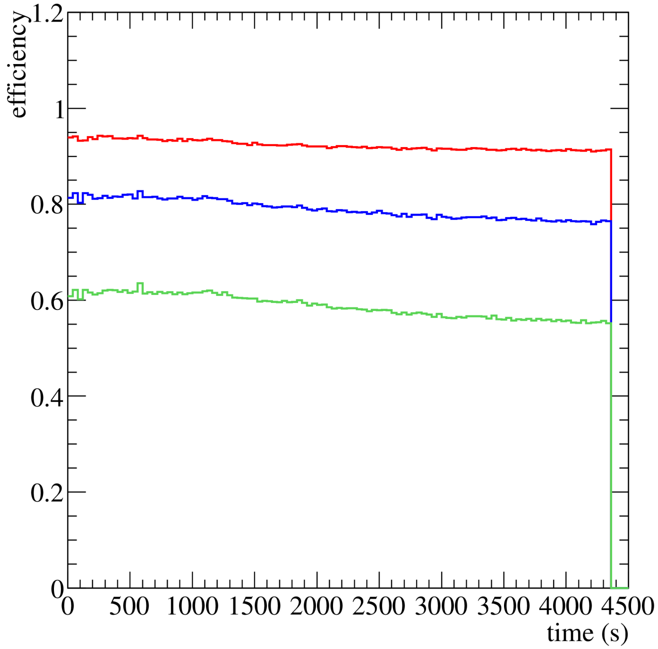
Vmesh = 530 V

Standard



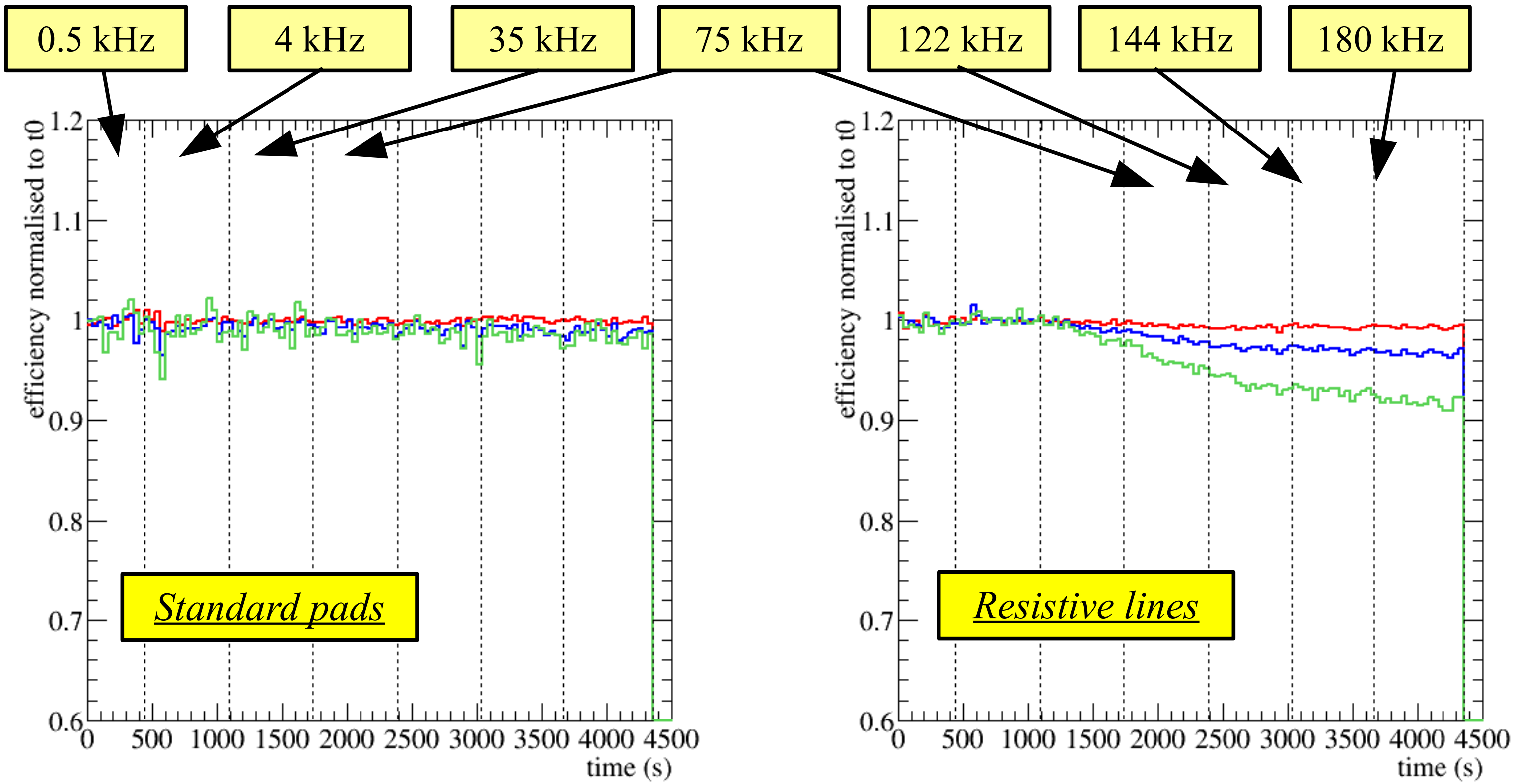
Vmesh = 475 V

Resistive vias



Vmesh = 510 V

Normalised trends, resistive lines

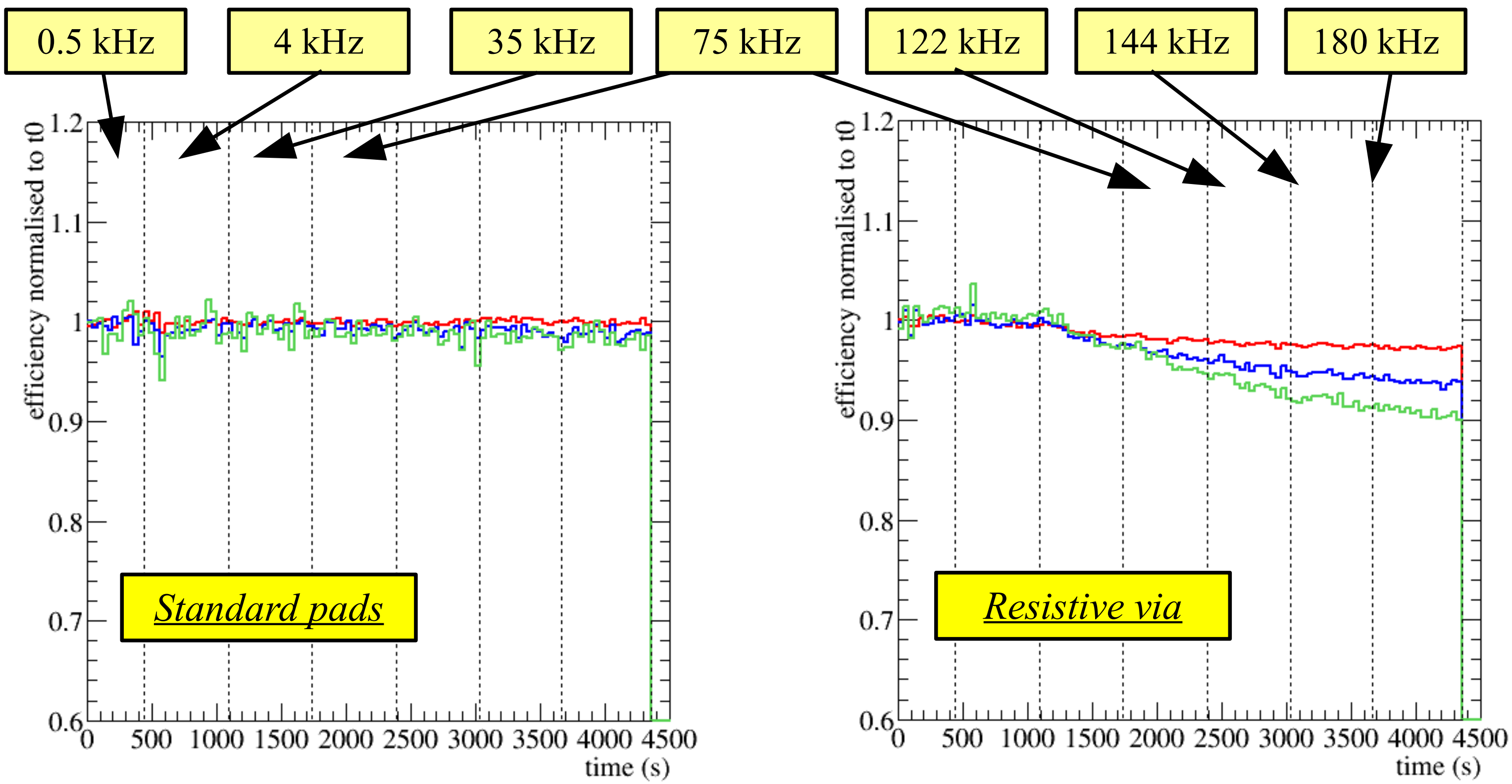


Rate scan

5 GeV e$^-$ beam

Collim. 2x2 cm^2

Normalised trends, resistive via



Rate scan

5 GeV e^- beam

Collim. 2x2 cm^2

Conclusions

- ✗ Spark protection successfully implemented
- ✗ Hit multiplicity still close to 1
- ✗ Charge-up effect, analysis on-going
  - ✗ Effects seems to show up between 1-10 kHz/cm^2
  - ✗ Yet, preliminary results & more work needed
    → direct rate measurement from data in ASIC memory
  - ✗ Understand & model the underlying mechanisms
    before scaling-up the prototype area