Status of SRS + Timepix

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RD51 Collaboration meeting
February 7, CERN

Outline

- Motivation
-
- Timepix chip
- Status at testbeam 2013
- Status now
- Plans for 2014

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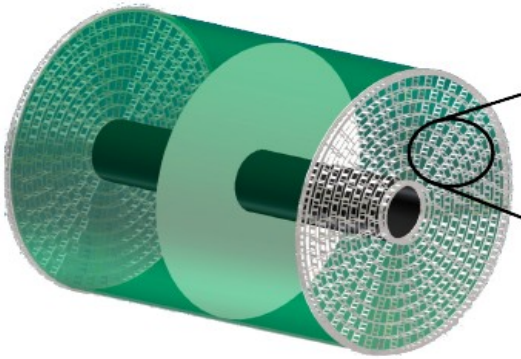
Motivation

Goal: ~100 Chip module for the LCTPC prototype at DESY

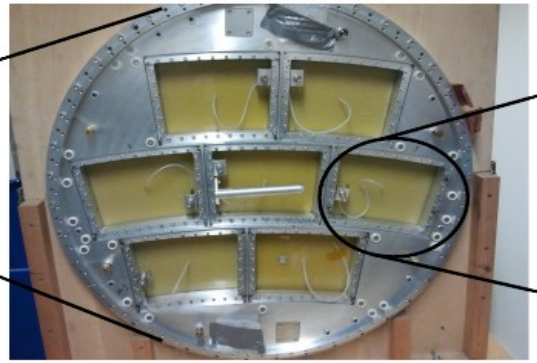
→ channels: 256x256x100 = 6,5 mio

→ demonstrator module for a pixel TPC

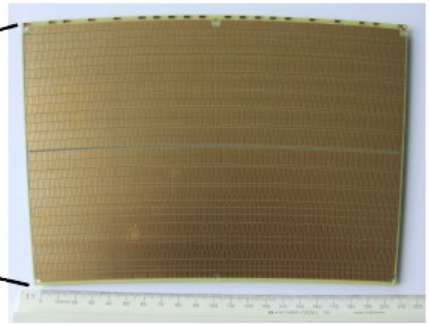
ILD TPC

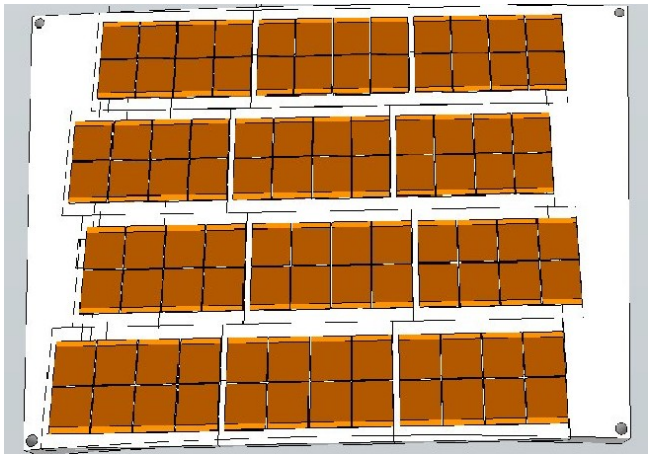


Large Prototype (LP)



Trapezoid Readout Module
(230 mm × 170 mm)





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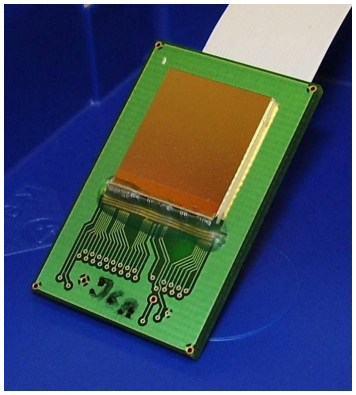
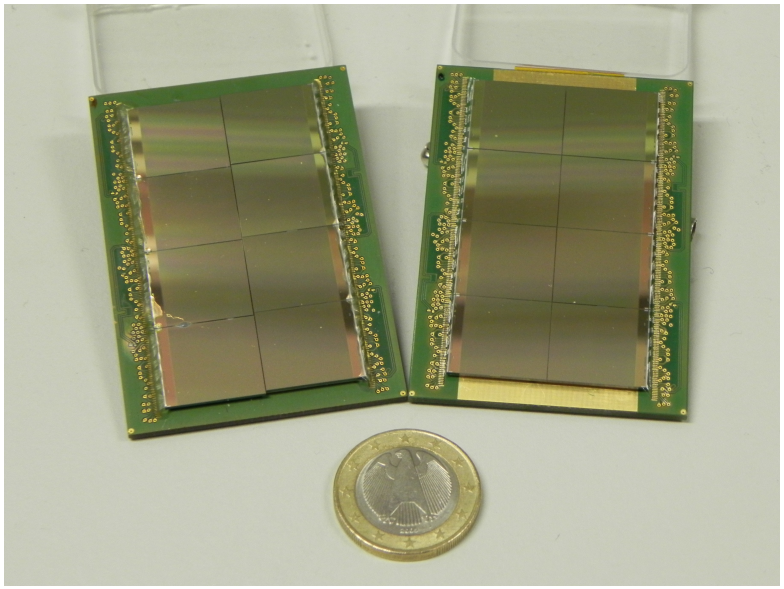
Timepix chip

- Digital readout chip: The Timepix ASIC



- Properties
  - 1.4 x 1.4 cm² active surface
  - 256 x 256 pixel matrix
  - CMOS 250 nm technology, IBM
  - 55 x 55 µm² per pixel
  - amplifier/shaper (t_{rise} ~150 ns)
  - 14 bits count clock cycles
    → Pixel pit when/how long
  - clock up to 100 MHz in every pixel
  - lower threshold
  - threshold level ~ 500 e^- (90 e^- ENC)



- Used as readout anode plane in gaseous detectors

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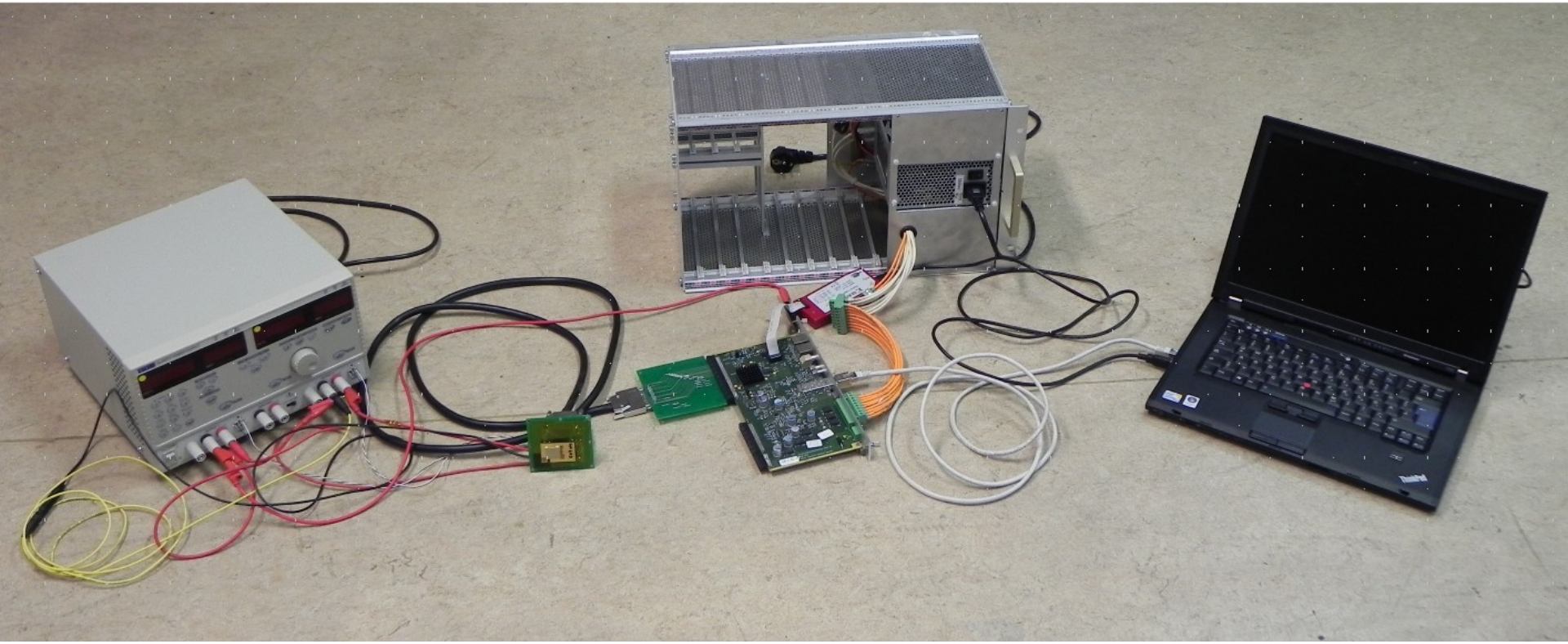
Status at testbeam 2013

- 2 modules, each 8 chips (one InGrid, one triple GEM)

- Readout chain:



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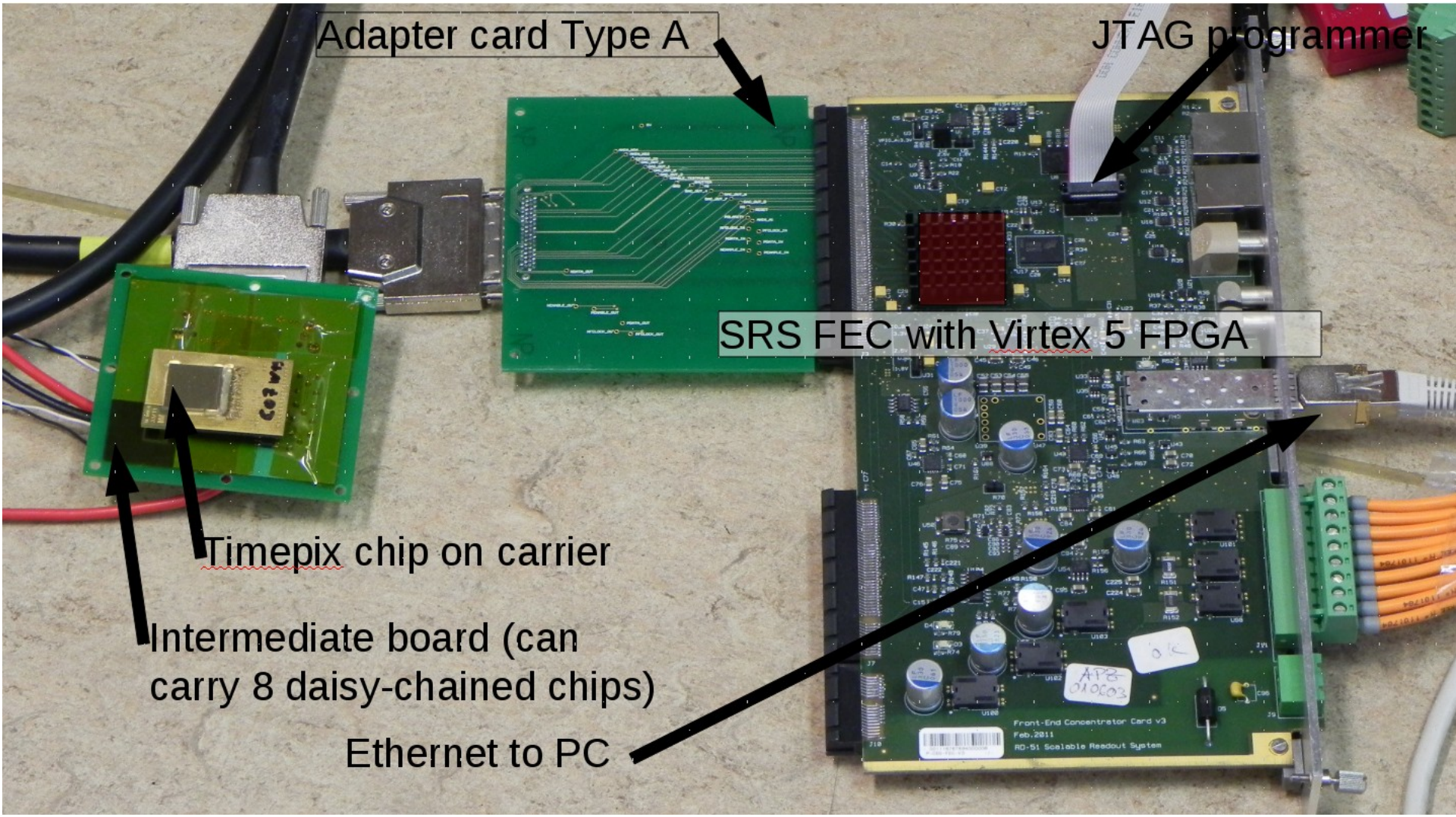
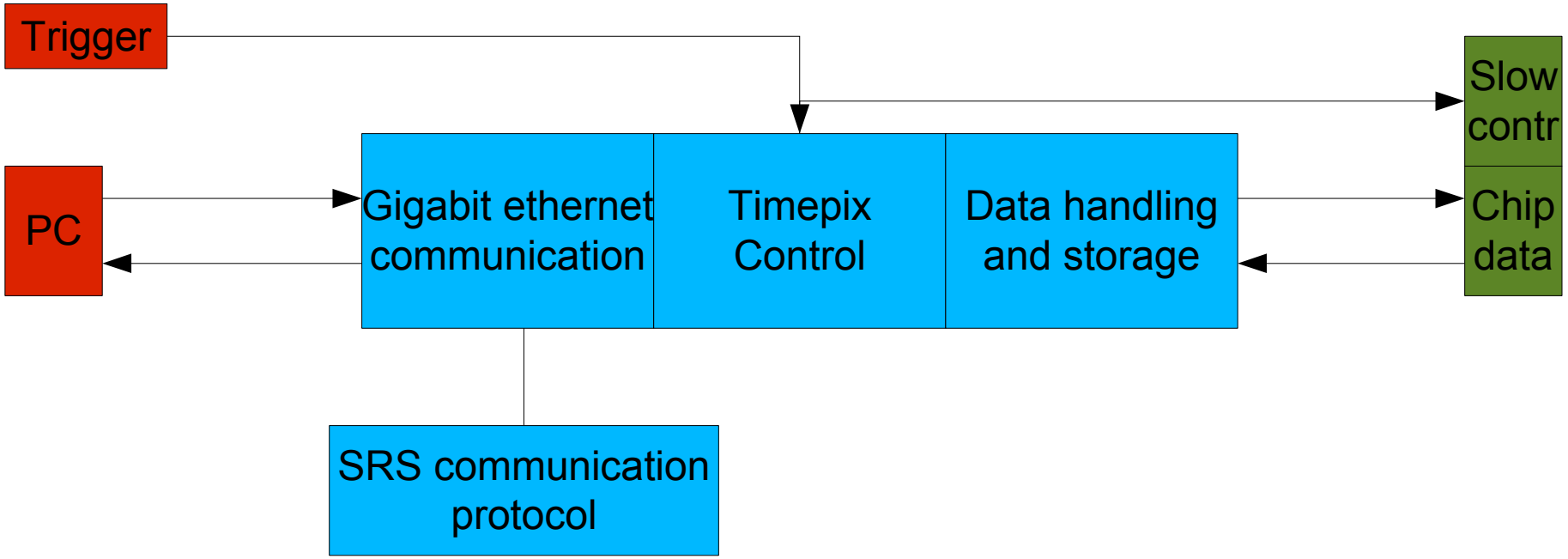
Status at testbeam 2013

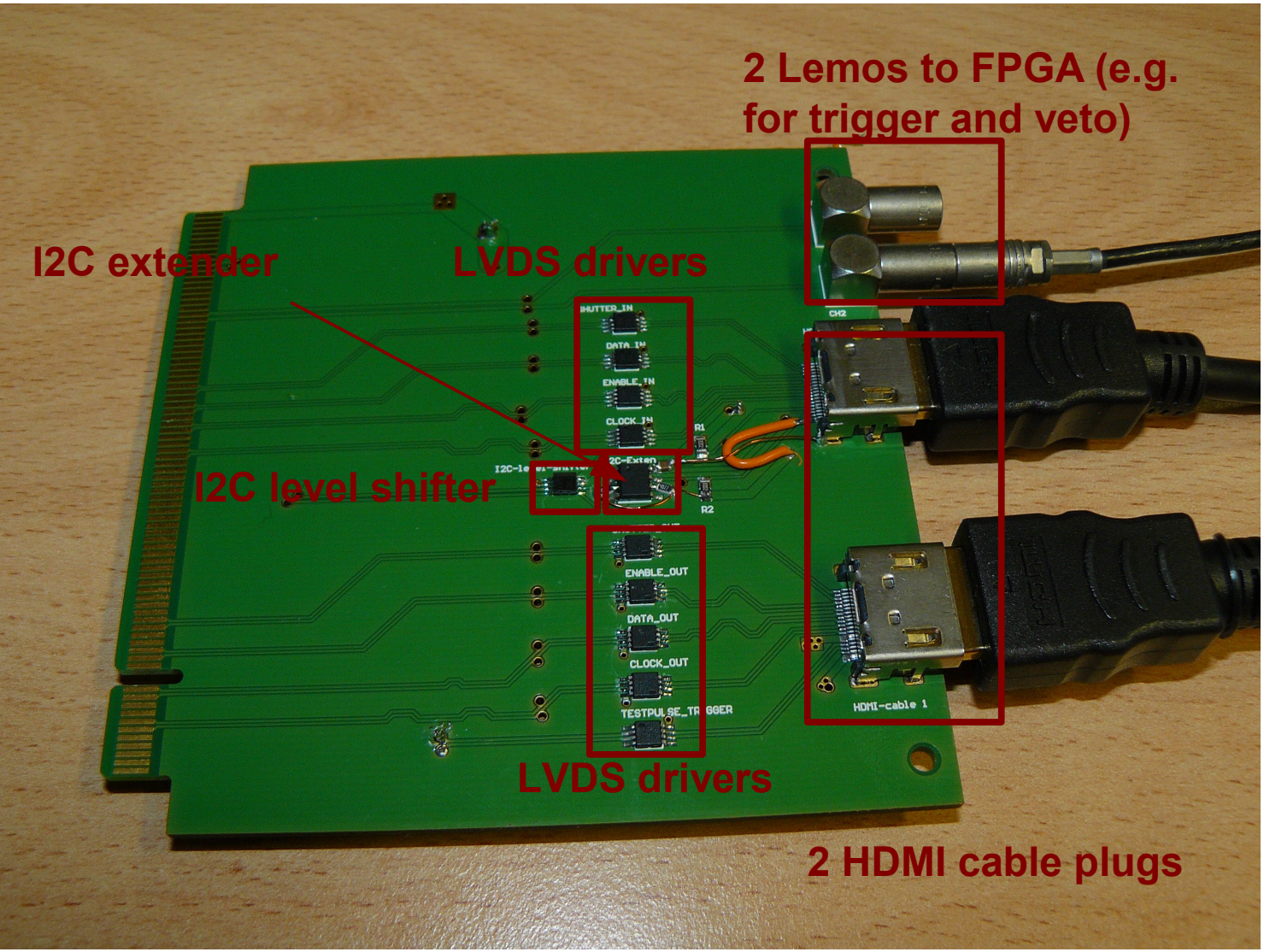
- FEC and simple A Card:



FPGA Firmware



New A Card



I2C: standard for small network.
Signals:
scl: clock
sda: data
Originally between PCBs next to each other.
With externs: Several meters distance.

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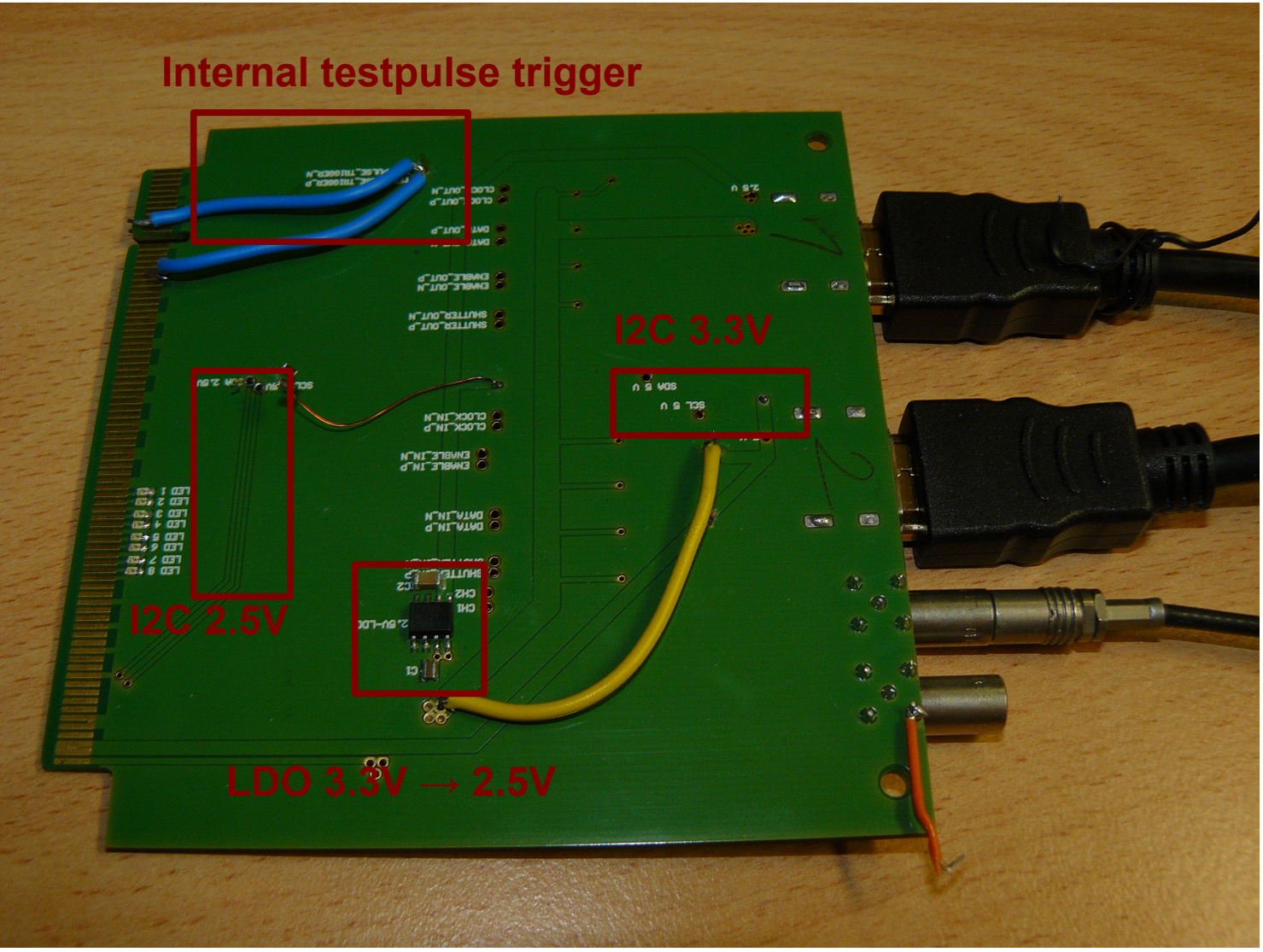
New A Card



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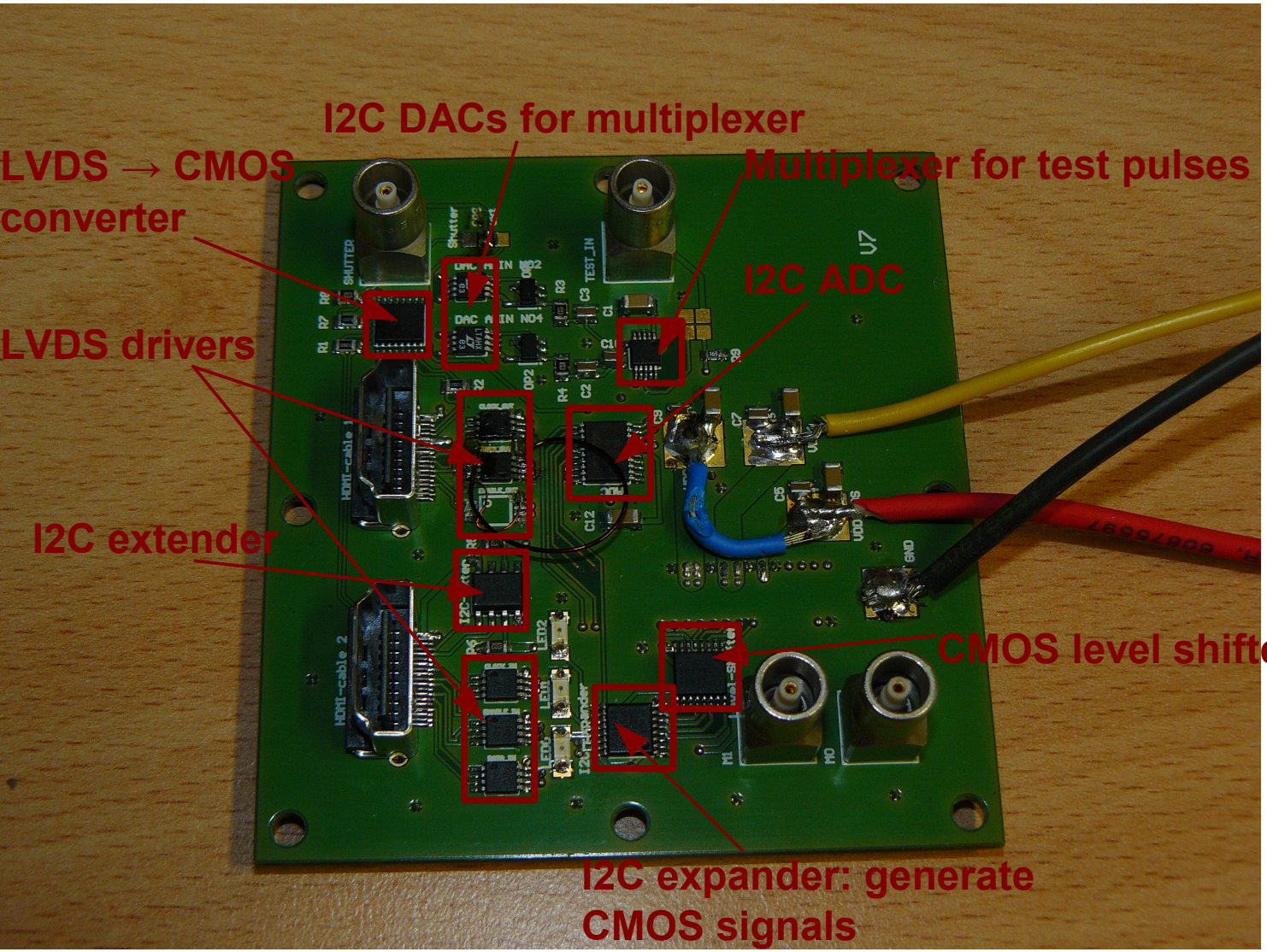
New Intermediate board



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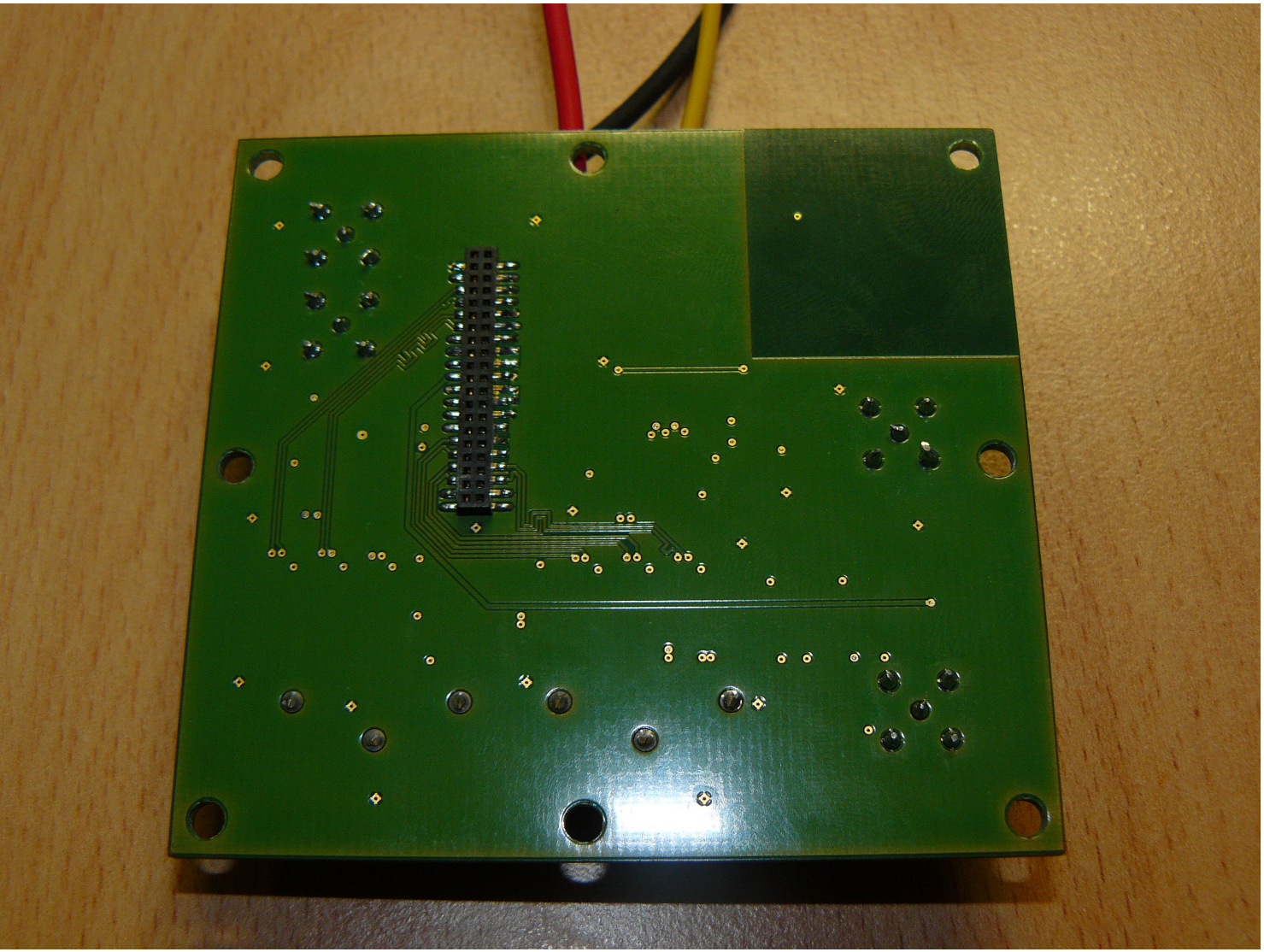
New Intermediate board



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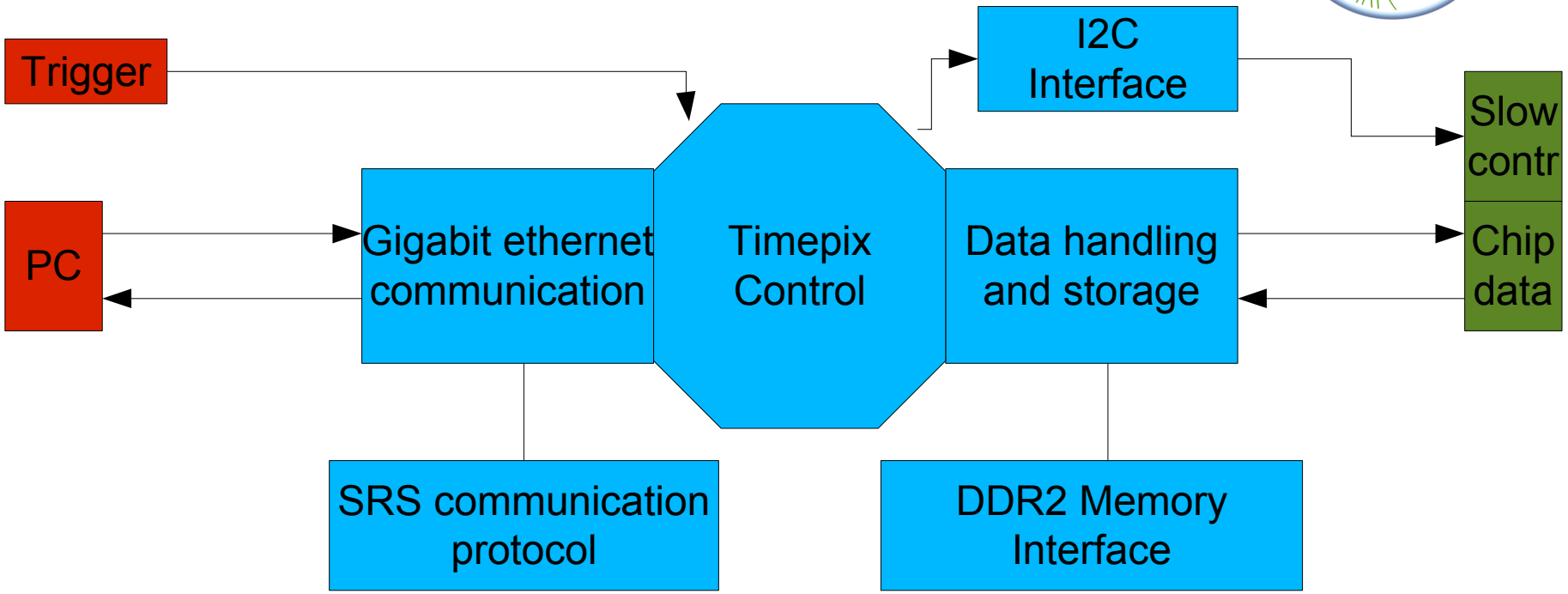
FPGA Firmware



New features:

- ~~Multithreading~~ (read chip while sending data of last frame)
- DDR2 RAM to store data of 8 chips
- I2C for slow control

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Status Timepix+SRS Readout

- New A-Card and intermediate board:
  - HDMI cables
  - Signals optimised for long distance (~25 m)
  - Many new components on A card and intermediate board:
  - LVDS drivers for long distance
  - I2C network for CMOS signal reduction
  - Remaining CMOS signals transmitted as LVDS and converted to CMOS on intermediate board
  - I2C level shifter and extender for long distance
  - ADC to read back analogue signals from Chip (DAC_out)
  - DACs to set voltages for multiplexer
- New parts of FPGA Firmware:
  - I2C Interface
  - DDR2 Interface

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Status Timepix+SRS Readout

- Test of new components ongoing
  - I2C network ok (DACs, ADC, expander work)
  - DDR2 Ram ok, needs long time testing
  - LVDS driver work

    => chip can be operated, setting/reading matrix ok

    data taking ok, even for 8 chips
- Test of FPGA Firmware:
  - DDR2 Ram ok, needs long time testing
  - I2C interface ready
- Software implementation coming (e.g. ADC readout, automatic calibration, ...)

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Plans for 2014

- System for 96 chips
  - Get FECs with V6
  - 12 octoboards
  - 3 or 4 octoboards / FEC
    => check PCI pinout
  - Synchonisation, trigger? Need CTF card?
- Module construction:
  - Space is limited
  - Electronics
  - Low voltage? 12 x 2,2V/4A power supply
  - HV for gas amplification
- Software

  => go to testbeam at the end of 2014

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We can provide soon:

- SRS (A card) with full functionality (for MUROS compatible intermediate board)
  - Users with SRS can plug and play Timepix
  - Users can use MUROS or SRS for same detector
  - Comparability study, documentation
- V6 evaluation board (VHDCI cables MUROS compatible):
  Updated adapter board, I2c network tested
  - ADC, DAC control and readout with i2c (firmware, software)
  - Users with V6 board can plug and play Timepix
    - Users can use MUROS or SRS for same detector
    - Comparability study, documentation:
  - Use in CAST

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Summary and Outlook

SRS + Timepix had a very successful 2013.

SRS + Timepix readout system got new hardware components optimised for test beam.

Preparation of LCTPC module with ~100 chips

- Scaling up of new hardware
- Want: 3-4 Octoboards/FEC
- Power supply still unsolved

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