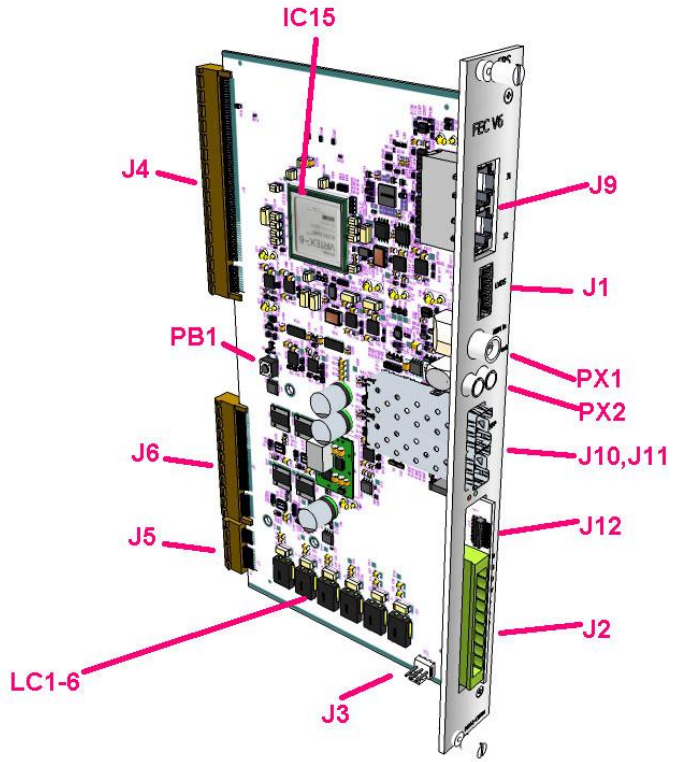
New FEC V6

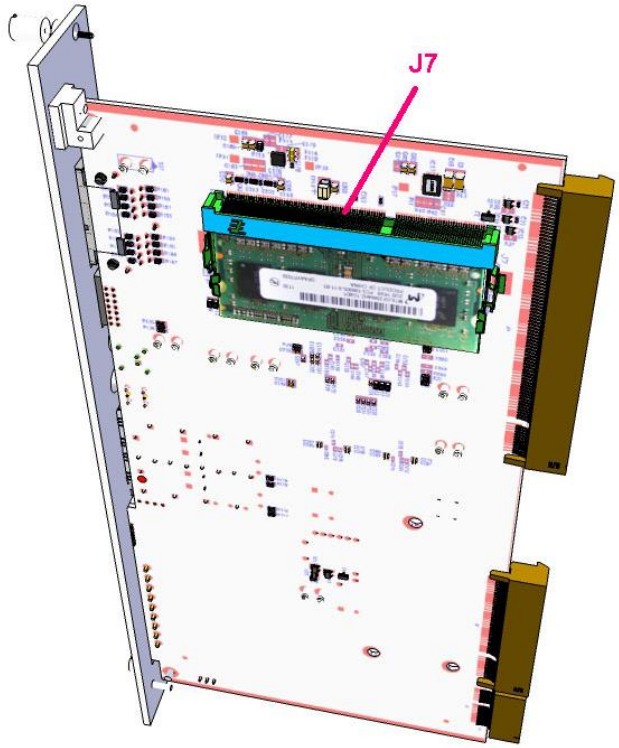
A long story..

Design periods 2013

Schematics:	UPV Valencia
3D component layout	RD51/CERN
12 layer PCB routing:	AES Madrid

Component procurement	RD51/CERN
Front panel	RD51/CERN
PCB mounting:	TELSA Sion
Testing 4 protos:	UPV Valencia

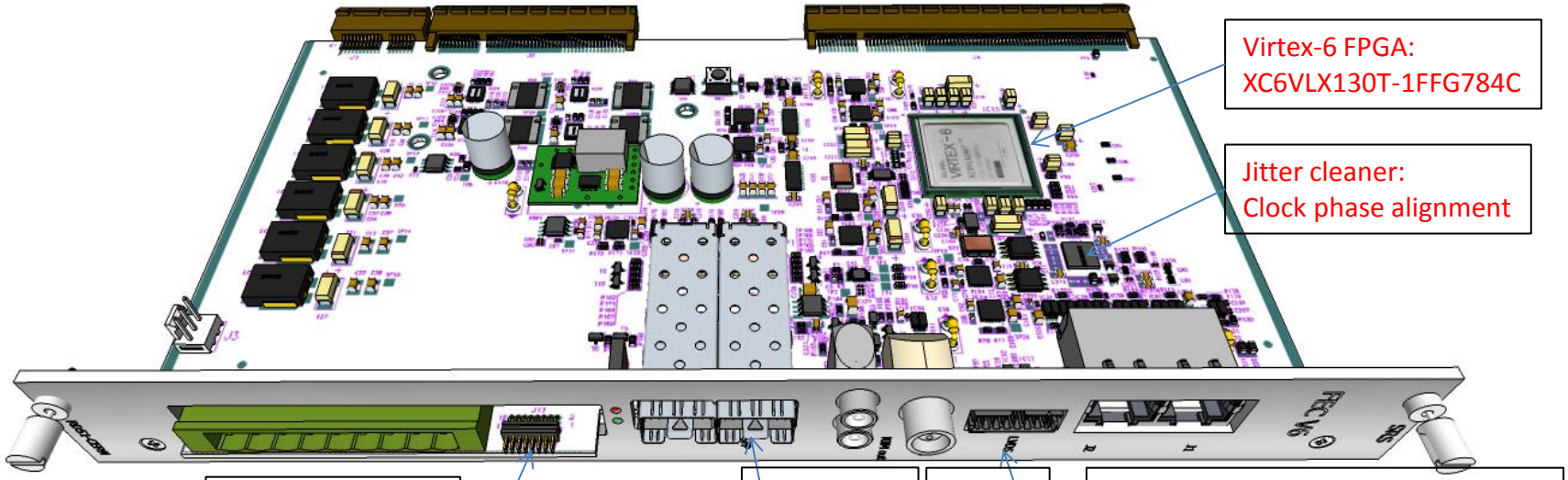




Main motivation for FEC upgrade

- Need more FPGA resources (Zero-supression etc)
- Need 2nd SFP for more flexible architectures
- DDR memory plug in
- Jitter cleaner for precise clock Xmission to SRU
- Additional I/O connector on front panel

Common FEC V6 card



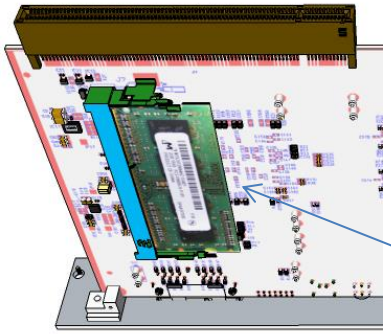
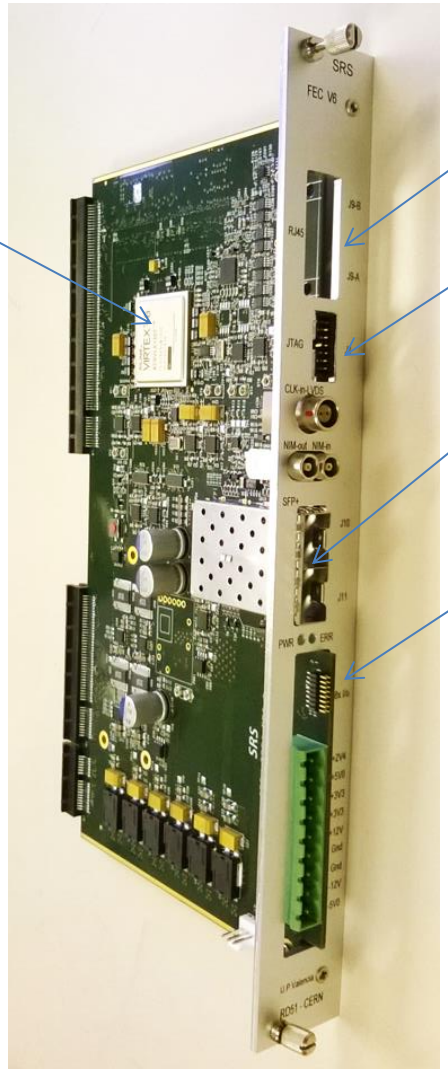


Photo FEC V6

Jan 2014



Virtex 6

Dual RJ45

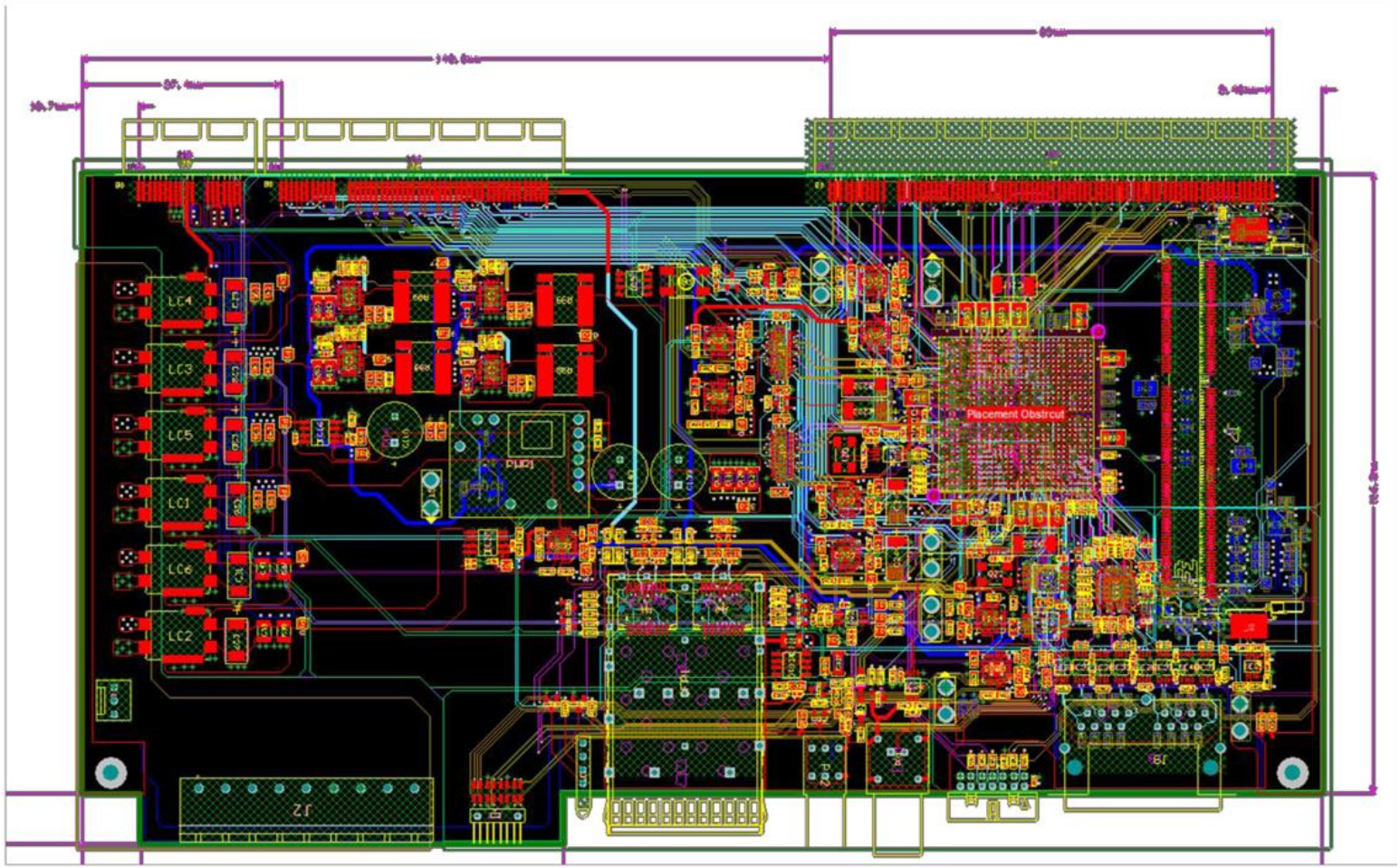
JTAG

Dual SFP+

aux I/O

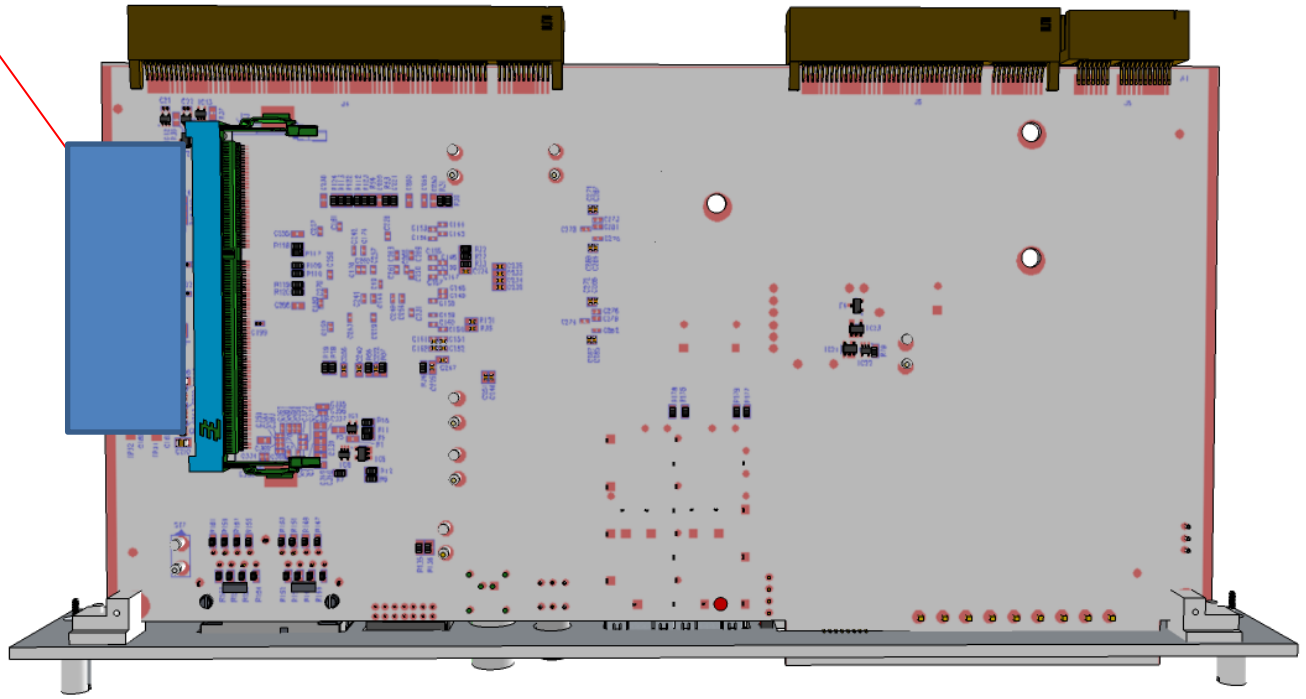
DDR3 plugin

AES 14 layer routing



Several hickups 2013

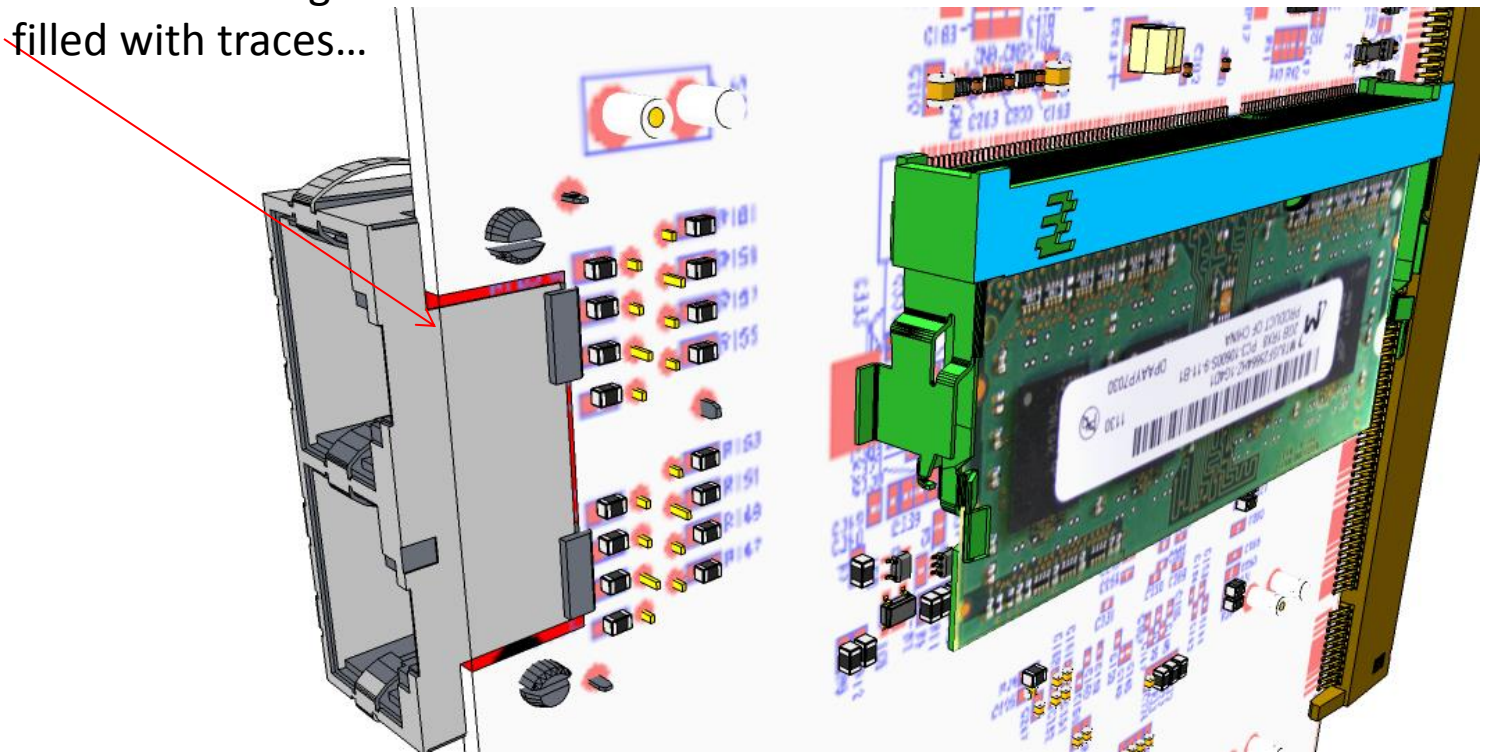
Bari routing 1Q 2013 was not successful until June 2013, complexity too high
June-July 2013 : 3 calls for commercial FEC V6 routing
1st AES layout Aug 2013: DDR3 would hit the crate



This required complete re-routing of critical DDR3 lines, pin swapping ect by UPV
First PCBs and final component list ~ End Nov 2013…
Component procurement and call for PCB layout December 2013

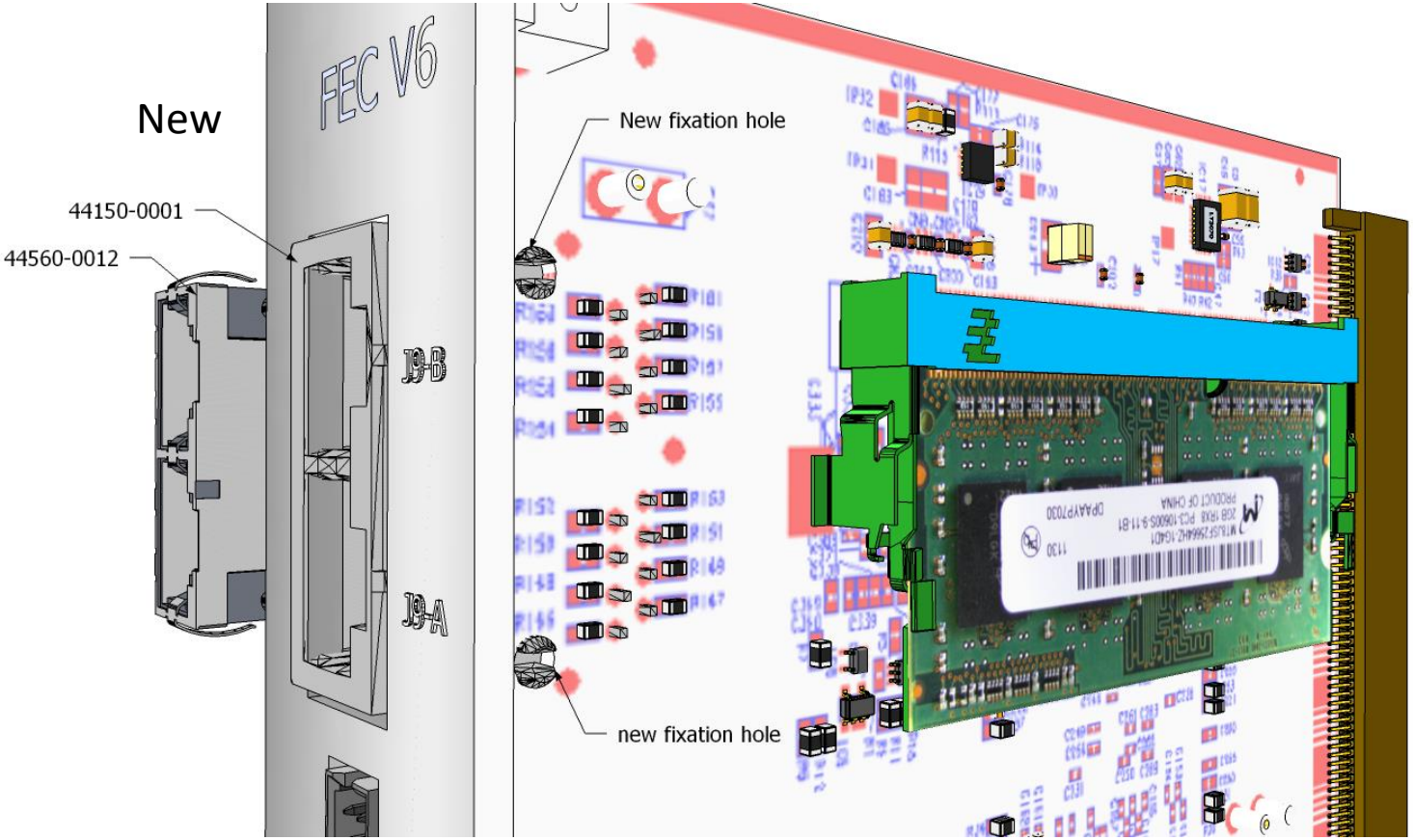
Small hickup 2

RJ45 cutout was forgotten
and filled with traces…



Waiting now for test results….

Fix: change of Rj45 connector modification of frontpanel



Status 2014

- All components and PCBs for 12 FECs @ TELSA
- 4 FEC-V6 prototypes produced
- 8 FEC –V6 still on hold @ TELSA
- 4 cards new at UPV for test , awaiting result
- BOM components revision procurement
- Expect 3-4 weeks after test result

Proto cost

- PCB layout/AES 5 kFs
- PCB's 12 layer NELCO/Lab Circuits 3.6 kFs
- PCB mounting /TELSA 6 kFs
- FPGA's /Silica 5 kFs
- Components /Mouser/Farnell/Digikey 3 kFs
- Front panels 0.2 kFs

- Total prototype cost 12 cards 22.8 kFs

- ➔ Proto cost 1.9 kFs/ FEC V6
- 10kFs contributed from common fund
- **12 x first user cost 1.1 kFs**

General FEC V6 availability

- After proto phase, FEC 6 to replace FEC V3
- PRISMA /CERN store production change
- Expect higher cost than FEC V3 (increased FPGA cost)