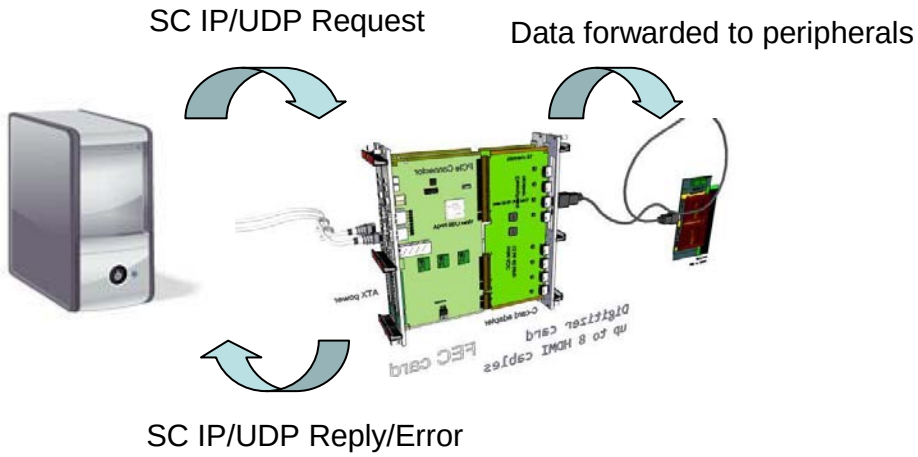
SRS Slow Control Manual

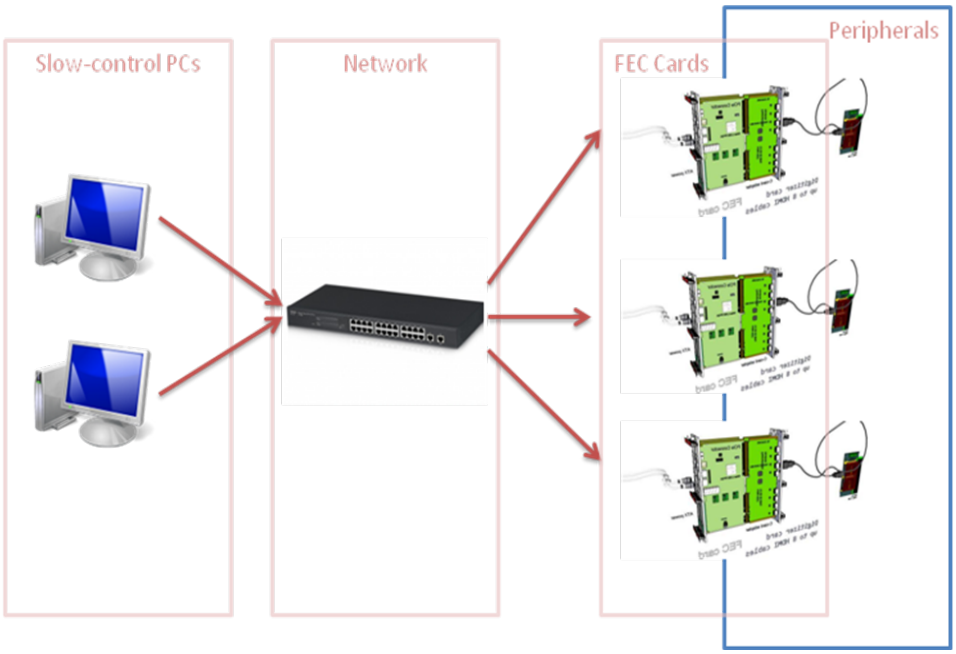
Overview

The slow-control of the SRS system is carried out using UDP over IP protocol on the available Gigabit Ethernet port of the FEC cards. When using a SRU unit to bundle many FEC cards together, the SRU will act as a packet switch, forwarding the slow-control frames to the FEC cards via the DTC links.



The components of the slow-control system are: the slow-control PC (SC-PC), the network (point-to-point connection/network switch/SRU), the FEC card and the peripherals that need to be configured. Peripherals can be either virtual devices (usually residing in the FEC firmware) or real hardware objects which are connected to the FEC FPGA, located on the FEC card, the A/B/C-Module Card or on the front-end hybrids. Generally the real peripherals have a logic interface located in the FEC firmware, which translates the slow-control commands in the format that the external device understands. The slow control protocol assures that, from the user point of view, the real or virtual attribute of a peripheral is transparent.

The slow-control transactions use a request/reply protocol between the SC-PC and the peripherals. The network and the FEC card guarantee the communication between the two. In particular the FEC Card can filter out ill-formed requests and issue error response packets. The reply packets are generated by the peripheral logic and travel back to the IP address which generated the request.



Peripherals

Name	Port (hex)	Port (dec)	Use	I/F type	Description	User level
SYS_PORT	1777	6007	runtime	reg	System registers. Dynamic control of IP address, MAC address, GbE parameters, ...	expert
FEC_BI2C_PORT	1787	6023	debug setup	I2C	Access to the FEC I2C line B. Used to program the on-board EEPROM	expert
APVAPP_PORT	1797	6039	runtime	reg	APV Application registers. APV trigger sequencer and event builder	user
APV_PORT	1877	6263	runtime	I2C	Access to the I2C registers of the APV chip	user
ADCCARD_PORT	1977	6519	runtime	I2C	I2C registers of the ADC CCARD.	user

System Registers (SYS_PORT = 6007)

Subaddress : not used (anything)

Name	Address (hex)	Byte count	Description
VERSION	0	2	Firmware version identifier. Reserved
FPGAMAC_VENDORID	1	3	Local MAC address, vendor identifier part.
FPGAMAC_ID	2	3	Local MAC address, device identifier part.
FPGA_IP	3	4	Local (FEC) IP address
DAQPORT	4	2	UDP port for data transfer
SCPORT	5	2	UDP port for slow-control
FRAMEDLY	6	2	Delay between UDP frames.
TOTFRAMES	7	2	DATE flow-control parameter. *Experimental*
ETHMODE	8	2	Ethernet control register. Reserved
SCMODE	9	2	Slow-control control register. Reserved
DAQ_IP	A	4	DAQ destination IP.
RST_REG	FFFFFFFF	FFFF8000 FFFF0001	Reboot FEC Warm-init

APV Application Registers (port 6039)

Subaddress : not used (anything)

Name	Address (hex)	Byte count	default	Description	Fw. ver.
BCLK_MODE	00	1	b00000111 (0x7)	Controls the trigger sequencer for the APV. See table below for details	
BCLK_TRGBURST	01	1	4	controls how many time slots the APV chip is reading from its memory for each trigger	
BCLK_FREQ	02	2	40000 (0x9C40)	Period of the trigger sequencer.	
BCLK_TRGDELAY	03	2	256 (0x100)	Delay between the external/internal trigger and the APV trigger	
BCLK_TPDELAY	04	2	128 (0x80)	Delay between the external/internal trigger and the APV test-pulse	
BCLK_ROSYNC	05	2	300 (0x12C)	Delay between the external/internal trigger and the start of data recording	
EVBLD_CHMASK	08	2	0xFFFF	Channel mask for the data transmission. Even bits are masters and odd bits are slaves	
EVBLD_DATALENGTH	09	2	3000 (0x0BB8)	Length of the data capture window	
EVBLD_MODE	0A	1	0	Event Builder mode register. Bit 0 = use 32-bit framecounter Bit 1 = use 24-bit timestamp	2.05
EVBLD_EVENTINFOTYPE	0B	1	0	Controls the data format.	
EVBLD_EVENTINFODATA	0C	4	0xAABB0BB8	Data for the optional info-filed in the data format	
RO_ENABLE	0F		0	Readout Enable register (bit 0). Triggers are accepted for acquisition when this bit is 1	2.01
RST_REG	FFFFFFFF			Reset register. Bit 0 = APV sync reset	2.02

BCLK_MODE (address 00) bit description:

Bit	7 - 4	3	2	1	0
Descr.	**reserved**	**TRGIN polarity**	**TRIGGER mode**	**APV Test Pulse**	**APV Reset**
V=0		NIM	Internally generated continuous loop	Test pulse disabled	Disabled. Default for run mode.
V=1		Inverse NIM	External. Controlled by TRGIN	Test pulse enabled	Enabled. Used with the test-pulse.

Example:

3 (b00000011) => continuous loop with test pulse and reset (test mode)

4 (b00000100) => triggered externally, no test-pulse, no reset (running mode - acquisition controlled by external trigger)

BCLK_TRGBURST (address 01)**:** controls how many time slots the APV chip is reading from its memory for each trigger. The formula is **(n + 1) x 3**. Setting this to 4 means a number of 15 time slots. The maximum is 30 time slots (n = 9).

BCLK_FREQ (address 02)**:**

a) (**APVAPP_PORT.BCLK_MODE.TRIGGER_MODE** = 1) When trigger source is set to external this parameter controls the deadtime introduced by the FPGA. After accepting a trigger, the FPGA will ignore all triggers incoming for **Bclk_freq x 64 x 25ns** time. 40000 means 1ms. This time should not be lower than the total acquisition time of one event which is about 222 us (with default parameters).

b) (**APVAPP_PORT.BCLK_MODE.TRIGGER_MODE** = 0) When the trigger source is set to internal this parameter controls the repetition rate of the internal generated trigger.

BCLK_TRGDELAY (address 03)**:** The FPGA delays the trigger for this number of clock-cycles (25ns) until propagating it to the chip. The global latency of the trigger is the difference between **APV_PORT.APV_LATENCY** and **APVAPP_PORT.BCLK_TRGDELAY.**

EVBLD_CHMASK (address 0x08) – Channel mapping:

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HDMI channel	7		6		5		4		3		2		1		0	
Master/Slave	S	M	S	M	S	M	S	M	S	M	S	M	S	M	S	M

<u>ADCCARD registers</u> (ADCCARD_PORT = 6519)

Subaddress: not used (anything)

Name	Address (hex)	Byte count	Description	default
HYBRID_RST_N	00	1	Reset pin for each HDMI channel. Valid low for the APV hybrid.	xFF
PWRDOWN_CH0	01	1	Power-down control of the analog circuitry for the ***master*** path for each HDMI channel	x00
PWRDOWN_CH1	02	1	Power-down control of the analog circuitry for the ***slave*** path for each HDMI channel	x00
EQ_LEVEL_0	03	1	Equalization control (bit 0) for each HDMI channel	x00
EQ_LEVEL_1	04	1	Equalization control (bit 1) for each HDMI channel	x00
TRGOUT_ENABLE	05	1	Enables TRGOUT buffer for each HDMI channel	x00
BCLK_ENABLE	06	1	Enables BCLK buffer for each HDMI channel	xFF

Register Bit:	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Corresponding HDMI channel:	4	5	6	7	0	1	2	3

APV Hybrid Registers (APV_PORT = 6263)

Subaddress:

31 - 24	23 - 16	15 - 8	7 - 0
XX	XX	Channel mask	Device
		HDMI channel mapping:	R R R R R R D D
		4 5 6 7 0 1 2 3	R – Reserved
			PLL 0 0
			Master APV 0 1
			Slave APV 1 0
			Both APVs 1 1

Example: 0xXXXXFF03 => all APVs
0xXXXXFF00 => all PLLs
(X = anything(hex))

Device	Register	r/w	internal address (I2C)	address (hex)	Default value	Default value (hex)	Description
APV	ERROR	r	0000000x	00			SEU or Sync error
APV	MODE	r/w	0000001x	01	b00011001	19	See table below
APV	LATENCY	r/w	0000010x	02	128	80	Trigger latency
APV	MUXGAIN	r/w	0000011x	03	b00000100	04	Gain of the output buffer. One-hot value
APV	IPRE	r/w	0010000x	10	98	62	Preamplifier current
APV	IPCASC	r/w	0010001x	11	52	34	
APV	IPSF	r/w	0010010x	12	34	22	
APV	ISHA	r/w	0010011x	13	34	22	
APV	ISSF	r/w	0010100x	14	34	22	
APV	IPSP	r/w	0010101x	15	55	37	
APV	IMUXIN	r/w	0010110x	16	16	10	Output buffer pedestal control
APV	ICAL	r/w	0011000x	18	100	64	Calibration pulse strength
APV	VPSP	r/w	0011011x	19	40	28	
APV	VFS	r/w	0011010x	1A	60	3C	
APV	VFP	r/w	0011001x	1B	30	1E	
APV	CDRV	r/w	0011100x	1C	b11101111	EF	Calibration channel mask.
APV	CSEL	r/w	0011101x	1D	b11110111	F7	Calibration fine phase (3.125ns). One-hot value

Device	Register	r/w	internal address (I2C)	address (hex)	Default value	Default value (hex)	Description
PLL	CSR1_FINEDELAY	r/w		01	b00100000	20	Bit 3-0: CLK fine-phase adjustment (value ≤ 11) Bit 4: CLK phase flip Bit 5: enables access to TRG_DELAY register
PLL	TRG_DELAY	r/w		03	0	0	Trigger delay (clock cycles)

APV MODE register description:

Bit number	Function	Value = 0	Value = 1
7	Not Used	-	-
6	Not Used	-	-
5	Preamp Polarity	Non-Inverting	Inverting
4	Read-out Frequency	20MHz	40MHz
3	Read-out Mode	Deconvolution	Peak
2	Calibration Inhibit	OFF	ON
1	Trigger Mode	3-sample	1-sample
0	Analogue Bias	OFF	ON

Example:

`00011001 (hex: 19)` => 40 MHz, peak-mode, 3 samples-per-trigger with calibration pulse (test mode)

`00011101 (hex: 1D)` => same, without calibration pulse (running mode)

Appendix A. slow_control Linux program

Usage:

```
./slow_control file.txt
```

Contents of “file.txt”:

```
#IP address
10.0.0.2
#Peripheral port number
6039
#SC-Request Frame Data in 4-byte hex format
##Request ID (MSb = 1)
80000000
##Subaddress
00000000
##Command (Write pairs)
AAAAFFFF
##Command info (undefined)
00000000
##Register address
00000000
##Data to be written
00000004
##Register address
00000001
##Data to be written
00000004
```

…

Appendix B. SDC (Scalable Detector Control) software.

Refer to https://twiki.cern.ch/twiki/bin/view/AtlasPublic/SDC