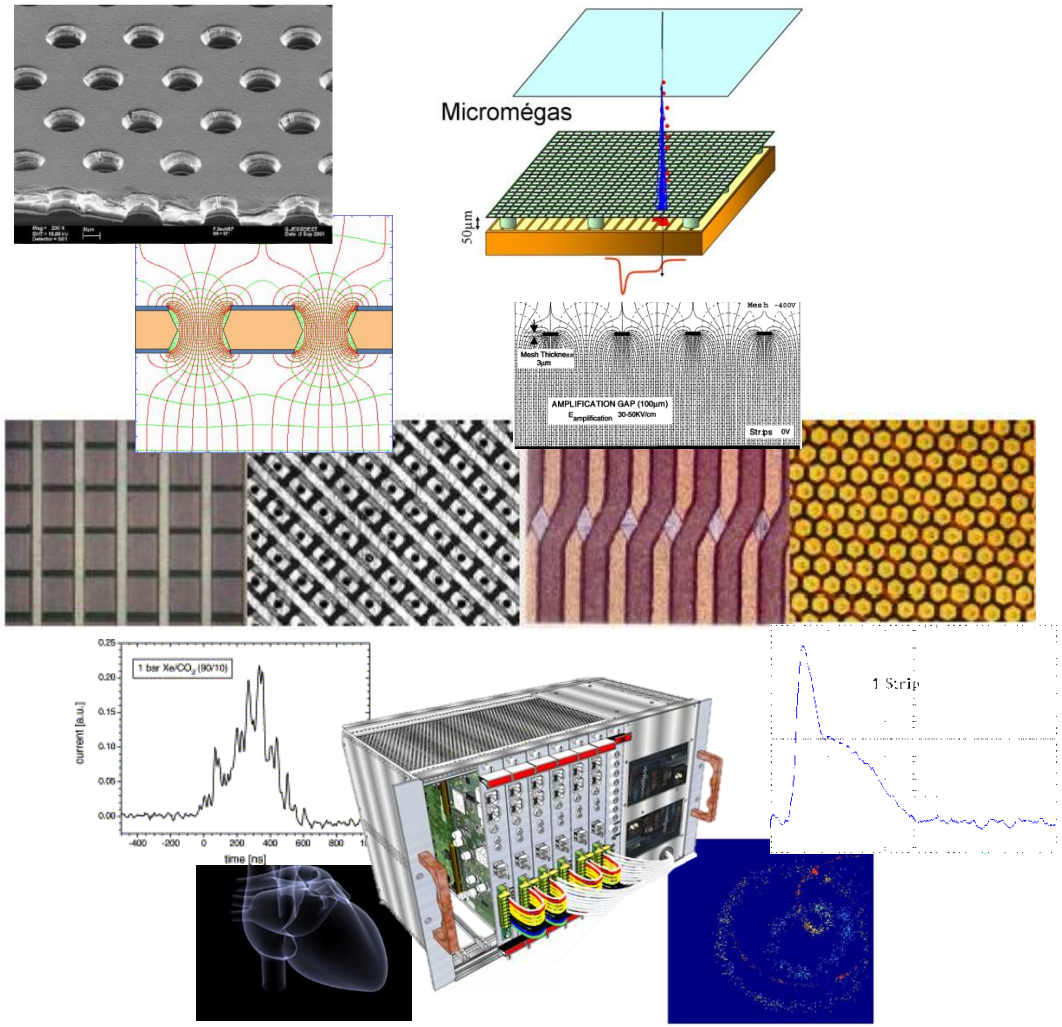
Electronics for Gas Detectors

Sorin Martoiu, CERN

Electronics for Gas Detectors



IONIZATION

DRIFT

MULTIPLICATION

READOUT

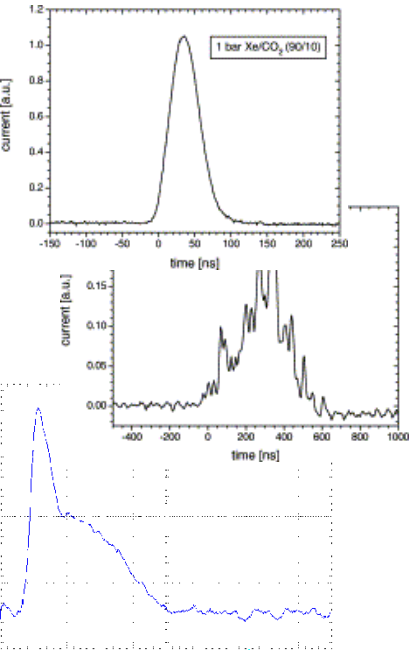
AMPLIFICATION

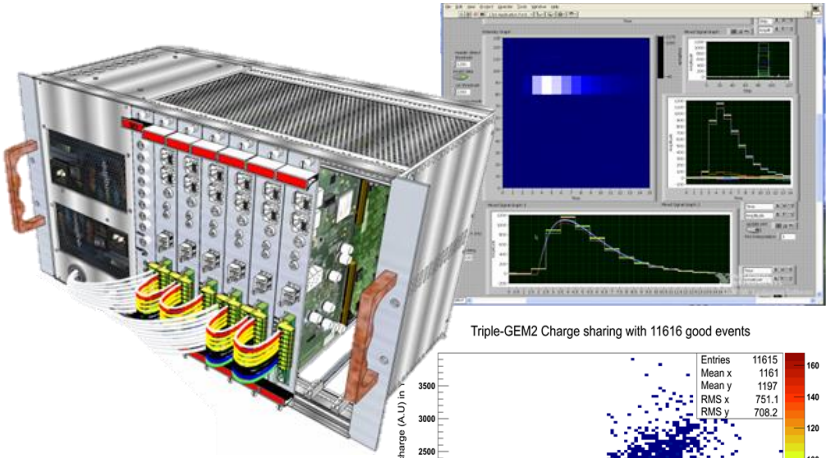
PROCESSING

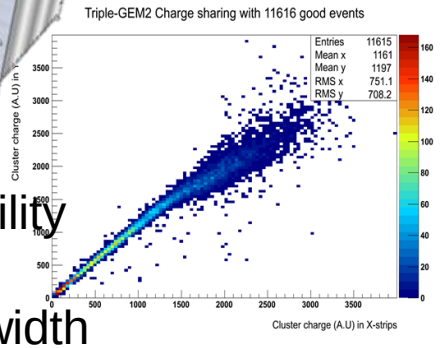
FEATURE EXTRACTION

EVENT CORRELATION

Electronics for Gas Detectors





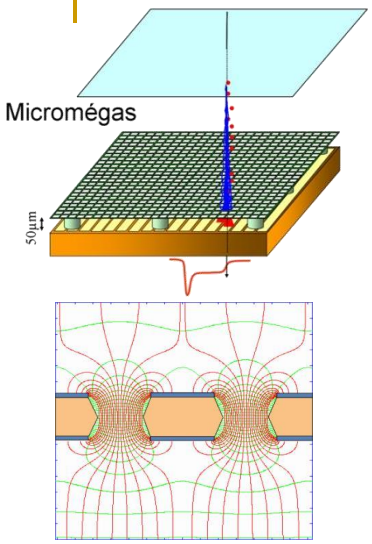


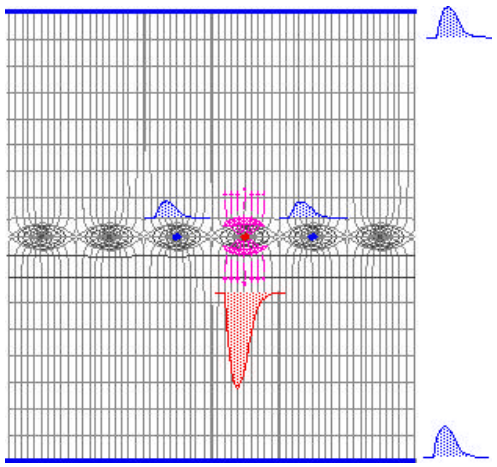
- Low noise *(0.1 ~ 1 ke)*
- High channel count *(up to millions of ch)*
- Discharge protection
- Radiation hardness

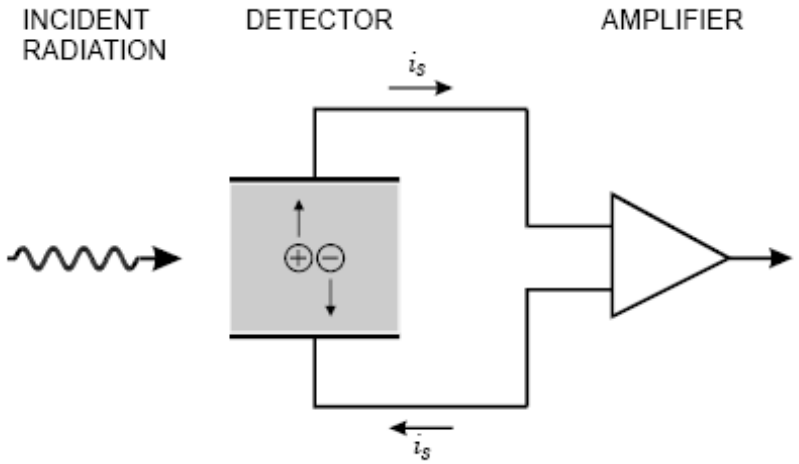
- signal range = 10 .. 1000 ke-
- signal width = 5 .. 200ns
- negative or positive polarity
- …

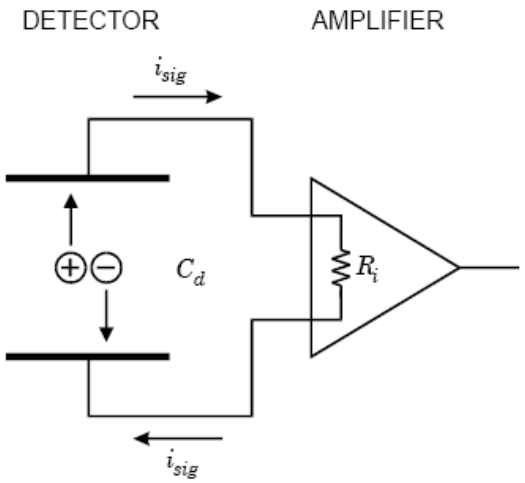
- Rate capability
- Efficiency
- Data Bandwidth

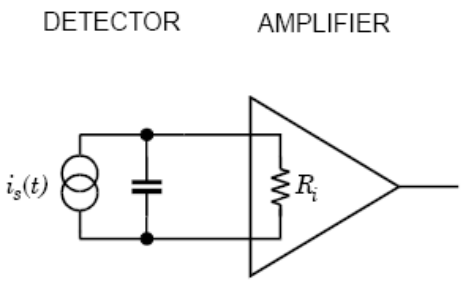
- Spatial resolution
- Temporal resolution
- Energy resolution

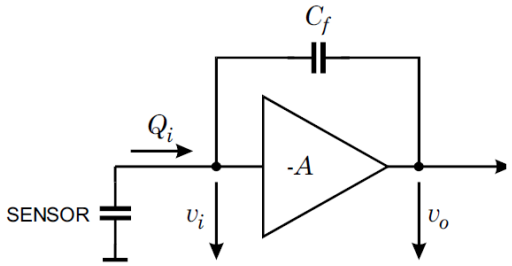






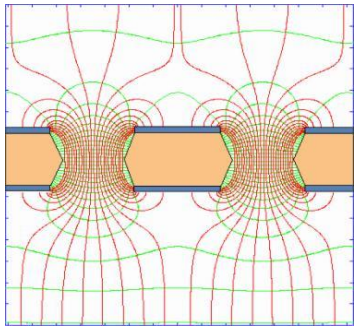


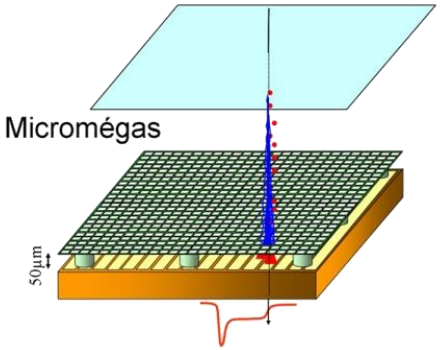


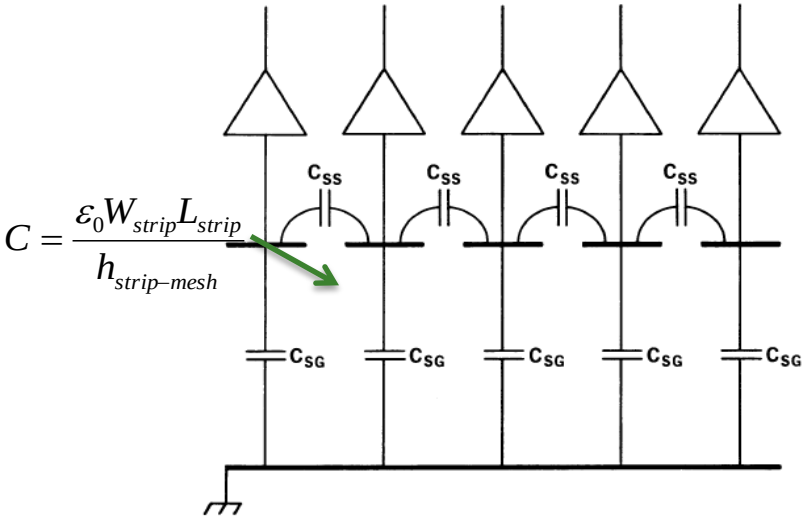


$$C_i = \frac{Q_i}{v_i} = C_f(A+1)\,.$$

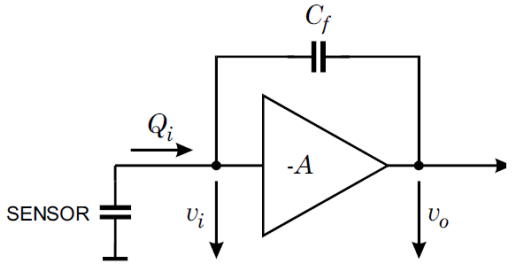
Parasitic Capacitances





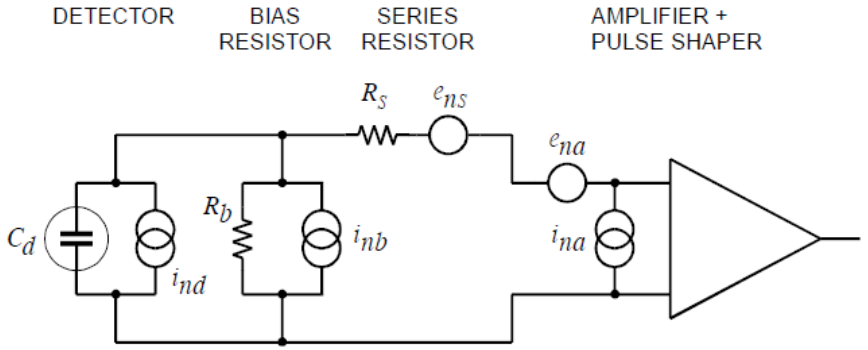


~ 0.1..1 pF/cm



$$C_i = \frac{Q_i}{v_i} = C_f(A+1).$$

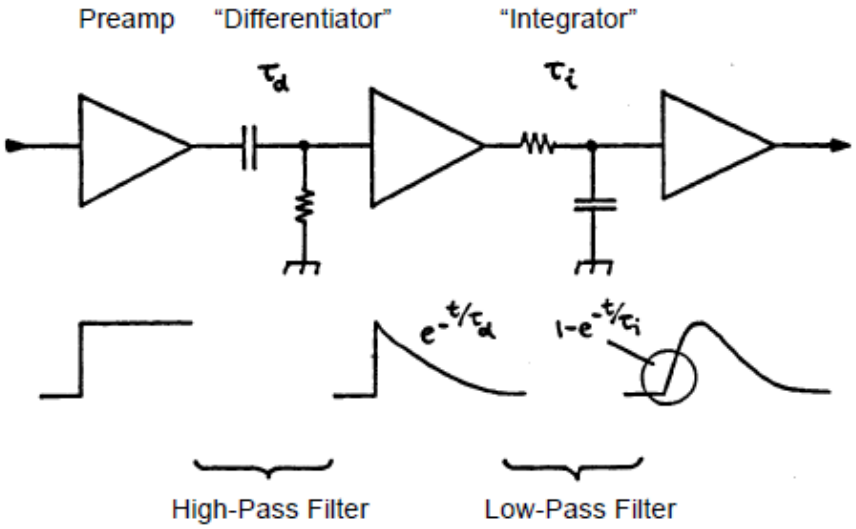
Noise



shunt resistance: $i_{nb}^2 = \frac{4kT}{R_b}$

series resistance: $e_{ns}^2 = 4kTR_s$

amplifier: e_{na}, i_{na}



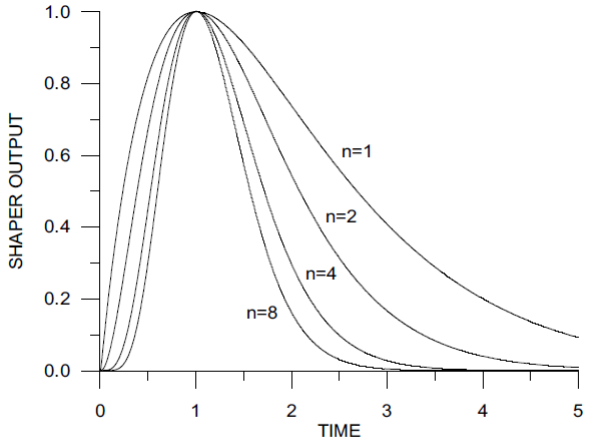
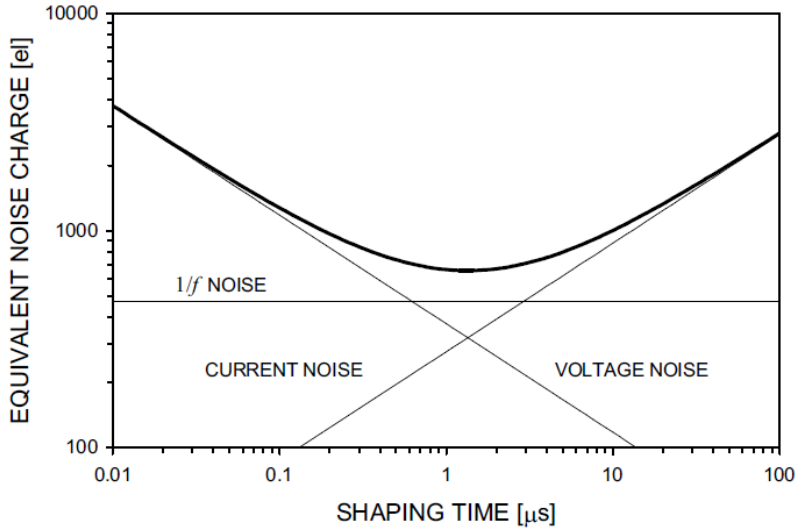


FIGURE 19. Pulse shape vs. number of integrators in a *CR-nRC* shaper

Noise Optimization

$$Q_n^2 = \left(\frac{e^2}{8}\right)\left[\left(2q_e I_b + \frac{4kT}{R_P}\right)\cdot\tau + \left(4kTR_S + v_{na}^2\right)\cdot\frac{C_D^2}{\tau} + 4A_f C_D^2\right]$$

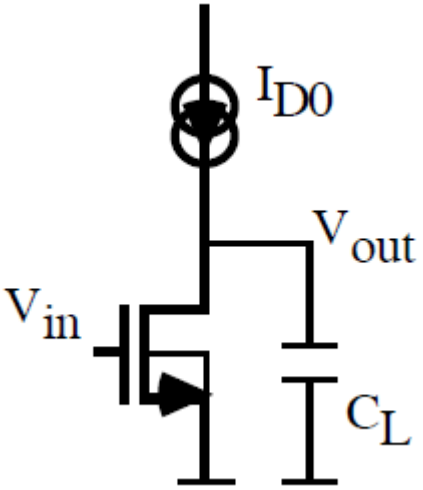
current noise	voltage noise	$1/f$ noise
$\propto \tau$	$\propto 1/\tau$	independent
independent of C_D	$\propto C_D^2$	of τ
		$\propto C_D^2$



MOS Preamplifier Example

$$ENC^2 = i_n{}^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

Shaper coefficients



$$i_{nb}^2 = \frac{4kT}{R_{bias}}$$

Bias resistor + bleeder …

$$S_w = \frac{8}{3}\frac{kT}{g_m}$$

MOS transconductance

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}$$

$$\frac{S_f}{f} = \frac{K_f}{C_{ox}^2 W L f}$$

Technology parameters

$$e_n^2 = S_w + \frac{S_f}{f}$$

Power consumption

Current Noise

detector capacitance

$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

shaping time

White Noise

1/f Noise

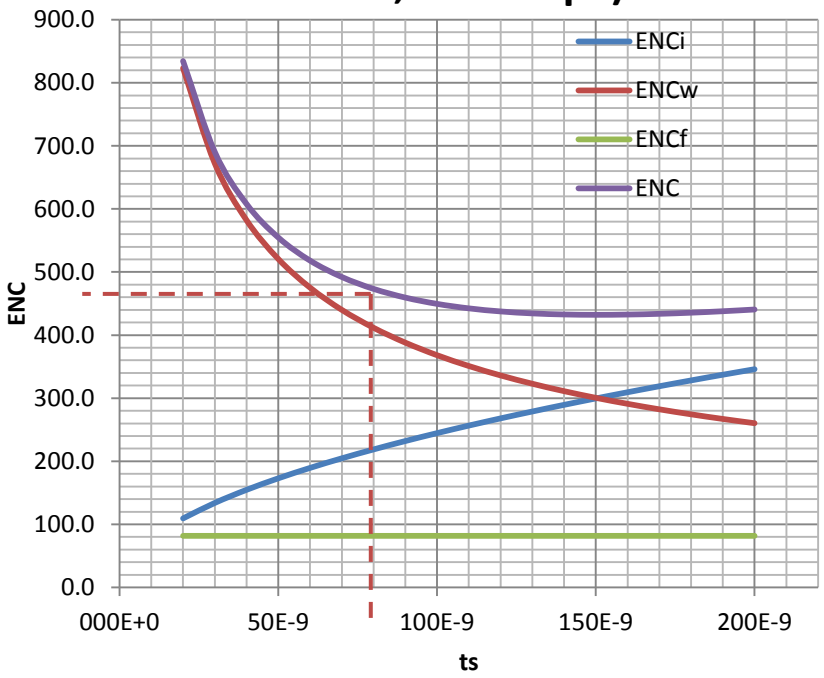
$$S_w = \frac{8}{3}\frac{KT}{g_m}$$

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}$$

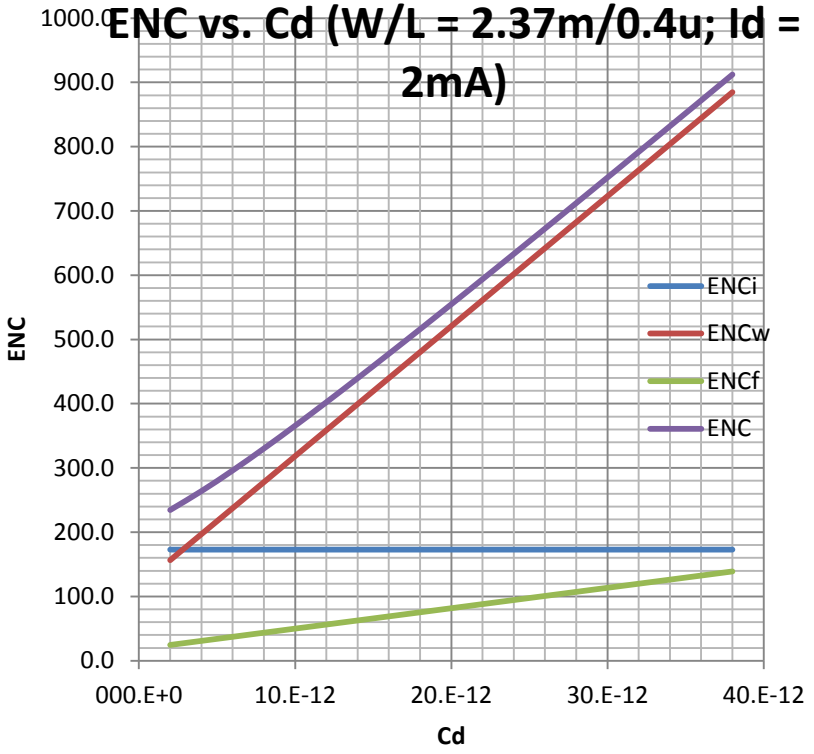
Noise increases with detector capacitance

** TSMC 0.35um data from the web*

ENC vs. Ts (W/L = 2.37m/0.4u; Id = 2m; Cd = 20pF)



ENC vs. Cd (W/L = 2.37m/0.4u; Id = 2mA)



Current Noise

detector capacitance

$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

shaping time

White Noise

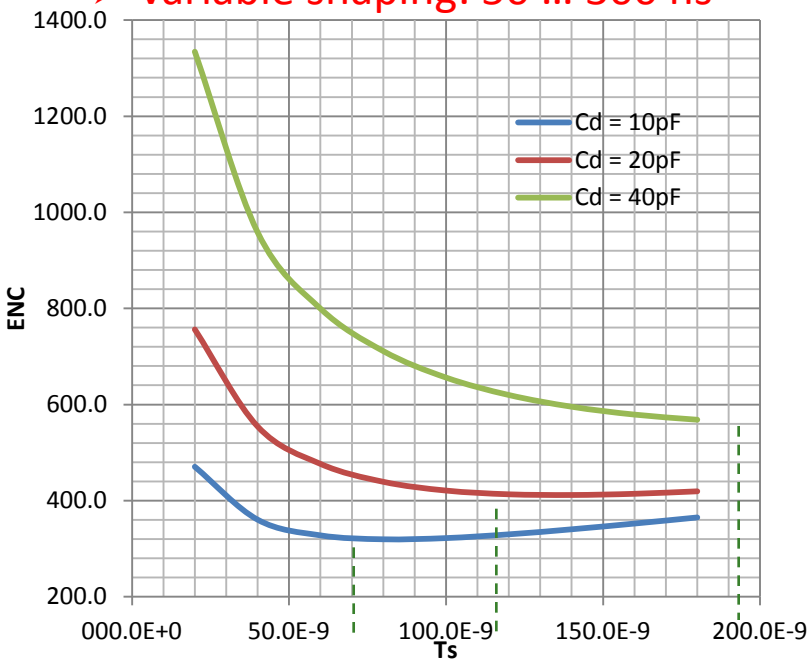
1/f Noise

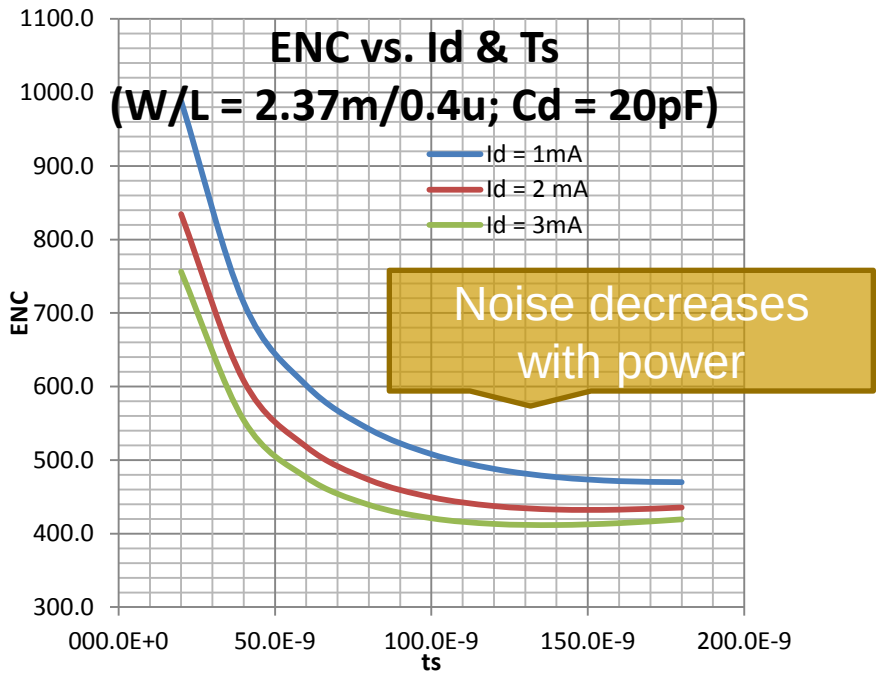
$$S_w = \frac{8}{3}\frac{KT}{g_m}$$

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}$$

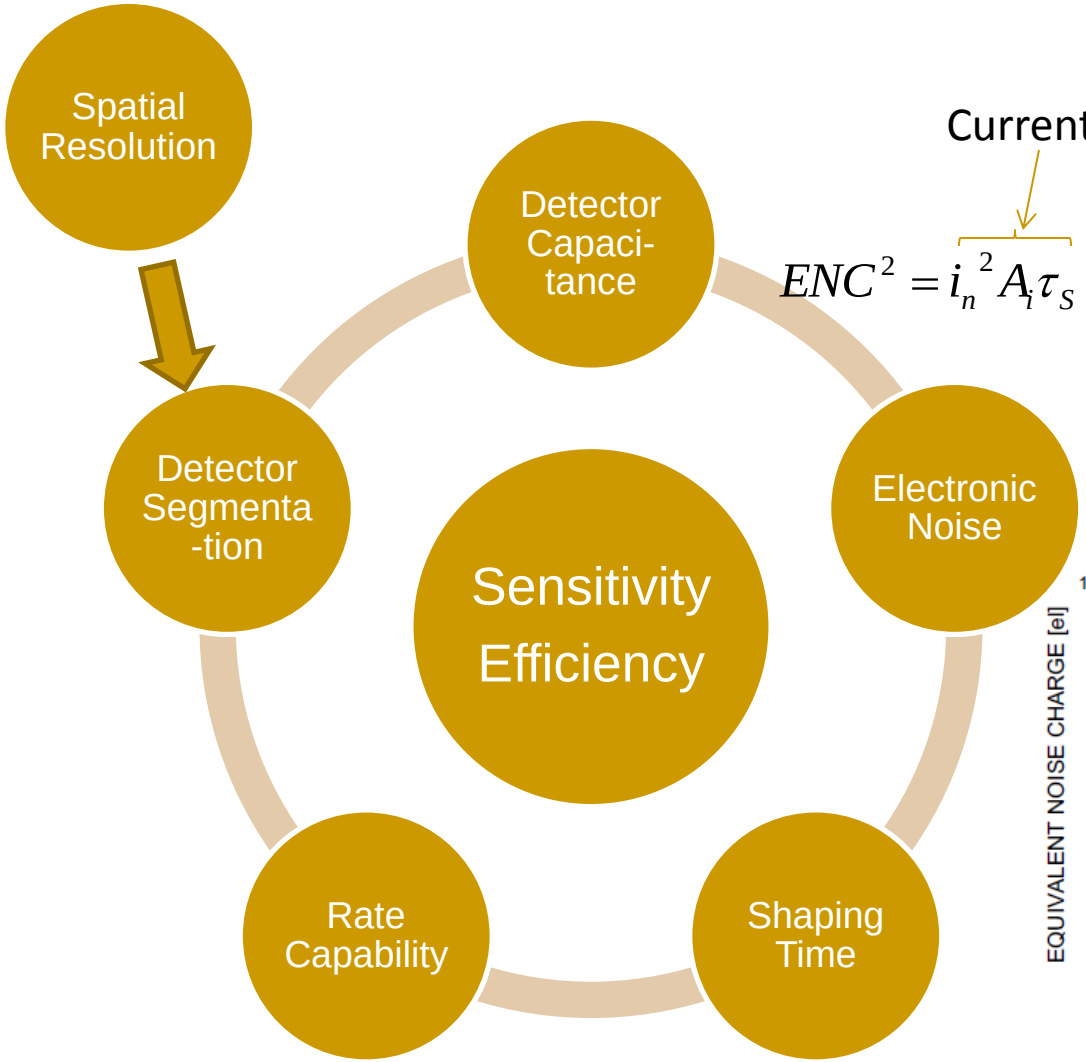
** TSMC 0.35um data from the web*

➢ variable shaping: 50 … 300 ns





Sensitivity vs. Efficiency



Current Noise

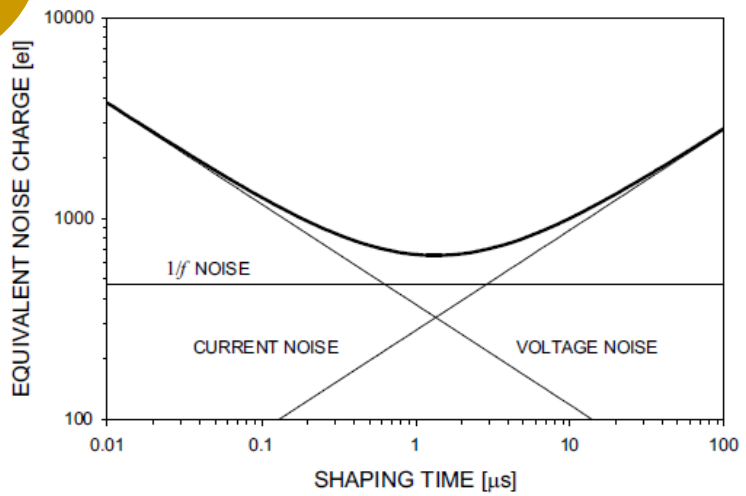
detector capacitance

$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

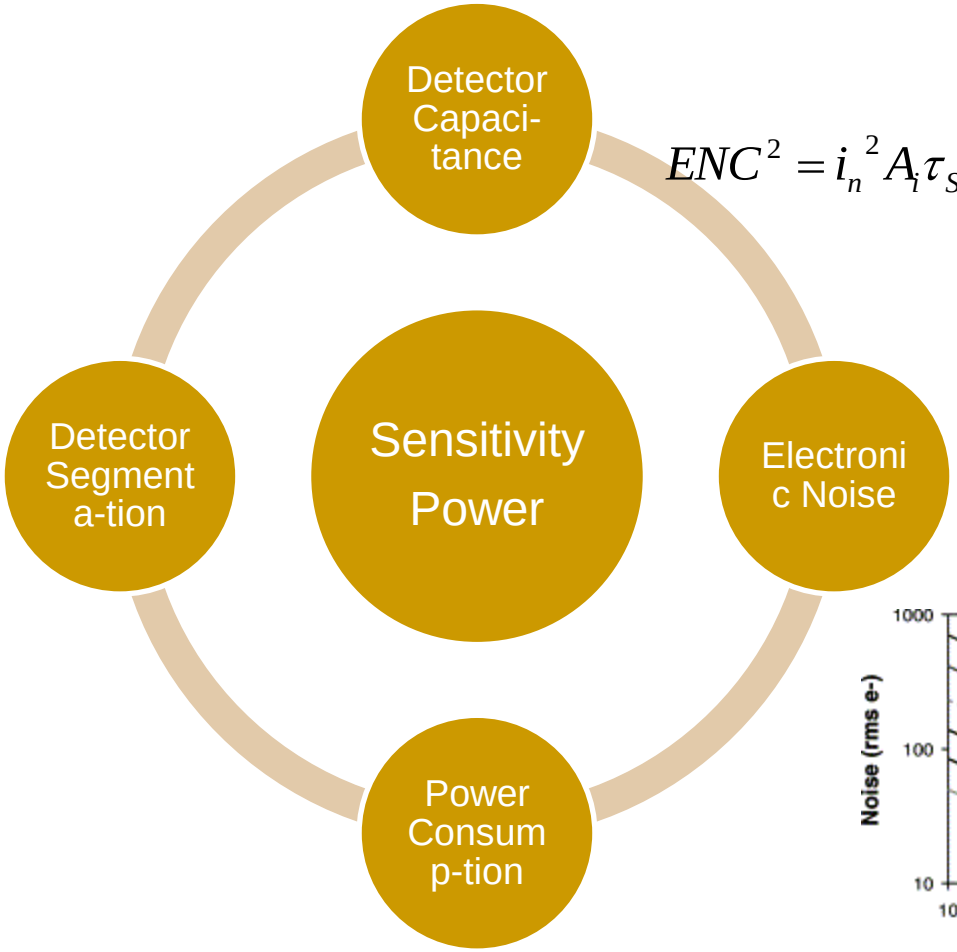
shaping time

White Noise

1/f Noise



Sensitivity vs. Power

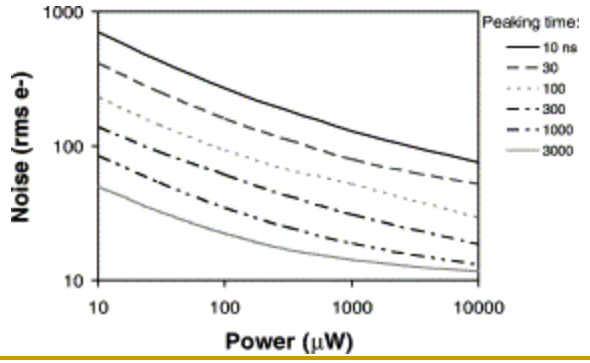


detector capacitance

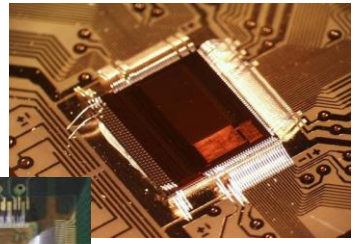
$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

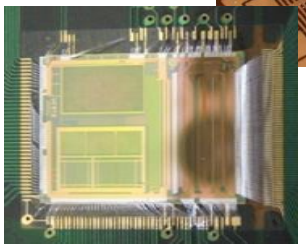
$$S_w = \frac{8}{3}\frac{KT}{g_m}$$

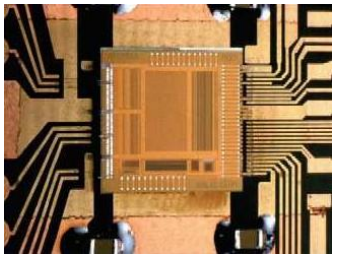
$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}$$



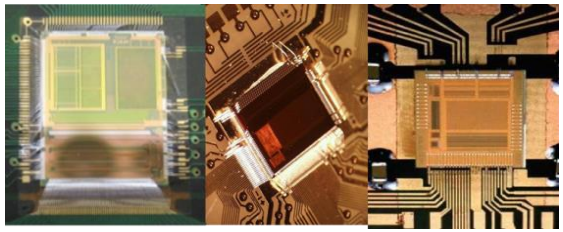
How do I readout all channels?



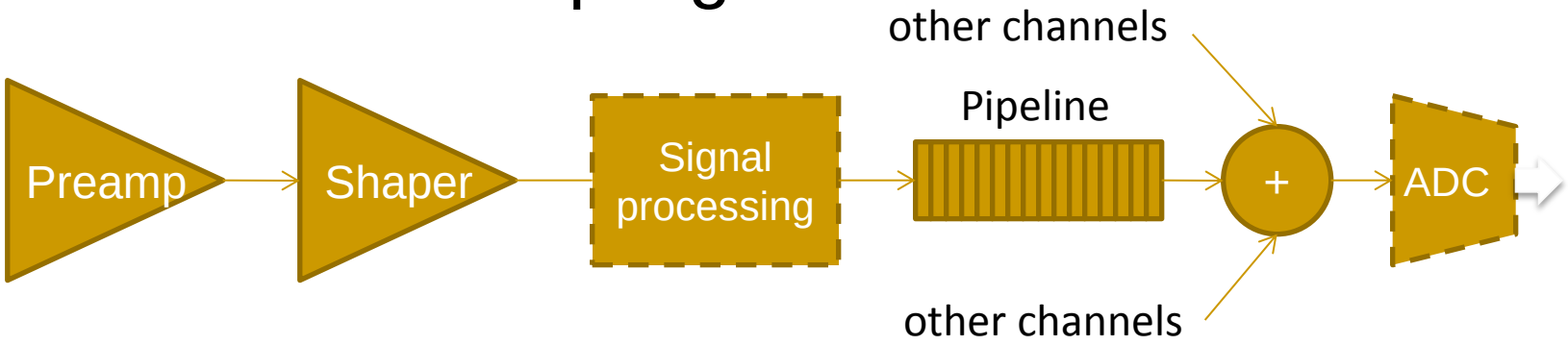




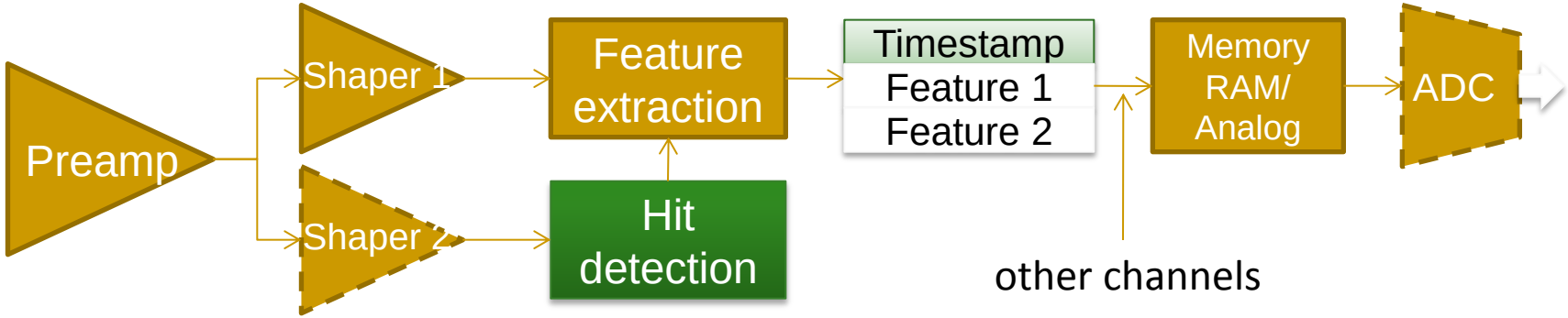
Front-End Architecture



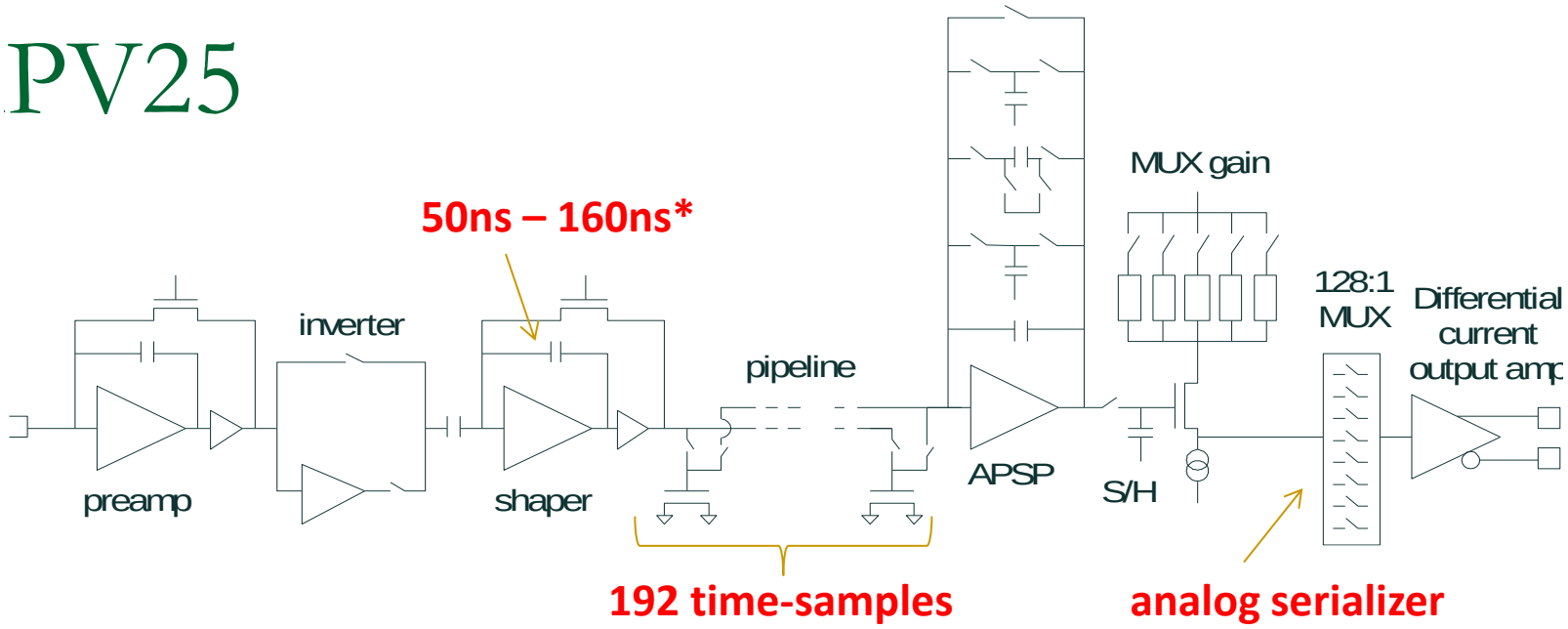
- Waveform sampling



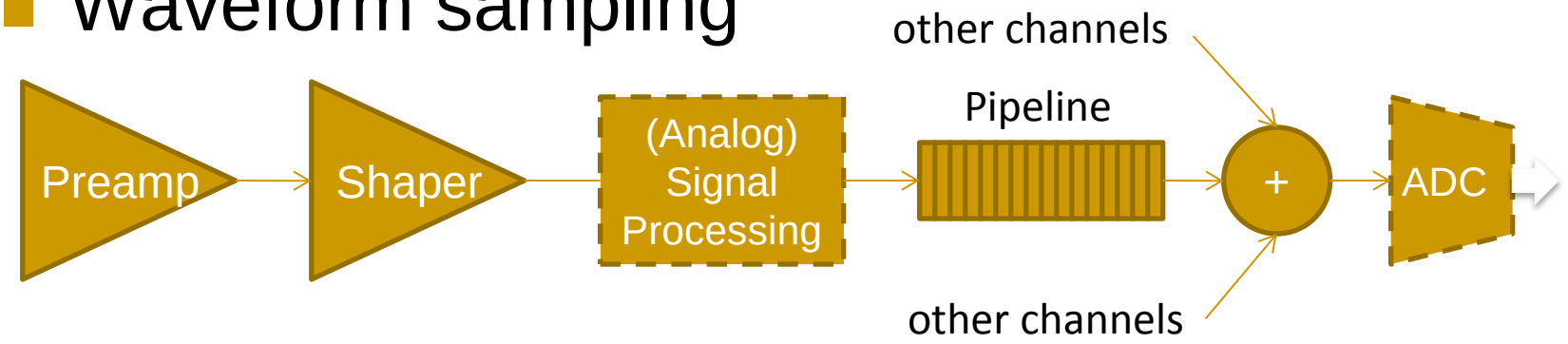
- Self-triggered channel



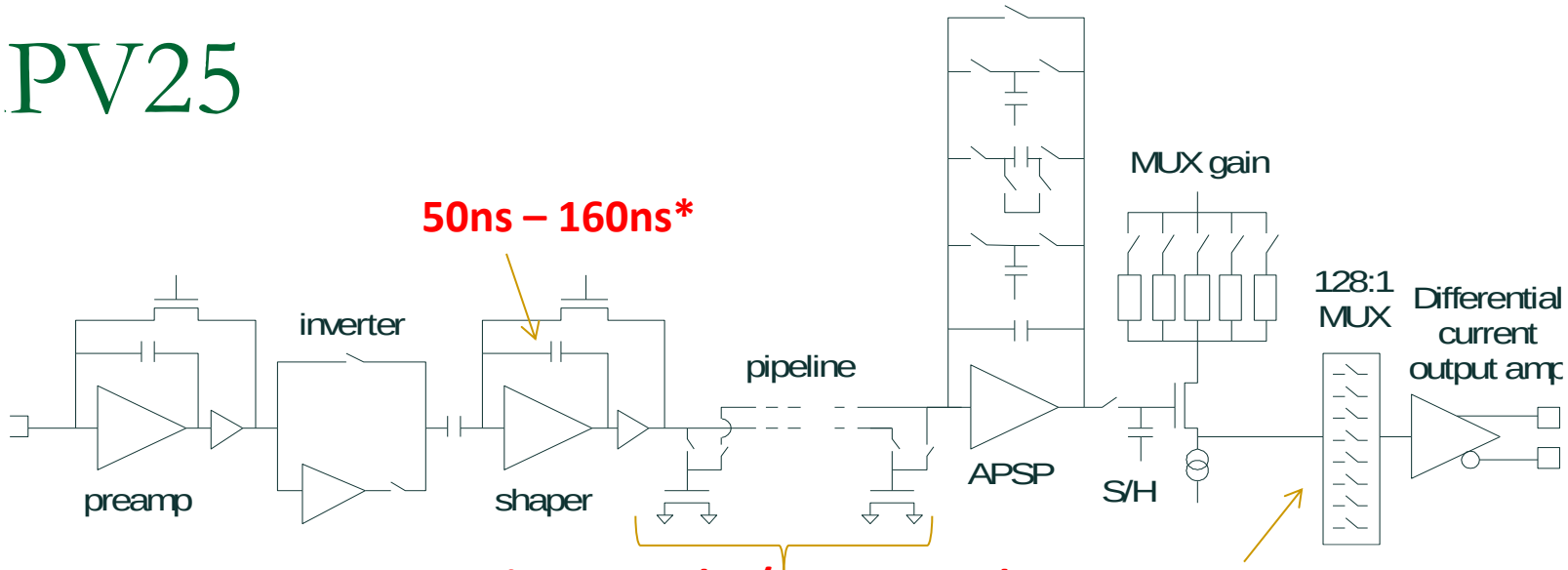
APV25

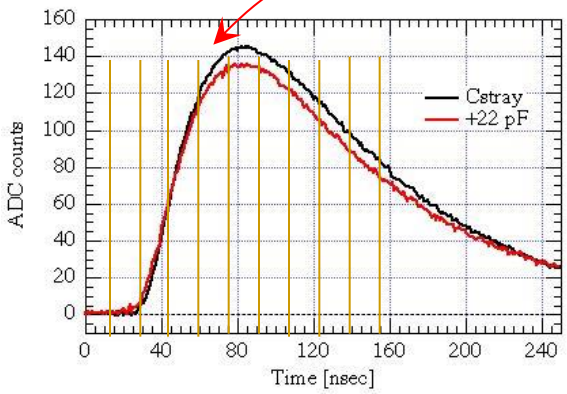


- Waveform sampling

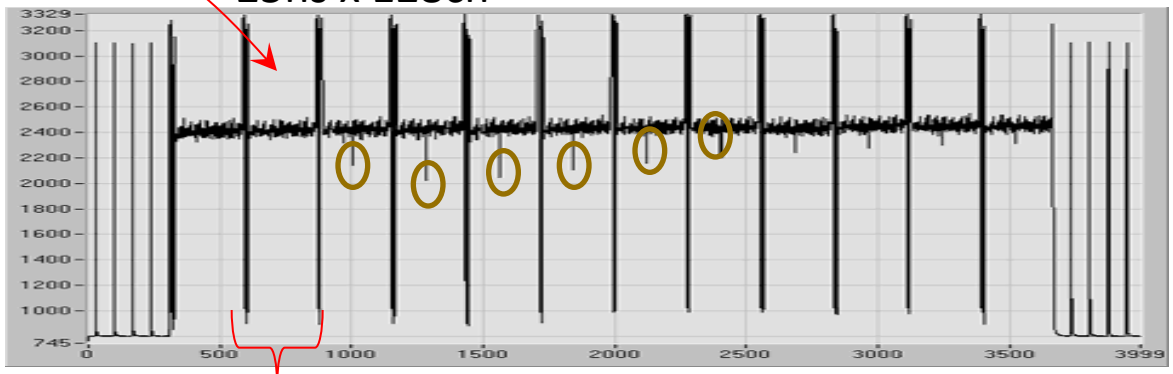


APV25



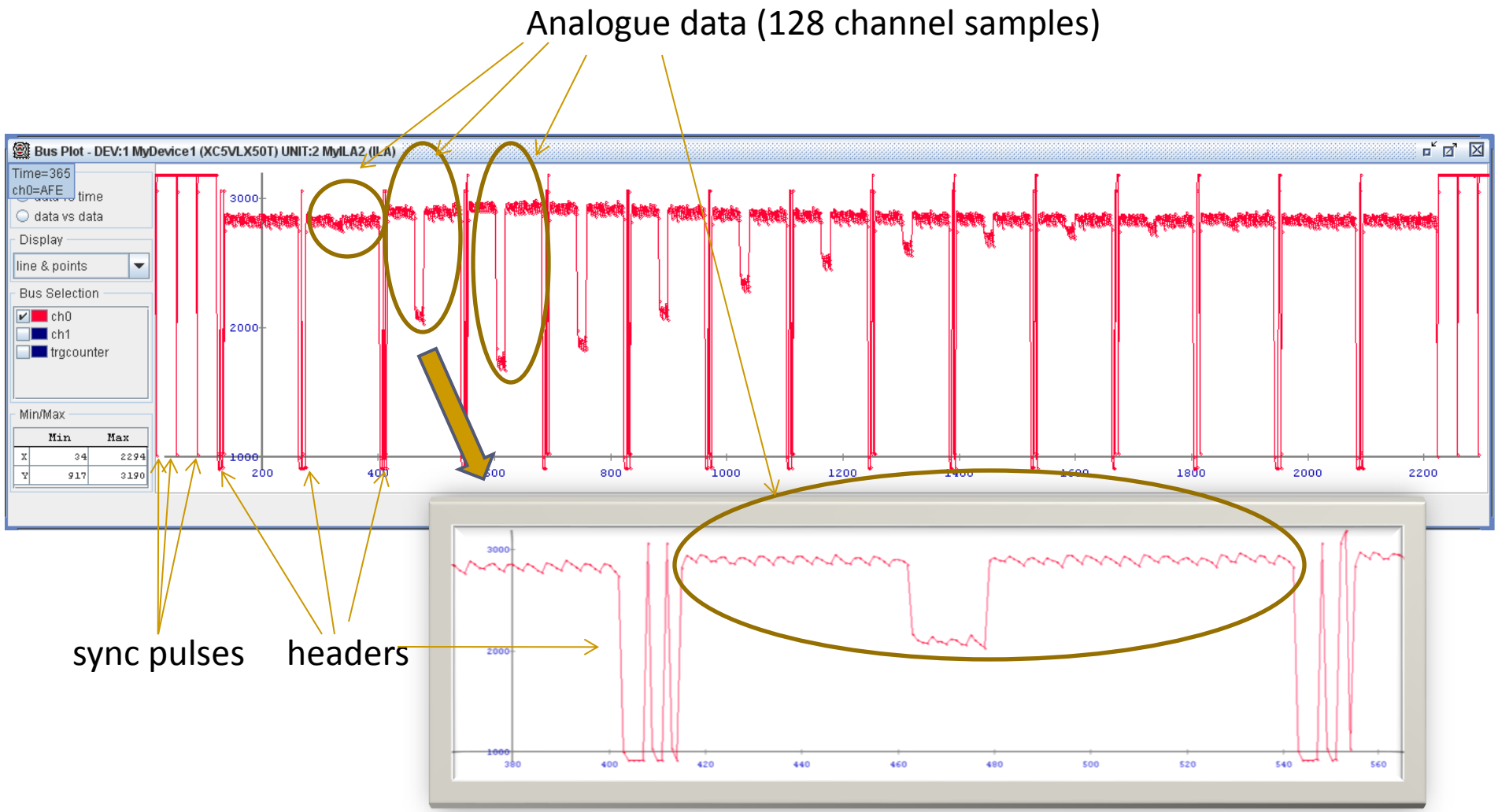


25ns x 128ch

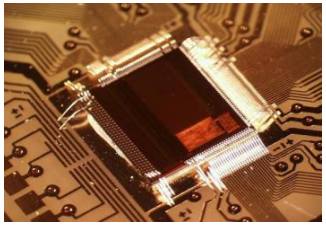


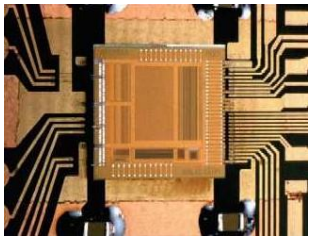
3.5us → Max rate(th) = 280kHz / nr_samples

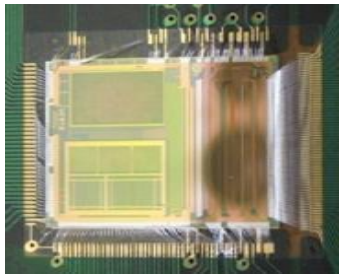
APV Analog Serial Frame



What front-end do I choose?

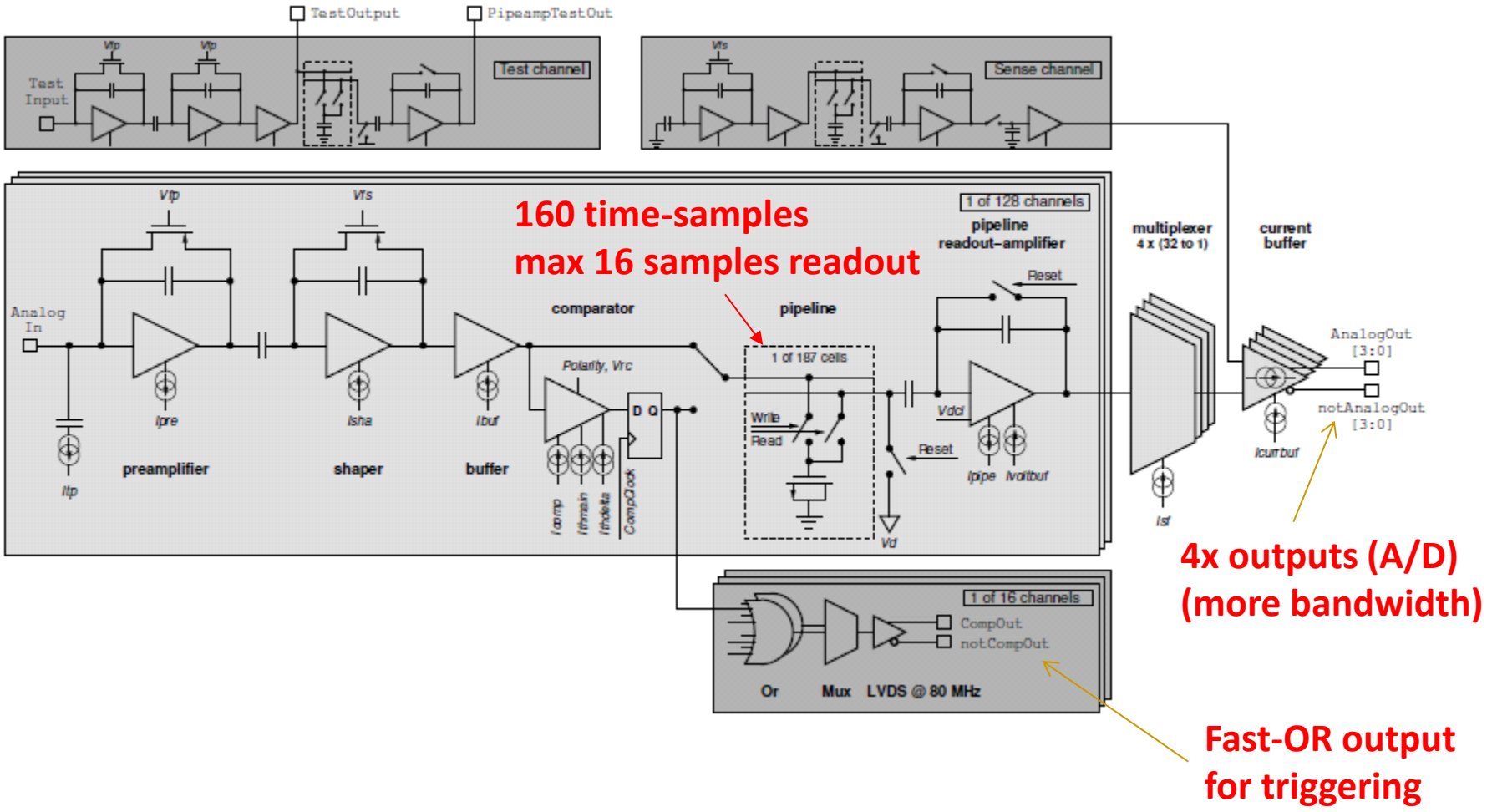




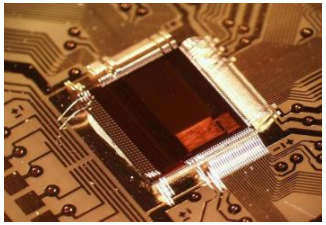


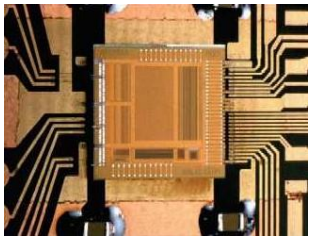
A little more data bandwidth if I use more outputs in parallel …

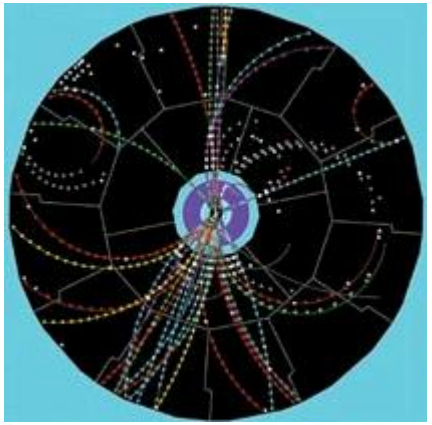
BEETLE

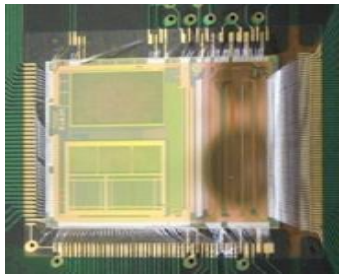

TestOutput
PipeampTestOut
Test Input
Test channel
Sense channel
160 time-samples
max 16 samples readout
1 of 128 channels
pipeline readout-amplifier
multiplexer 4 x (32 to 1)
current buffer
Analog In
preamplifier
shaper
buffer
comparator
pipeline
1 of 187 cells
Polarity, Vrc
Write
Read
Reset
AnalogOut [3:0]
notAnalogOut [3:0]
1 of 16 channels
CompOut
notCompOut
Or
Mux
LVDS @ 80 MHz
4x outputs (A/D)
(more bandwidth)
Fast-OR output
for triggering

What front-end do I choose?







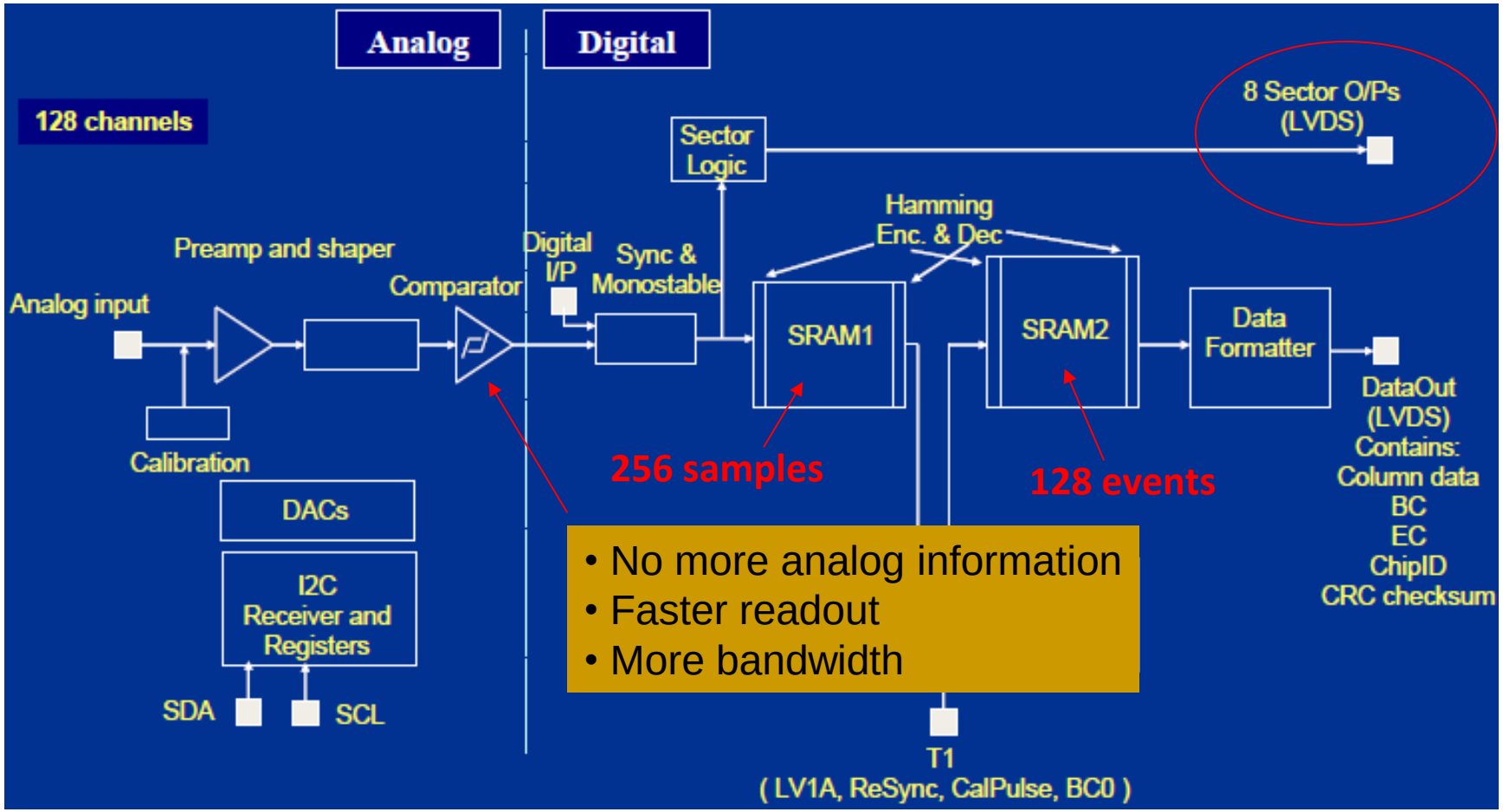


How can I go faster?

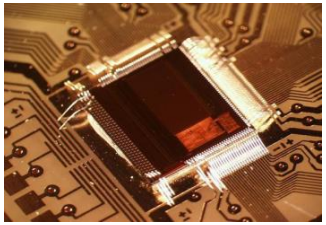
Is ADC resolution really necessary for my application or I can live with just one bit?

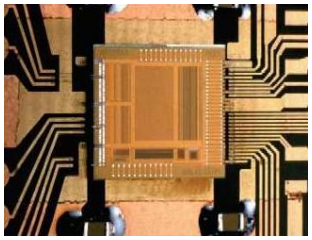
- Ex. Tracking detectors

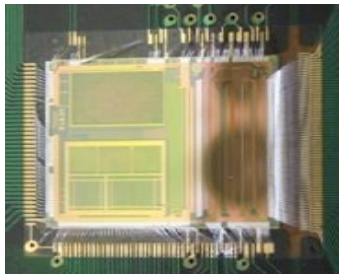
VFAT – Binary readout

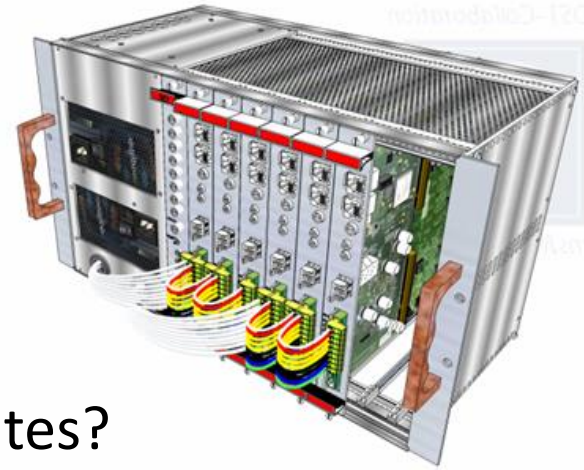


What front-end do I choose?



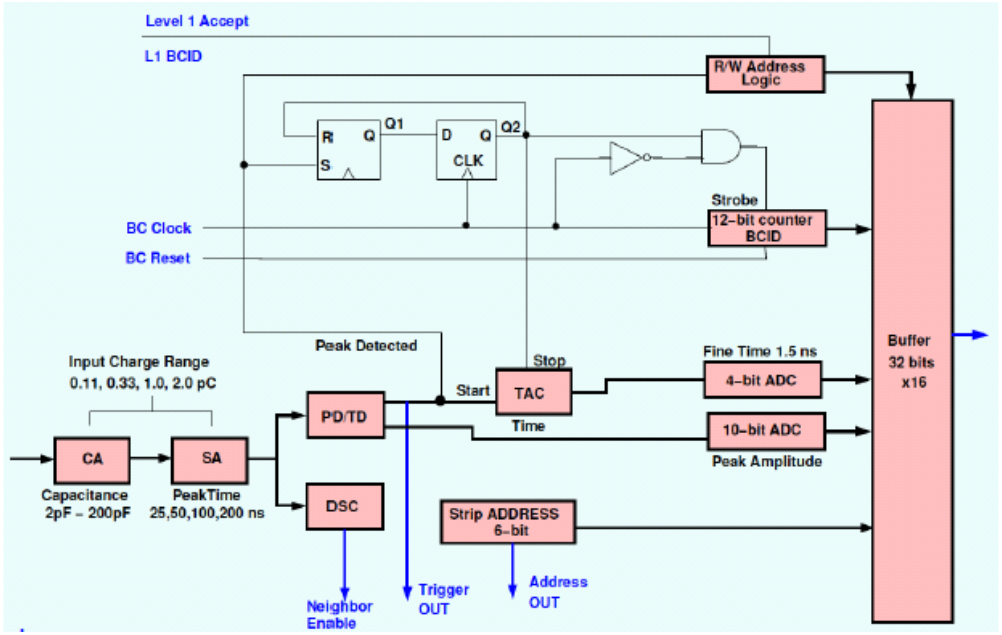


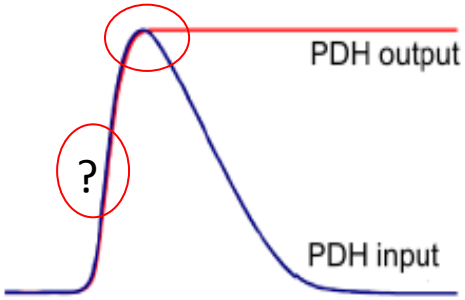




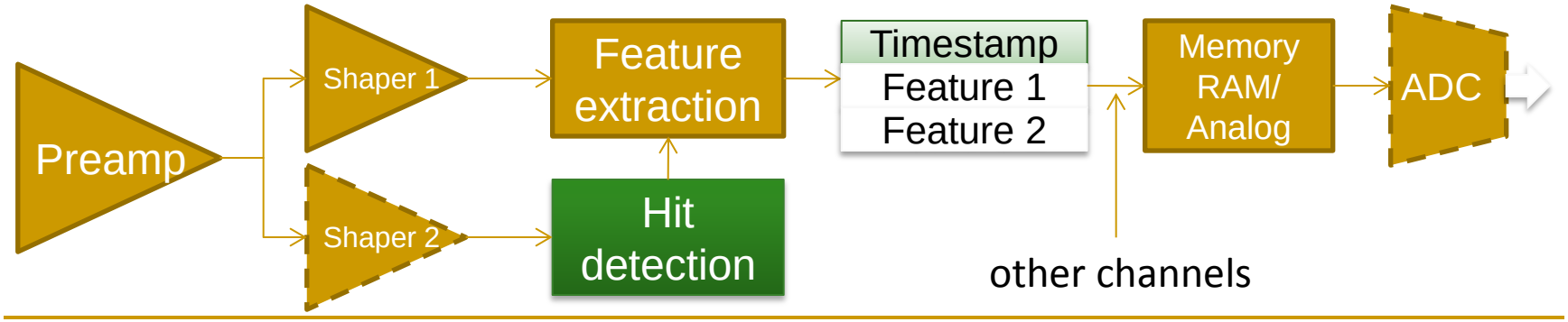
What do I do if I have very high events rates?

VMM (BNL)



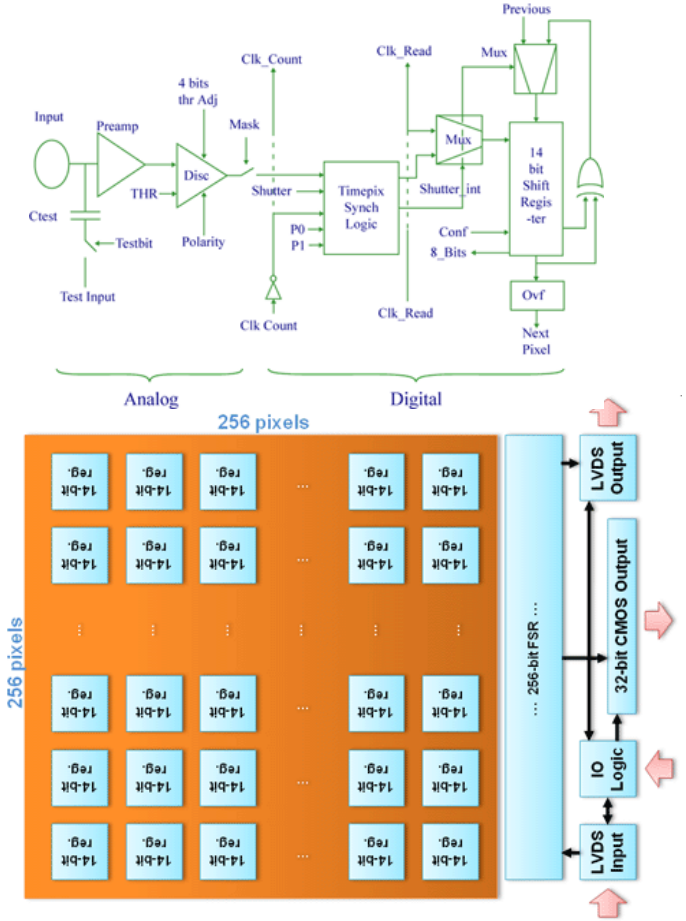


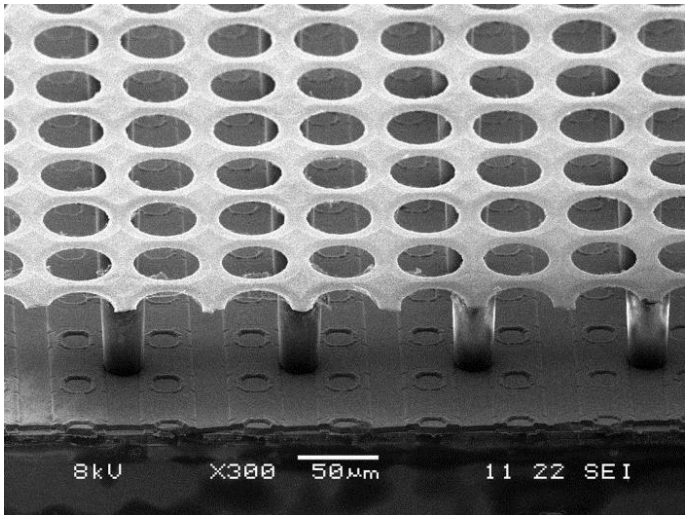
- Data driven system
- No sampling clock
- Self triggered
- Natural zero-suppression
- Feature extraction

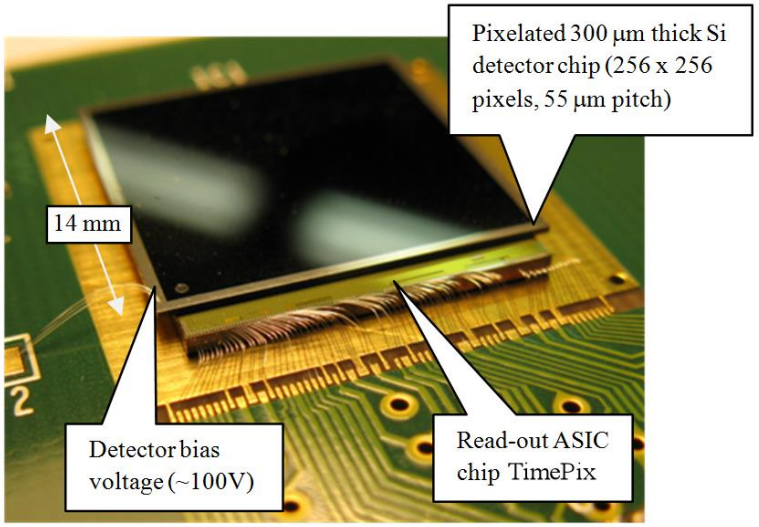


Other

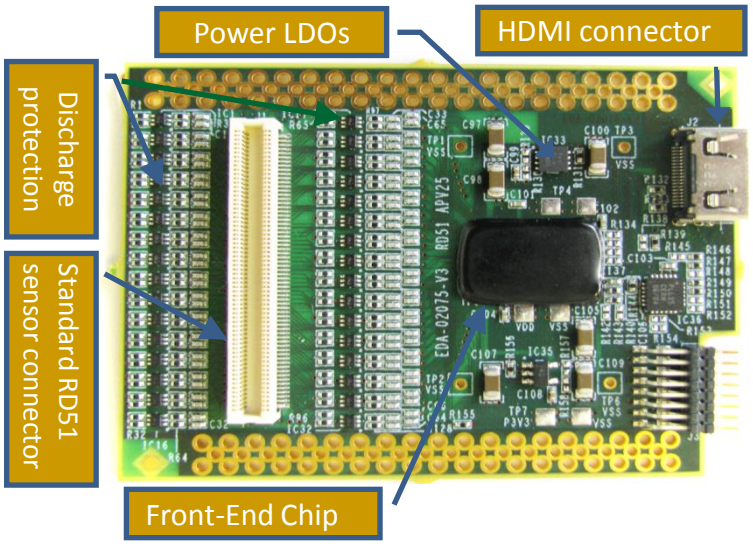
- Pixel readout - TIMEPIX

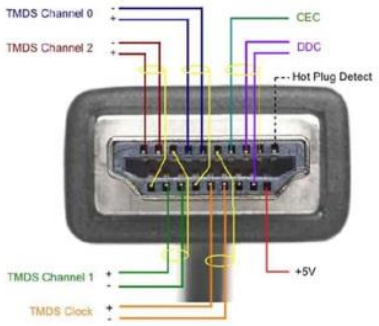


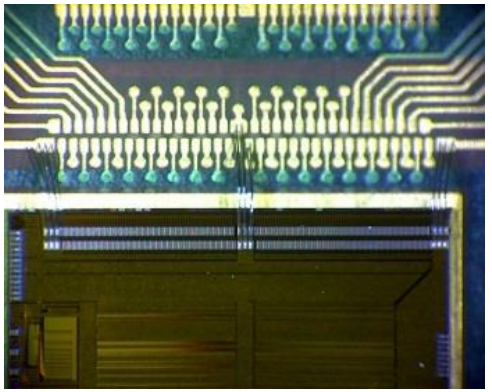


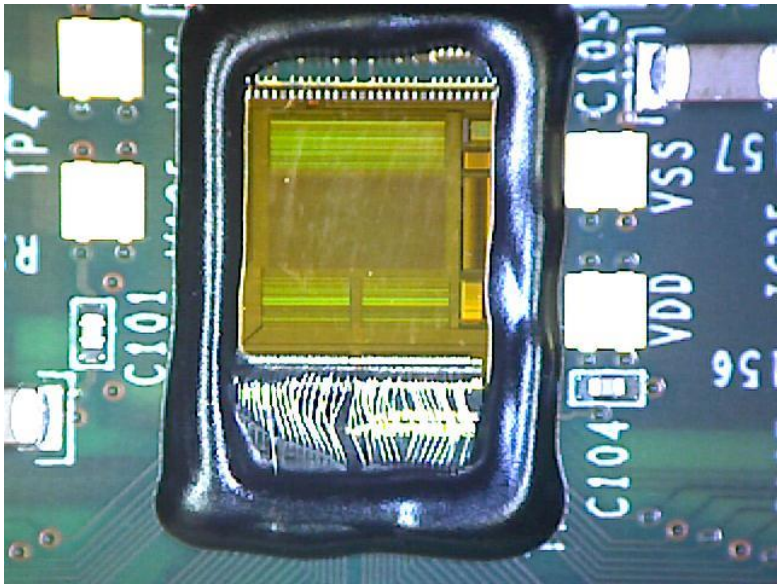


SRS Hybrids







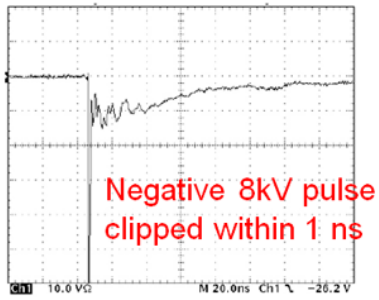


- standard RD51 connector
- discharge protection
- micro-HDMI
  - clk & trg
  - data links
  - dcs (I2C)
- industry-ready design
- purchase through CERN store

SRS Hybrids – Discharge Protection

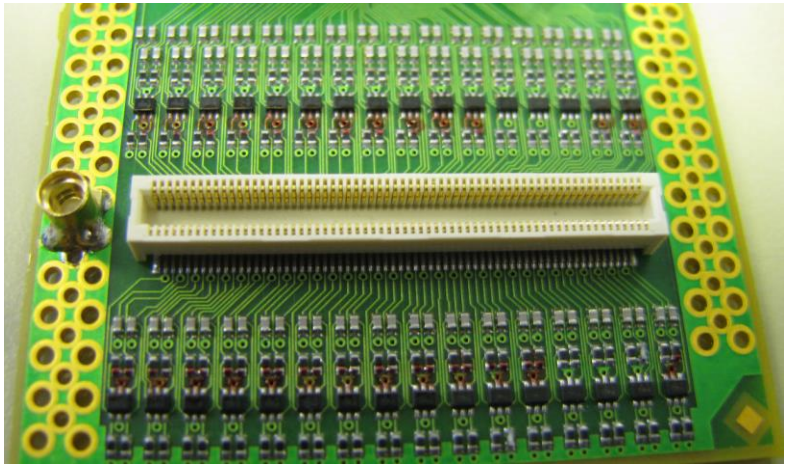
Sparc protection on hybrid

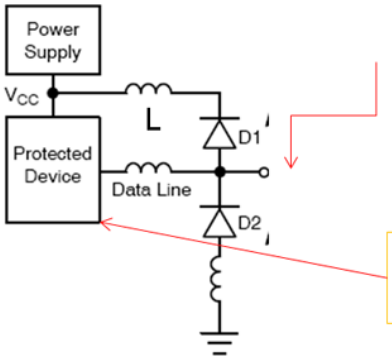
NUP4114UPXV6 quad ESD diodes: < 1 pF

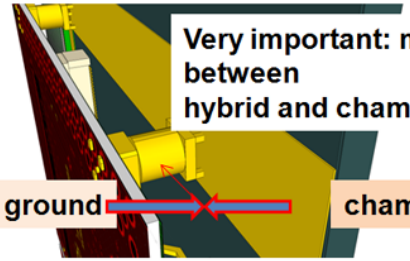


IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

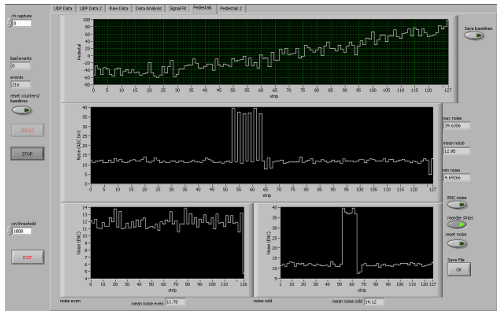






Very important: minimize L between hybrid and chamber: MMCX plugs

chip ground — chamber ground



Negative clipped: $V_n = -V_f - L \times dI_{esd}/dt$

Positive clipped: $V_p = V_{cc} + V_f + L \times dI_{esd}/dt$

SRS Hybrids – Discharge Protection

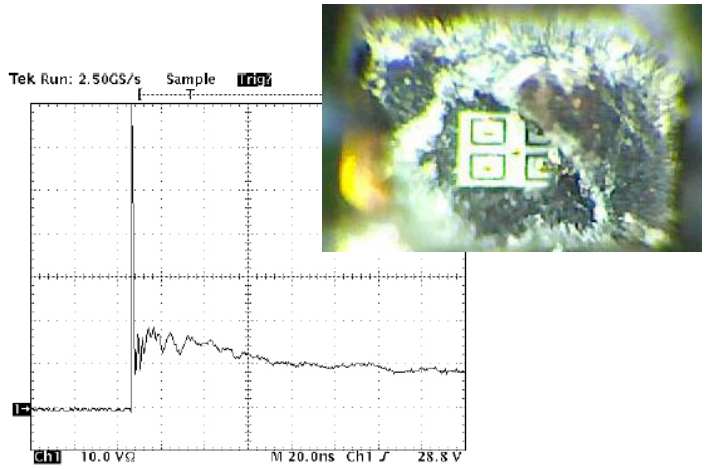
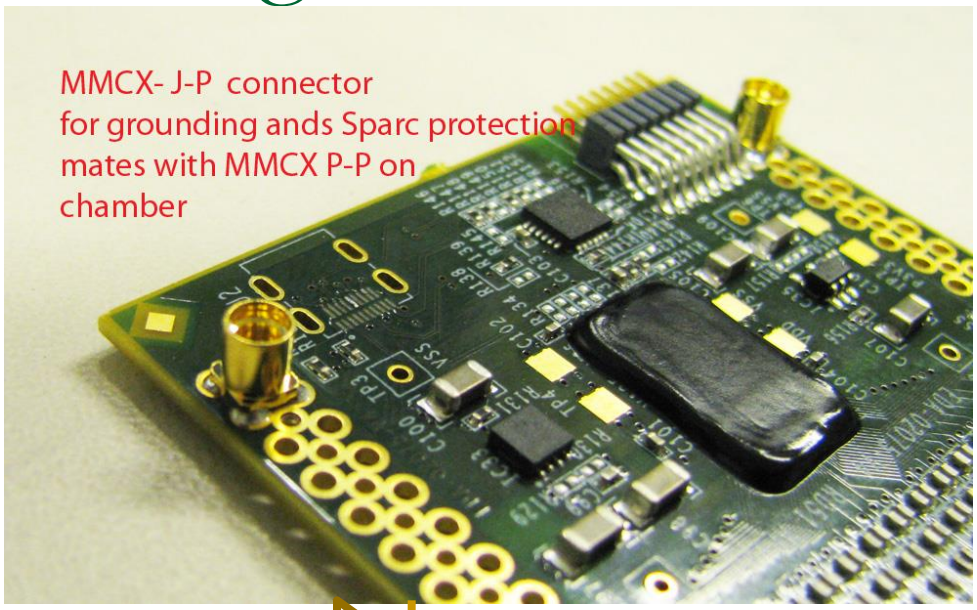
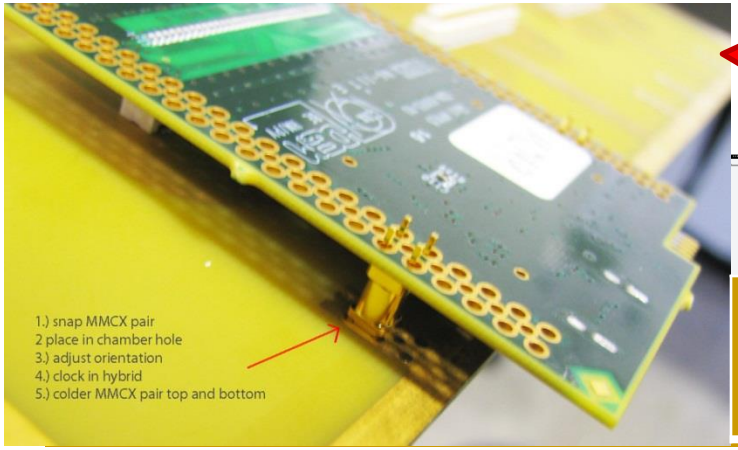
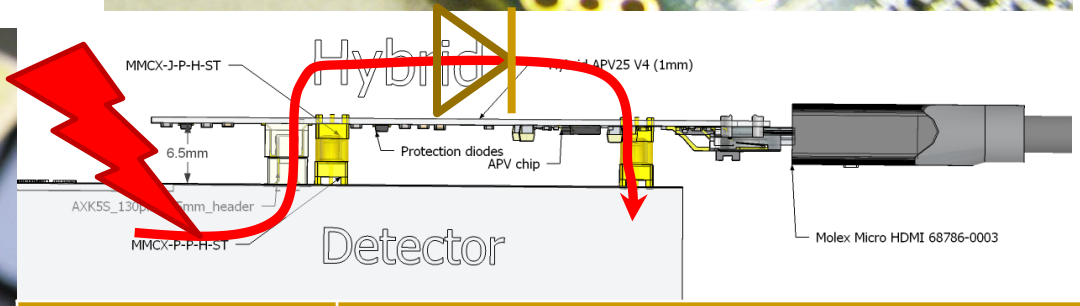


Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000-4-2





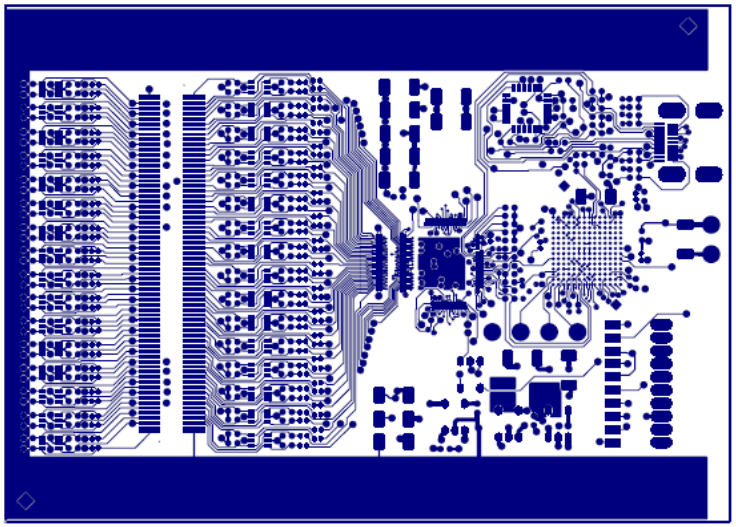


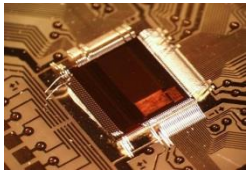
Samtec MMCX coax connector

GND connection (< 2mohm)
middle pin can be used for power
mechanical connection

New Hybrids

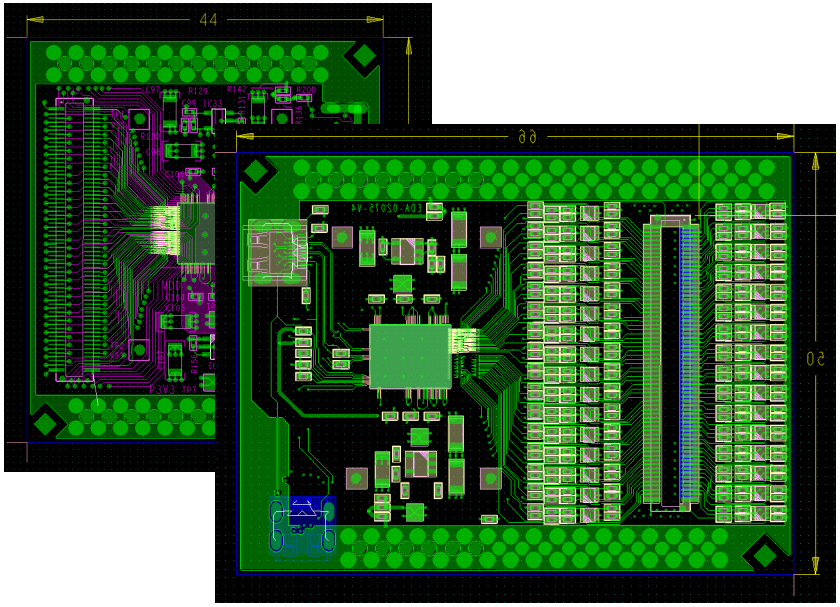
- BEETLE Hybrid





- Rad-tol CPLD
  - Comparator OR/MUX
  - Clk & Trg decode
- Work in progress

- VFAT2 Hybrid



- Optional stacking conn. for *cable-less* connection
- Power option via MMCX connectors
- First prototypes foreseen for Aug-Sep 2012

Scalability Concept
System Size (small)

1Gb Ethernet

off-detector

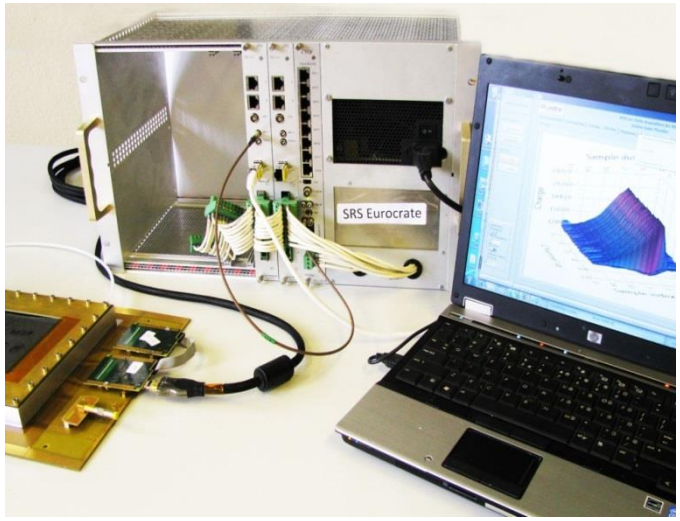
Front-end Adapter Card (FEC)

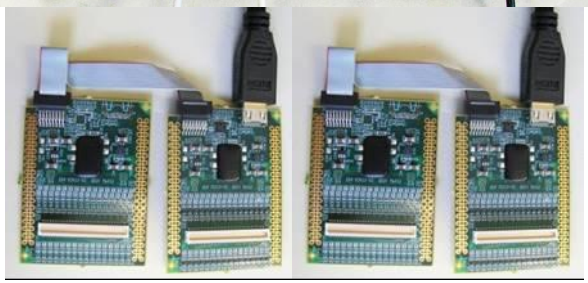
Chip-link (HDMI, fiber, …)

on-detector

FE ASIC | FE ASIC | FE ASIC

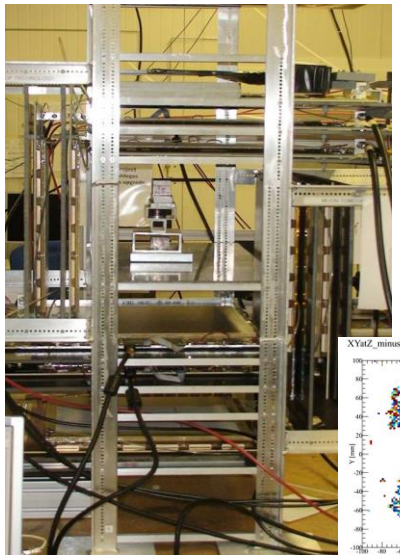
DETECTOR



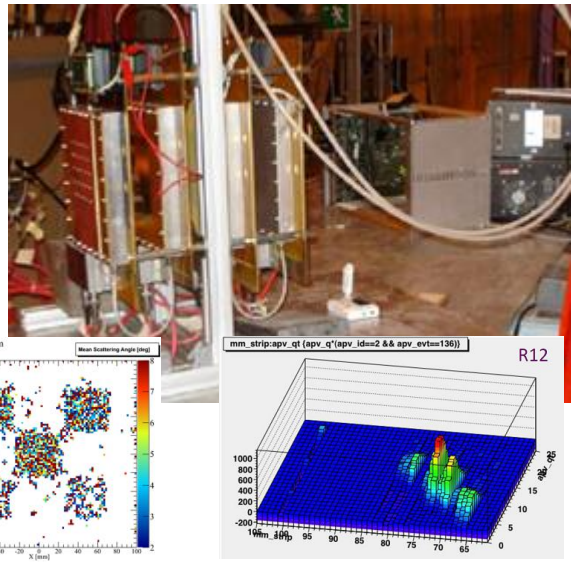


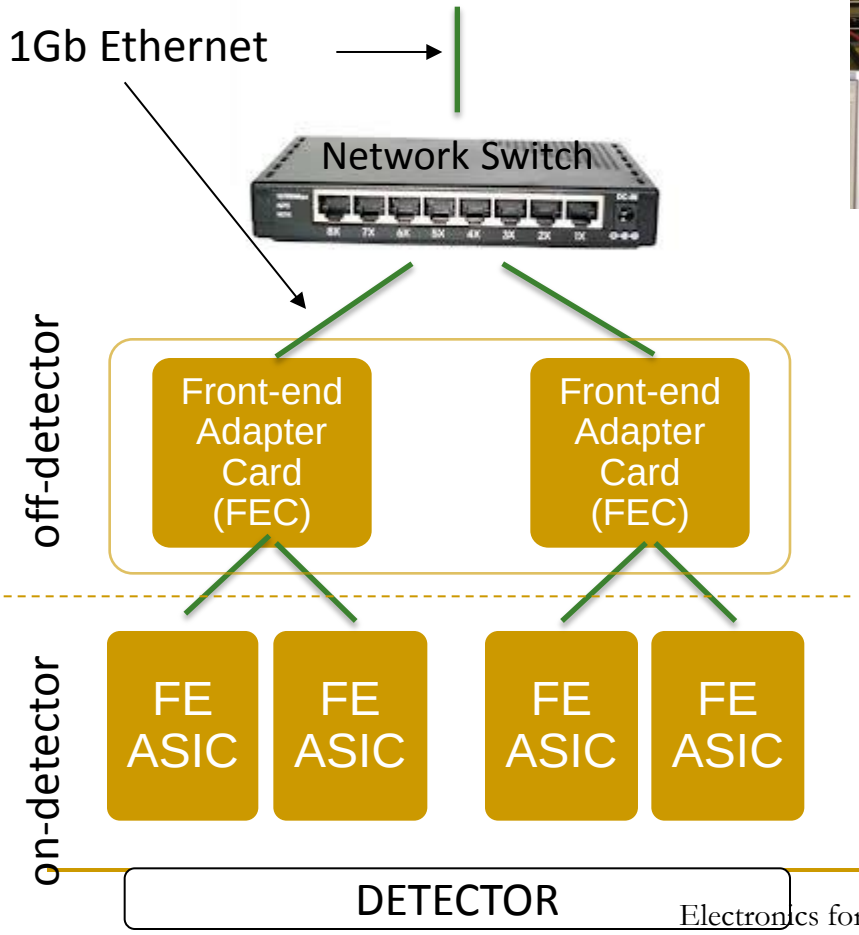
Scalability Concept System Size (medium)

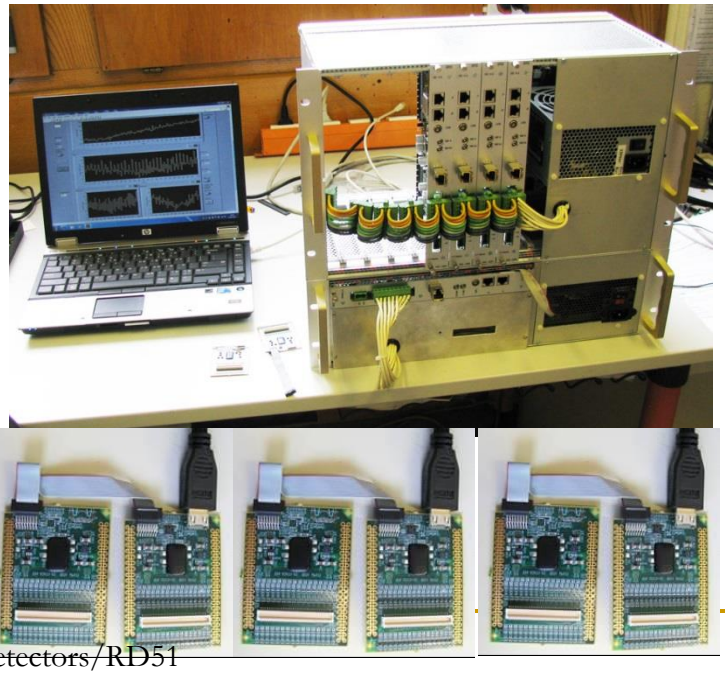
Muon Tomography (Florida)



MAMMA Beamtest (CERN)

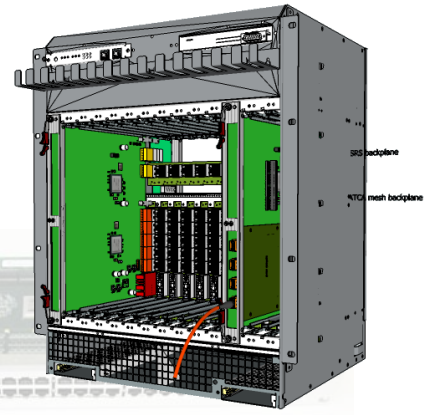






Scalability Concept System Size (large)

ATCA-SRS



1/10/*40*.. Gb Ethernet
(opt. DDL/S-Link/…)

Scalable Readout Unit (SRU)

DTC Link
(***D**ata,**T**rigger&**C**ontrol*)

Eurocrate

off-detector

Front-end Adapter Card (FEC)

Front-end Adapter Card (FEC)

Front-end Adapter Card (FEC)

on-detector

FE ASIC

FE ASIC

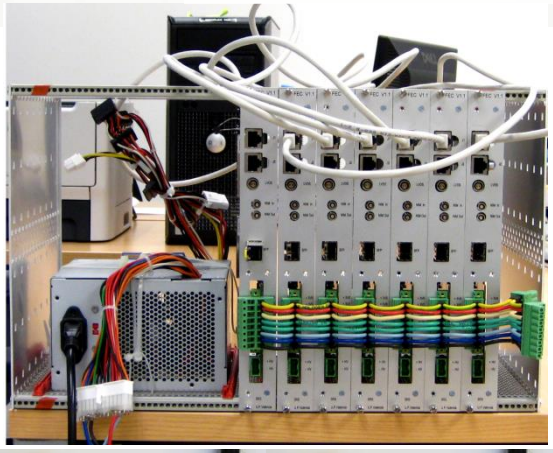
FE ASIC

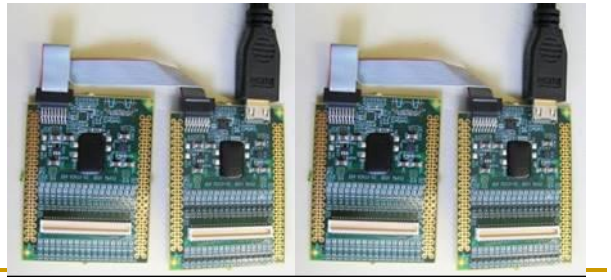
FE ASIC

FE ASIC

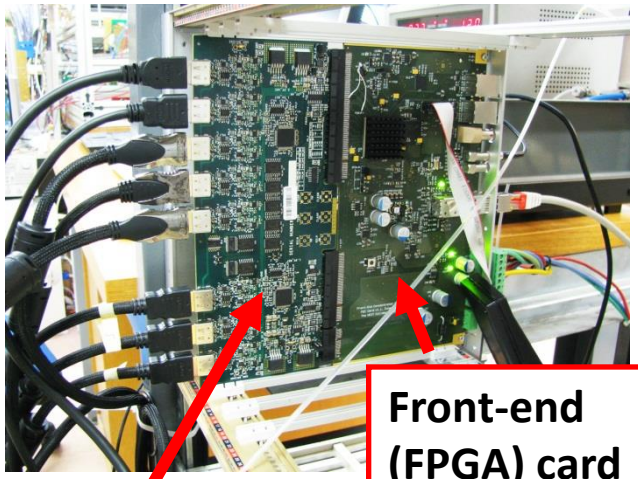
FE ASIC

DETECTOR



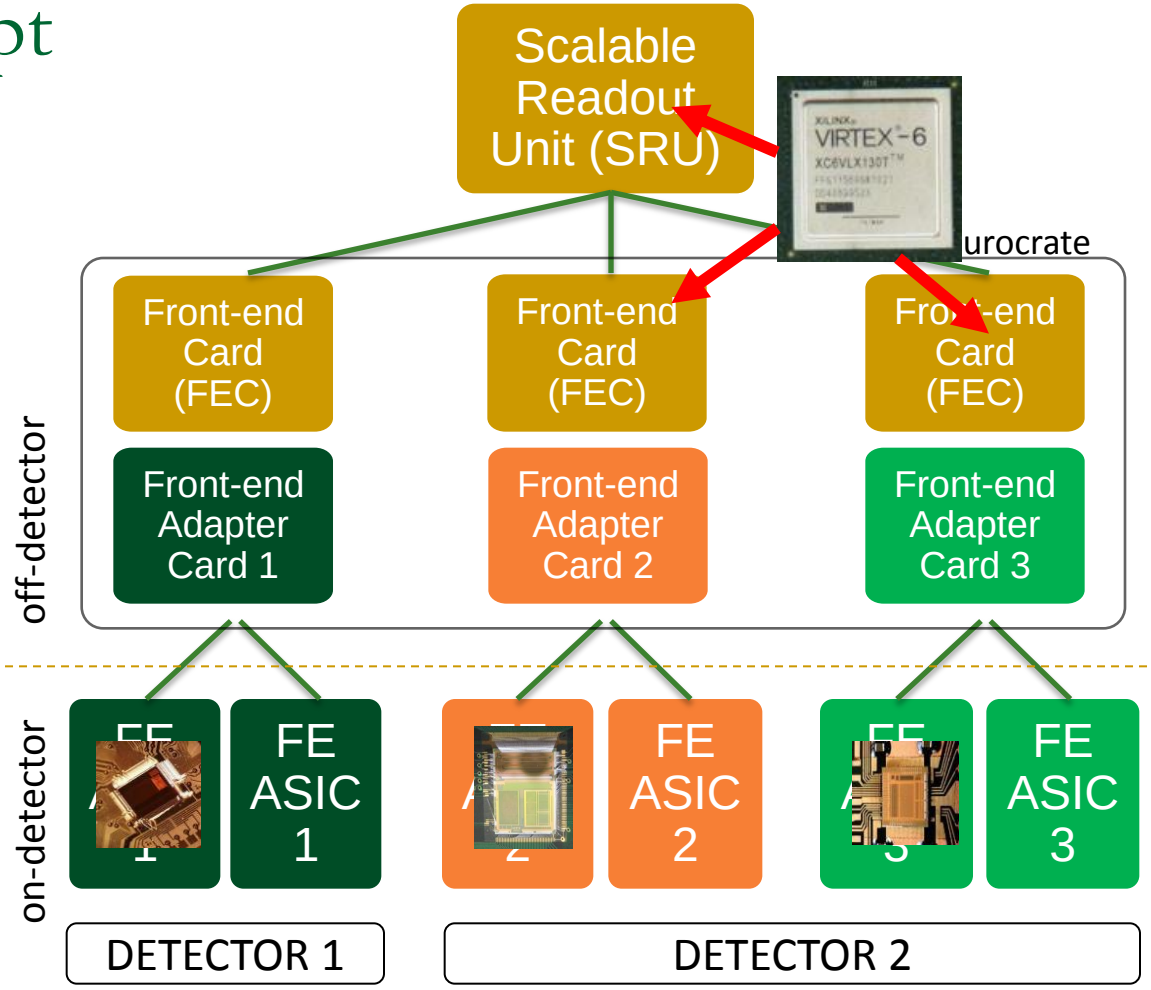


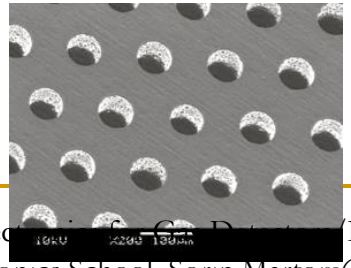
Scalability Concept Application

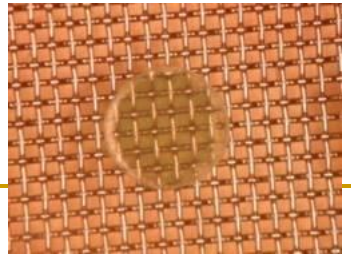


Front-end (FPGA) card

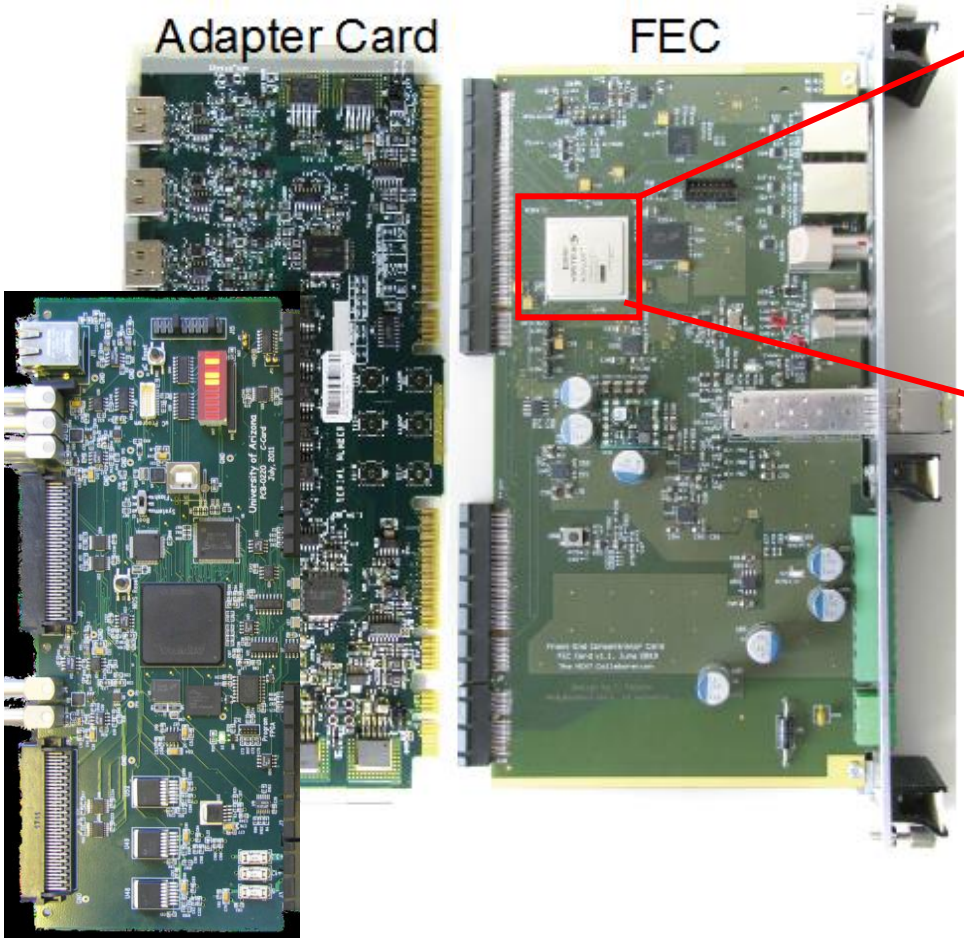
Adapter Card
- ADC / digital / optical /…

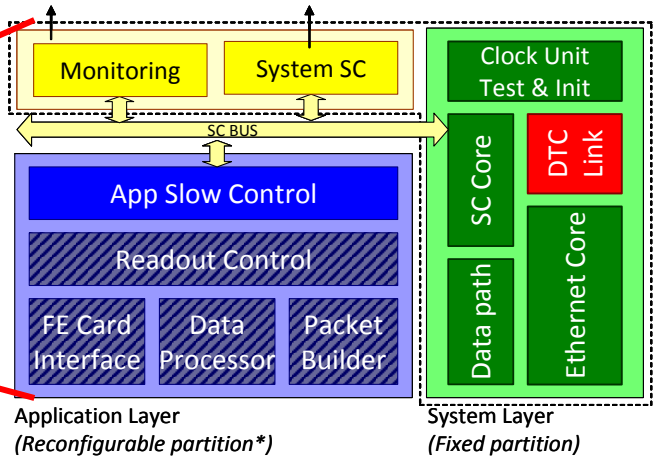






SRS – Digital Processing





- Signal processing
- Zero-suppression
- Feature extraction
- Packet/Event builder

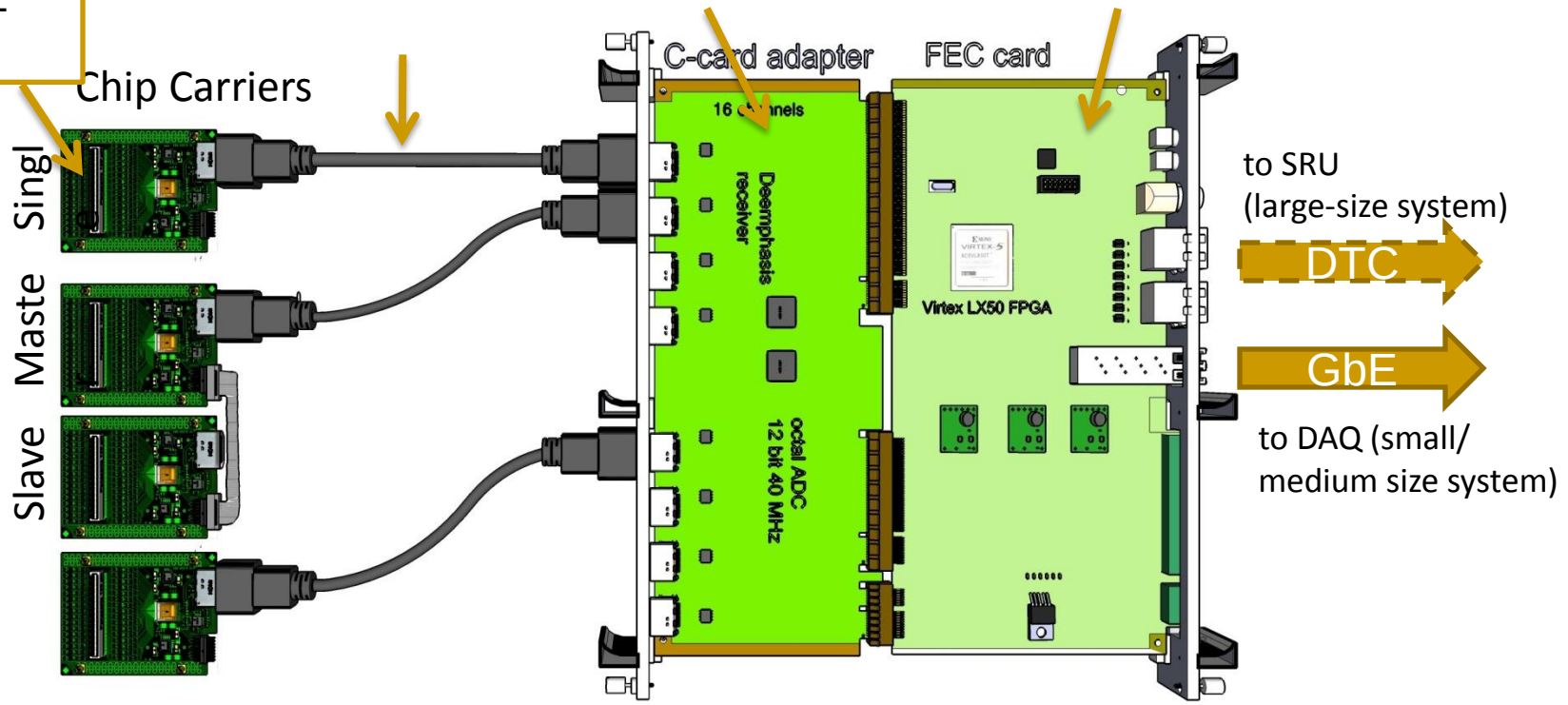
SRS Overview

On-detector front-end hybrids
- APV25
- VFAT
- BEETLE
- …

Chip-links
- HDMI
  - analog (APV/Beetle)
  - digital (VFAT/Beetle)
- optical (GBT. …)
- …

Front-end adapter (FE-specific)
- ADC card
- digital FE card (VFAT)
- GBT receiver
- …

Front-end FPGA card (SRS standard) modular firmware:
- SRS control
- application specific



Thank you!