John Adams Institute for Accelerator Science

Oxford Physics

Drive-beam Phase Feedforward

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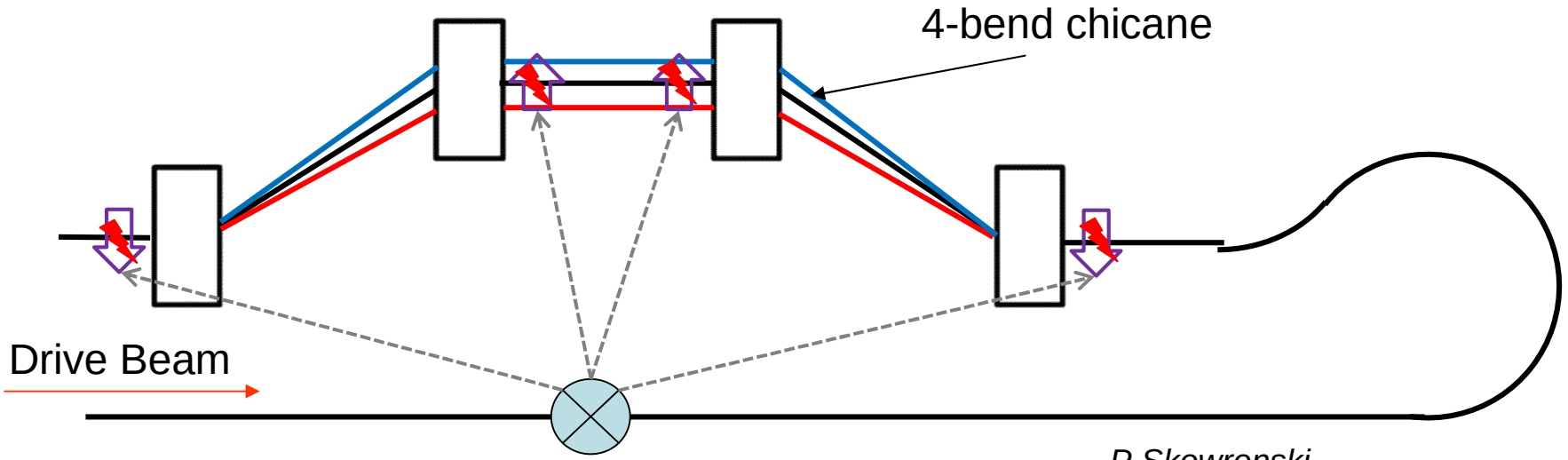
INFN, Frascati

CLIC-UK Review, 4 October 2013

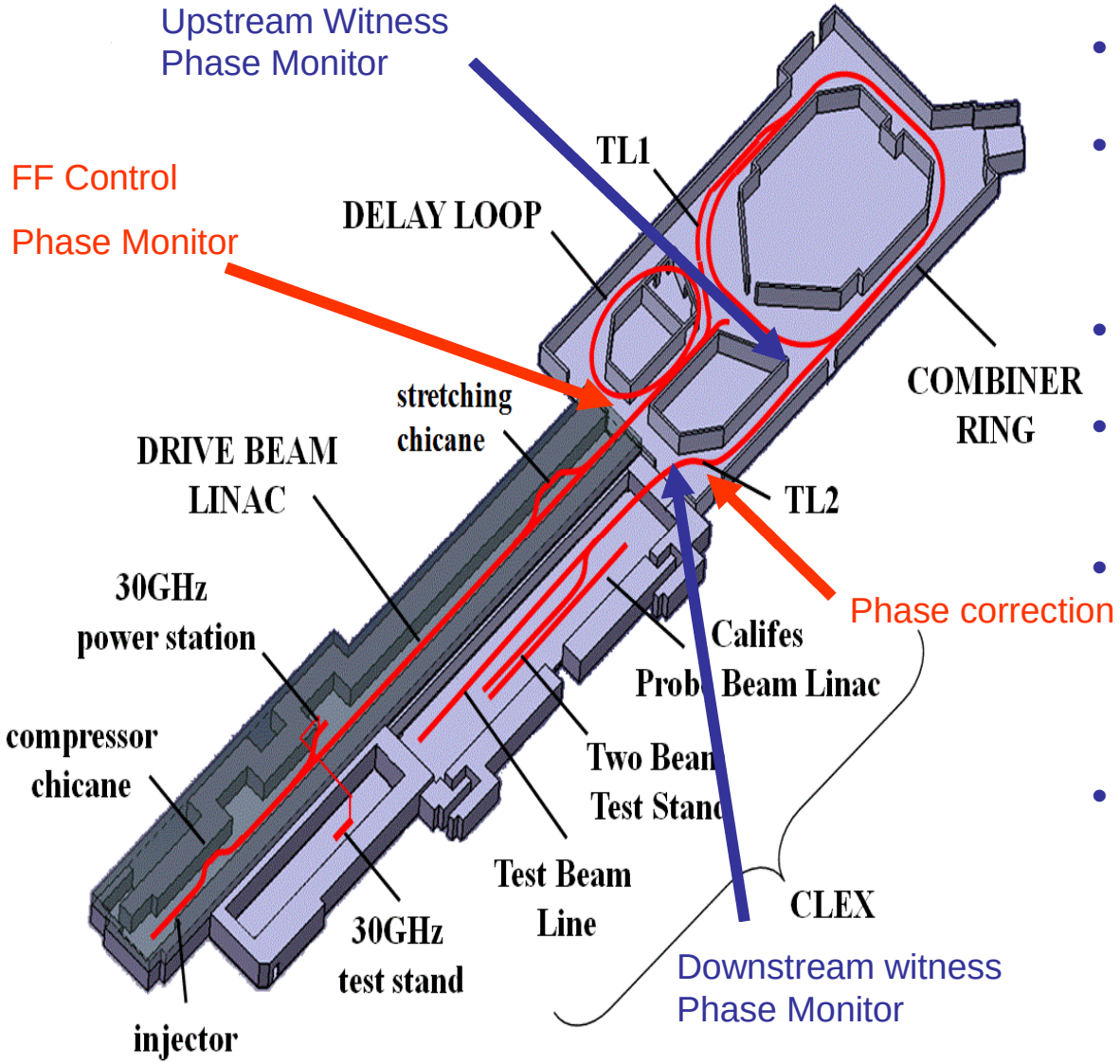
CLIC drive beam FF: concept

- Feed-forward system to reduce drive beam phase errors to below 0.1%
- Instrument each turnaround with feed-forward system:
  - Measure phase at TA entrance and correct with 4-bend magnetic chicane – compensate phase error, changing TOF in chicane.
    - 10 degree correction range, +/- 375 μrad at each bend – 4 kickers per bend
  - ‘Phase monitors’ (INFN Frascati) + readout electronics (CERN)
    - ~20 fs resolution, 100 MHz bandwidth
  - Amplifiers (JAI Oxford)
    - ~500 kW peak power per kicker, ~ 70 MHz bandwidth
  - Kickers (INFN Frascati)
    - 1 metre active length striplines – 16 per turnaround
- System replicated at each of 48 turnarounds at CLIC!



P.Skowronski

Drive Beam FF: Tests at CTF3

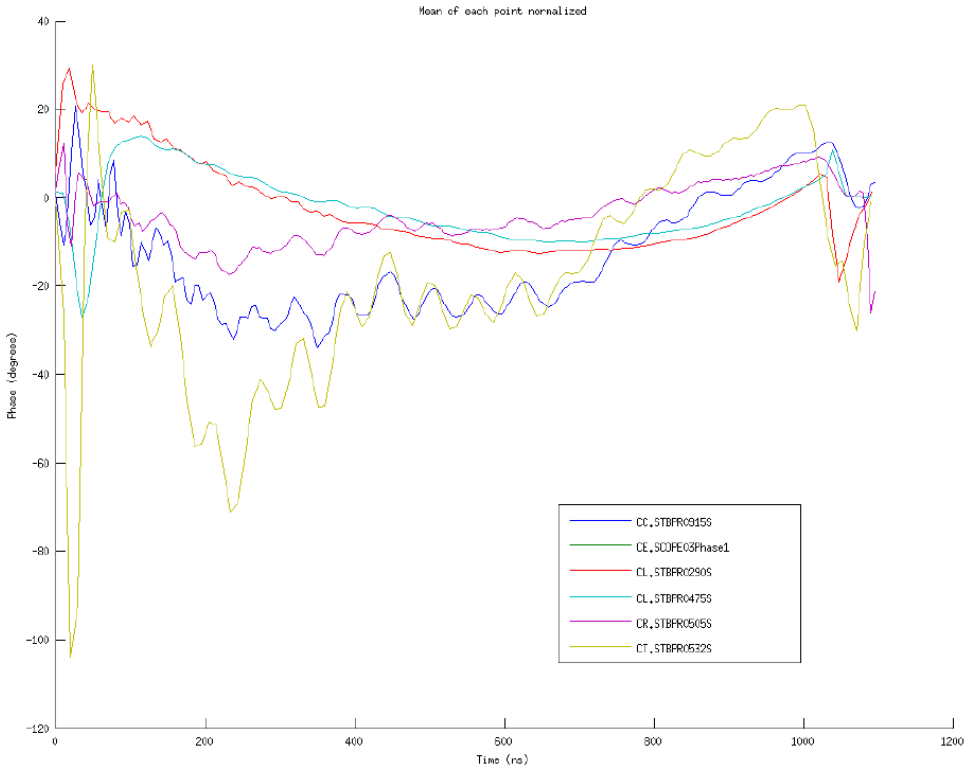


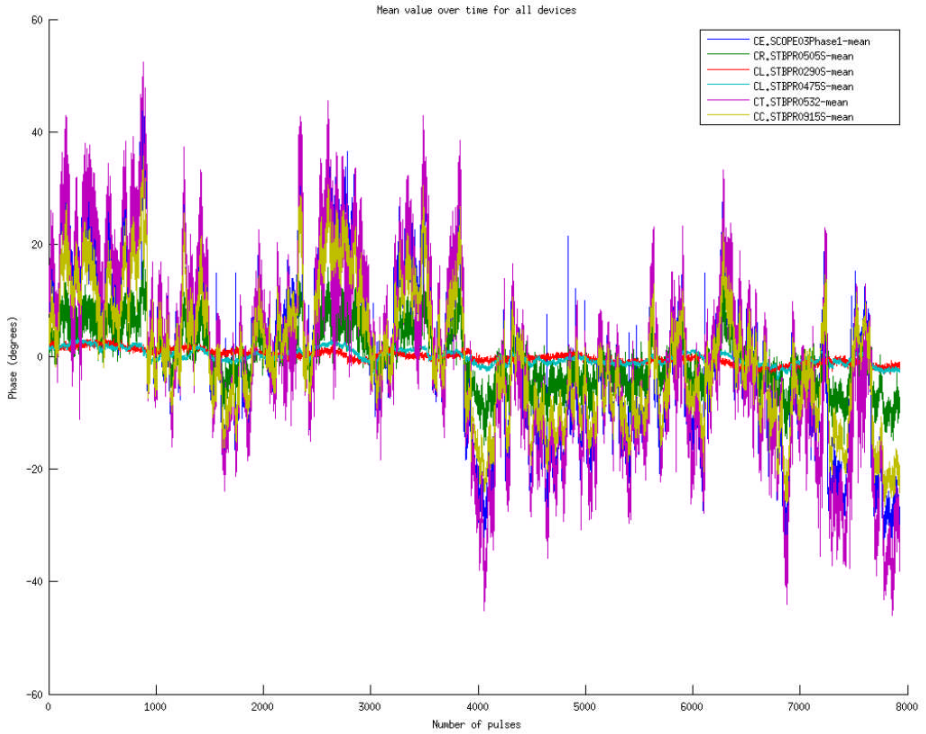
- Phase monitor at end of linac
- Correction in dog leg chicane in TL2 transfer line. Two kickers used to change TOF in chicane (large R52)
- Max kick 1mrad -> Δz = 1.2 mm (~17º at 12 GHz).
- Latency: 380 ns (given by beam TOF through minimum path)
- Demonstrate correction down to 0.2º (@12 GHz) for both uncombined (long pulse) and combined (factor 8) beam
- Oxford hardware deliverables:
  - high power amplifier
  - fast digital board and associated control and DAQ firmware/software

Measurements with existing phase monitors

(Ikarios/Gerbershagen)

Intra-pulse phase error on uncombined beam.
Overall phase sag ~ 20 degrees + fluctuations ~ 10 degrees





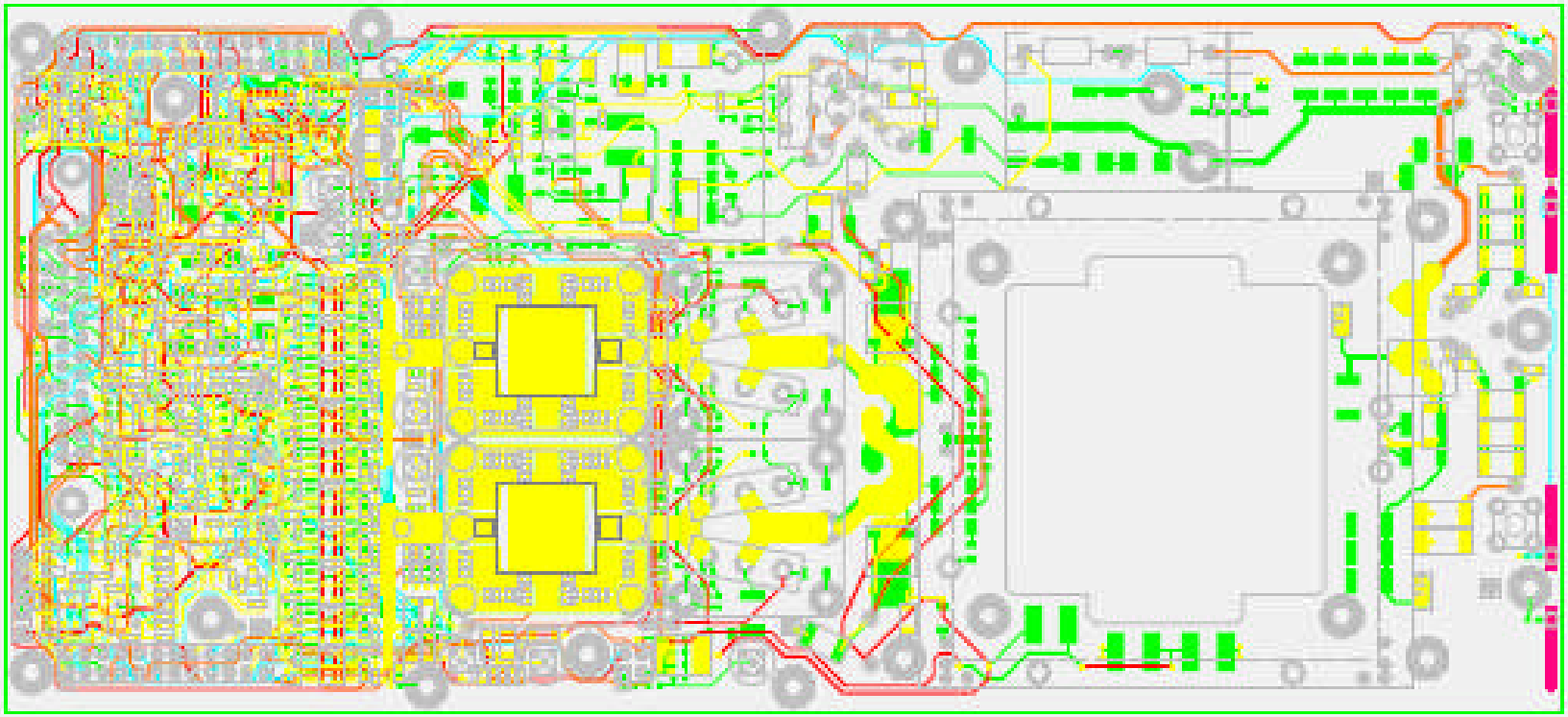
Pulse-to-pulse variation of the mean phase.
~ 20 degree drifts over ~10s of minutes, and oscillation on couple of minutes timescale (cooling water?).

Effects to mitigate slow variations investigated (eg R56 in linac stretching chicane)

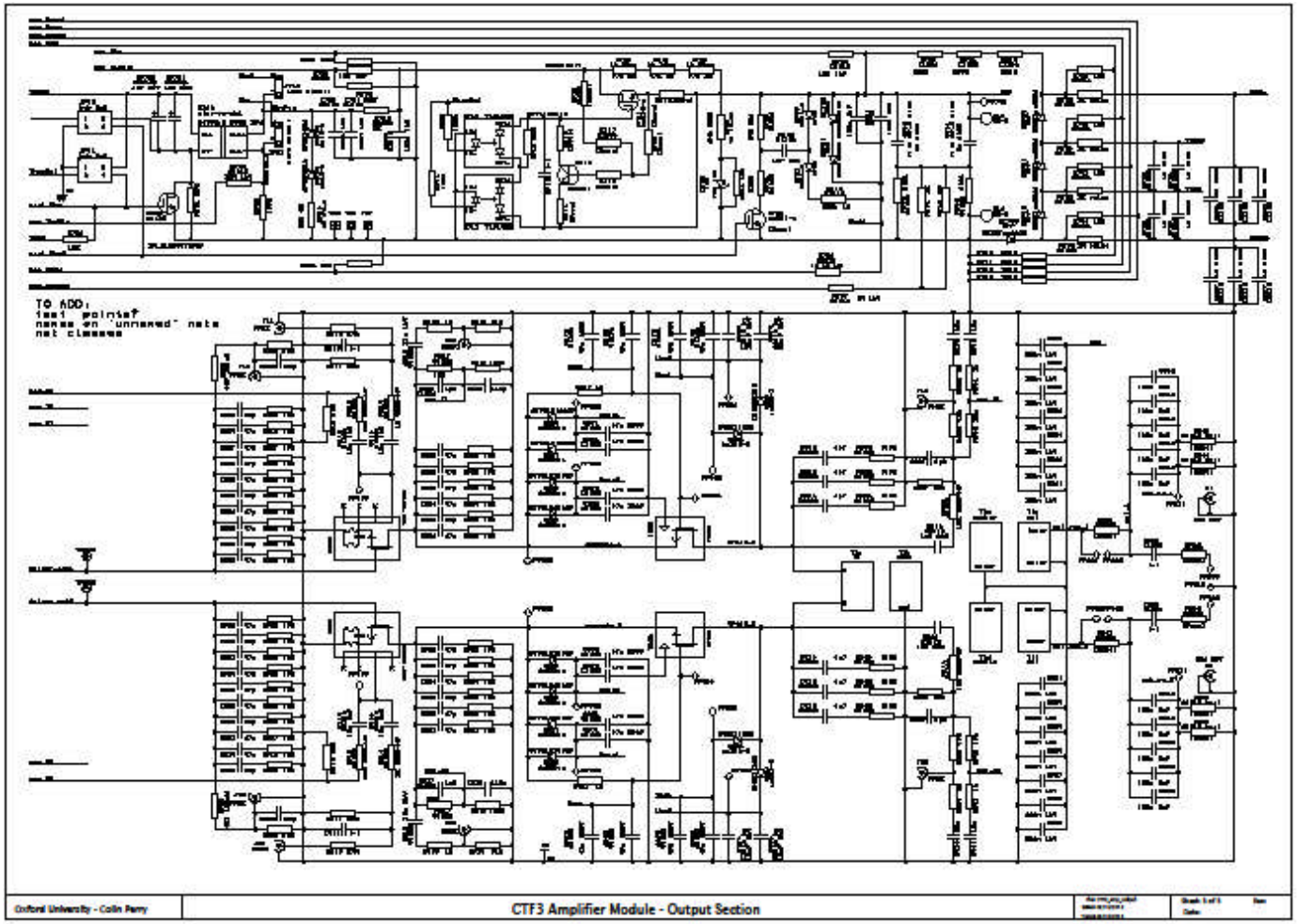
Kicker Drive Amplifier Design

- Designed for high power and high bandwidth
    - 65 kW nominal peak power
    - Bandwidth aim >50 MHz, although slew rate limited.
- Designed for operation over full 1.2 μs un-combined pulse, although full performance guaranteed over ~400 ns portion
    - Output droop limited to 10% across full pulse
- Modular design:
    - Each kicker will have four parallel amplifier modules, one combination module and one drive/control module
    - For initial testing, only one amplifier module per kicker
        - Provide half the total required drive initially
        - Combination module and further amplifier modules to follow afterwards
- Amplifier PCB design and layout complete and in final stages of checking

Kicker Drive Amplifier Layout

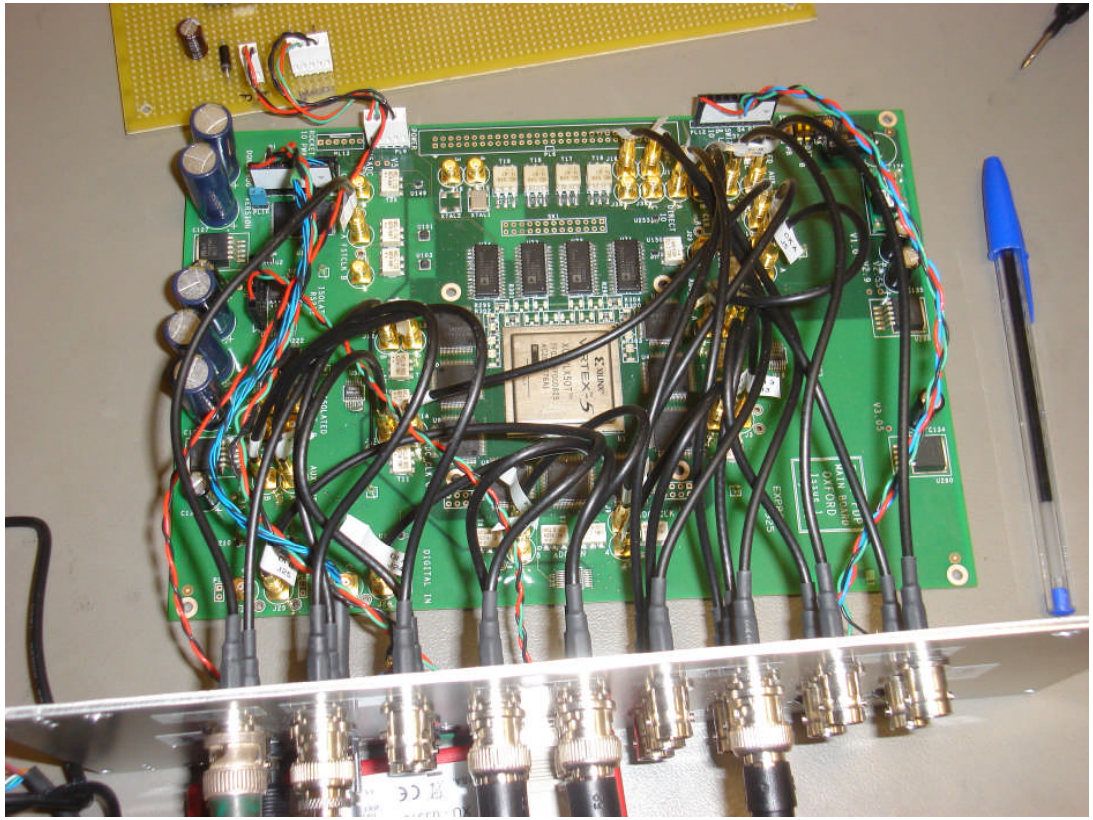


Kicker Drive Amplifier Schematic



FONT5 Digital Signal Processing board

- Based around Xilinx Virtex-5 FPGA (XC5VLXT50)
  - Max speed 550 MHz
  - 2160 Kbit integrated block memory
- 9 ADC channels (3 groups of 3)
  - TI ADS5474
  - 14 bits (only upper 13 connected)
  - Max sampling speed 400 MHz
  - 3.5 clock cycles latency
  - One common clock per ADC group
- 4 DAC channels (2 brought out to front panel by default)
  - Analog Devices AD9744
  - 14 bit (upper 13 connected)
  - Max conversion speed: 210 MHz
  - ~0.5 cycle latency
- UART for serial data TX/RX over RS-232
  - Up to 460.8 kbps
- Fast comparator for external system clock and on-board 40 MHz oscillator for ancillary functions

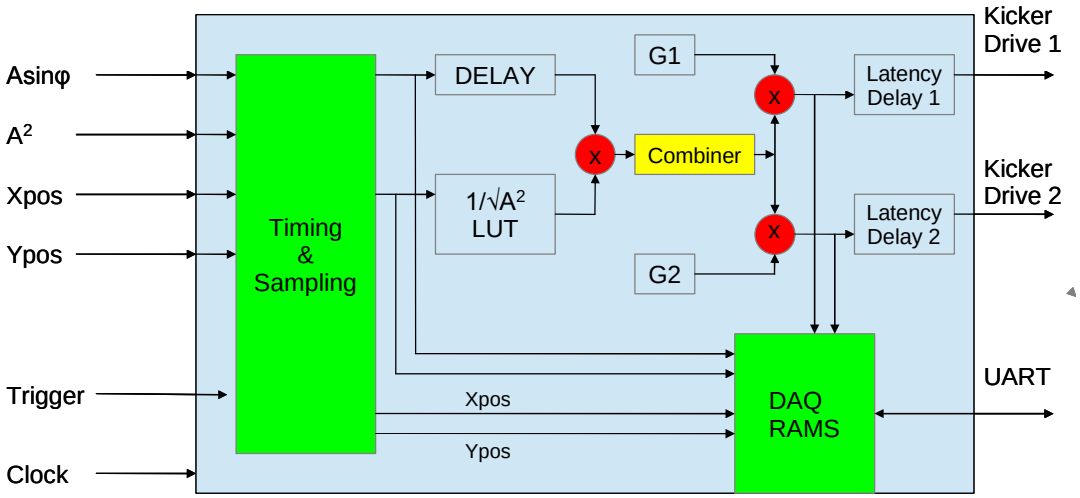


•Currently have two boards but ten new build (FONT5A) boards in production.

•Additional features: USB2 interface to support faster data rate; modified input transformers for CTF3 operation

•At least two boards will stay at CTF3 for Phase FF

FF Digitial Processing Firmware



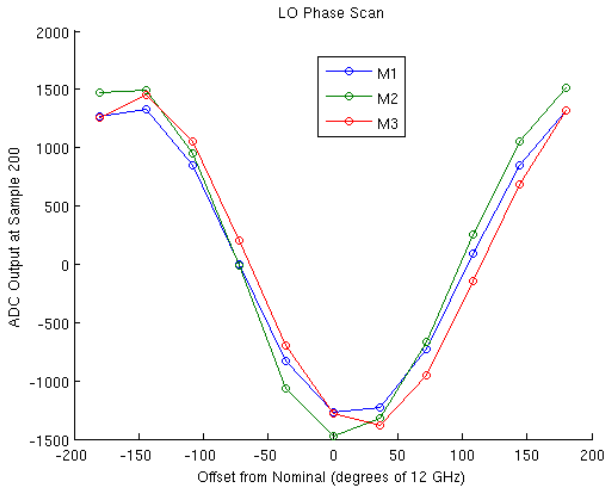
- Designed for both uncombined and combined (factor 8) FF operation
  - For factor 8 beam, mimick the interleaving by averaging respective samples from successive sub-pulse
- Fast sampling clock: 300 MHz target. Allow for multi-sample averaging within correction B/W
- Independent drive and timing for each kicker
- Initial slew rate compensation
  - Allow amplifier to slowly slew to initial phase correction
- Digital filtering
  - Anti-droop exponential (IIR) filter on inputs to correct for AC coupling of inputs
  - Variable depth moving averaging FIR on outputs
  - Possibility of extending to adaptive filtering to correct for non-linear amplifier response.

Current status of CTF3 Phase FF

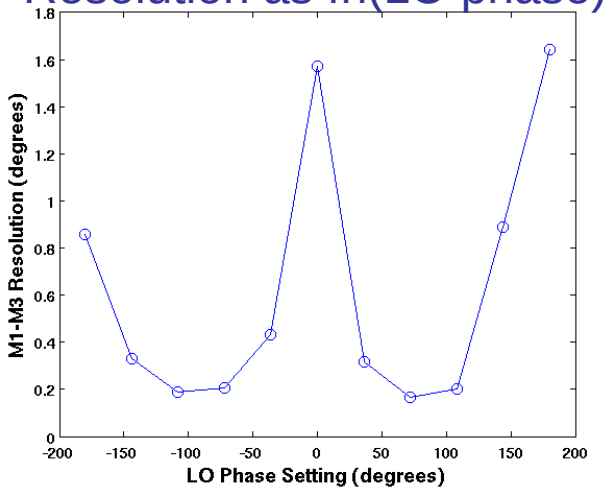
- Beamline installation (summer 2013)
  - Kickers installed in CTF3 dog-leg and magnet locations rearranged for phase FF tests
  - Kicker drive cables installed between chicane and klystron gallery
  - Phase monitors installed: FF control monitor upstream of delay loop, witness monitor downstream of dog-leg chicane
    - Third (witness) monitor for post combiner ring, to be returned to INFN for re-work
- Firmware and Data Acquisition software in later stages of development
  - Sampling and DAQ tests made with FONT5 digital processors and INFN phase monitors in May 2013
- Drive amplifier boards out for production imminently
- Aiming for delivery of amplifiers in ~ 1 month time

FONT5 digitiser tests at CTF3

Calibration Scan

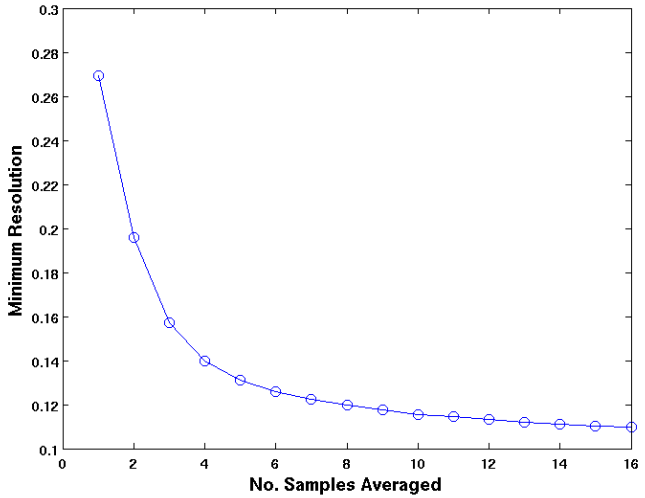


Resolution as fn(LO phase)



- May 2013 – opportunity to make tests of FONT5 digitiser system at CTF3 whilst three monitors installed at same location in CTF3 linac
- Calibrated the phase by sweeping the LO phase over full 360 degrees
- Resolution: compared output of two monitors measuring same input
- Minimum resolution of 0.2 degrees obtained at optimal working point of monitors.

Resolution with averaging



Phase FF plans (1)

- Pre- FF startup
  - Commission optics in new chicane layout with dipole correctors
  - Study phase monitor response and check phase transportation between control and witness monitor location
  - Stabilise pulse-pulse phase variations with slow (several cycle) dipole-corrector based FB
  - Check operation and performance of digital processors
    - New input coupling transformers
    - Check logic for FF operation

Phase FF plans (2)

- First tests with fast FF amplifier
  - Confirm optics with FF amplifier
  - Check phase monitor bandwidth (phase response to fast kick)
  - Measure closed-loop latency
    - If present cable delays too large:
      - For uncombined beam : delay beam in DL and/or CR (short pulse only – 280 ns limit)
      - For combined beam : calculate partial average, i.e. disregard contribution from final sub-pulse(s)
  - Initially, drive limited to ~10 degrees
    - Aim to demonstrate correction over 280-420 ns segment of uncombined pulse
    - First investigations of FF performance on combined (factor 8) beam
      - Limited due to unavailability of third (witness) monitor
- 2013/14 winter shutdown
  - Assess system latency and re-route cables if necessary
  - Assess performance of fast amplifier prototype
    - Proceed with further amplifier and drive combination modules for full drive power
  - Install third monitor in CTF3 as upstream witness, if ready

Phase FF plans (3)

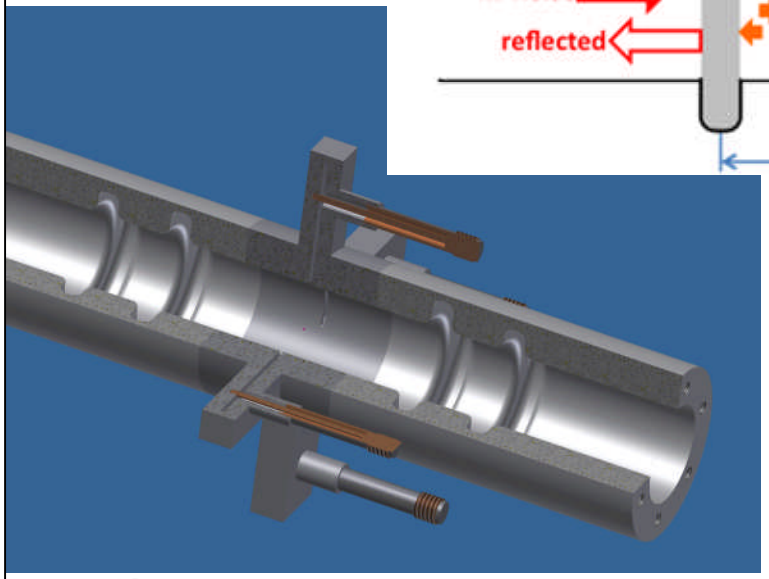
- Longer term plans
  - Difficult to predict longer terms requirements until start making experiments with system
  - Providing hardware works as expected:
    - Demonstrate full drive performance of phase FF system on both uncombined and combined beam
    - Demonstrating ultimate resolution of the system
      - May require more sophisticated digital signal processing, eg adaptive filtering to overcome potential amplifier non-linearity
  - Engineering design and cost optimisation for CLIC specific system, based on experience with CTF3 system
    - Improved power bandwidth
    - Possible tests of prototypes at CTF3
    - Provide engineering solutions for a future TDR

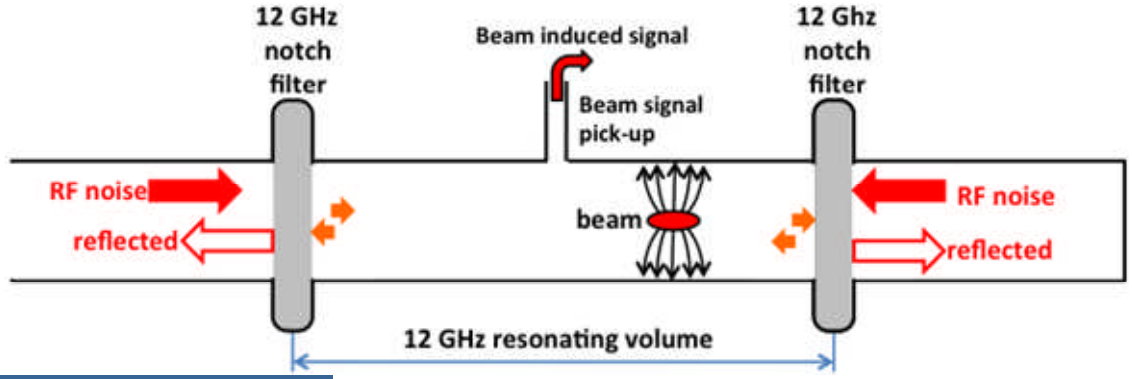
Extras

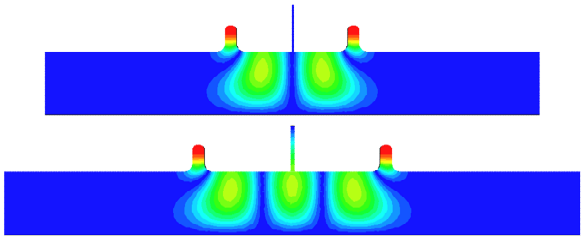
Phase Monitors

LNF/INFN Frascati

- 12GHz RF pickups using a choke mode cavity
  - 30MHz bandwidth
  - 0.2° at 12GHz resolution







Skowronski, IPAC13 talk

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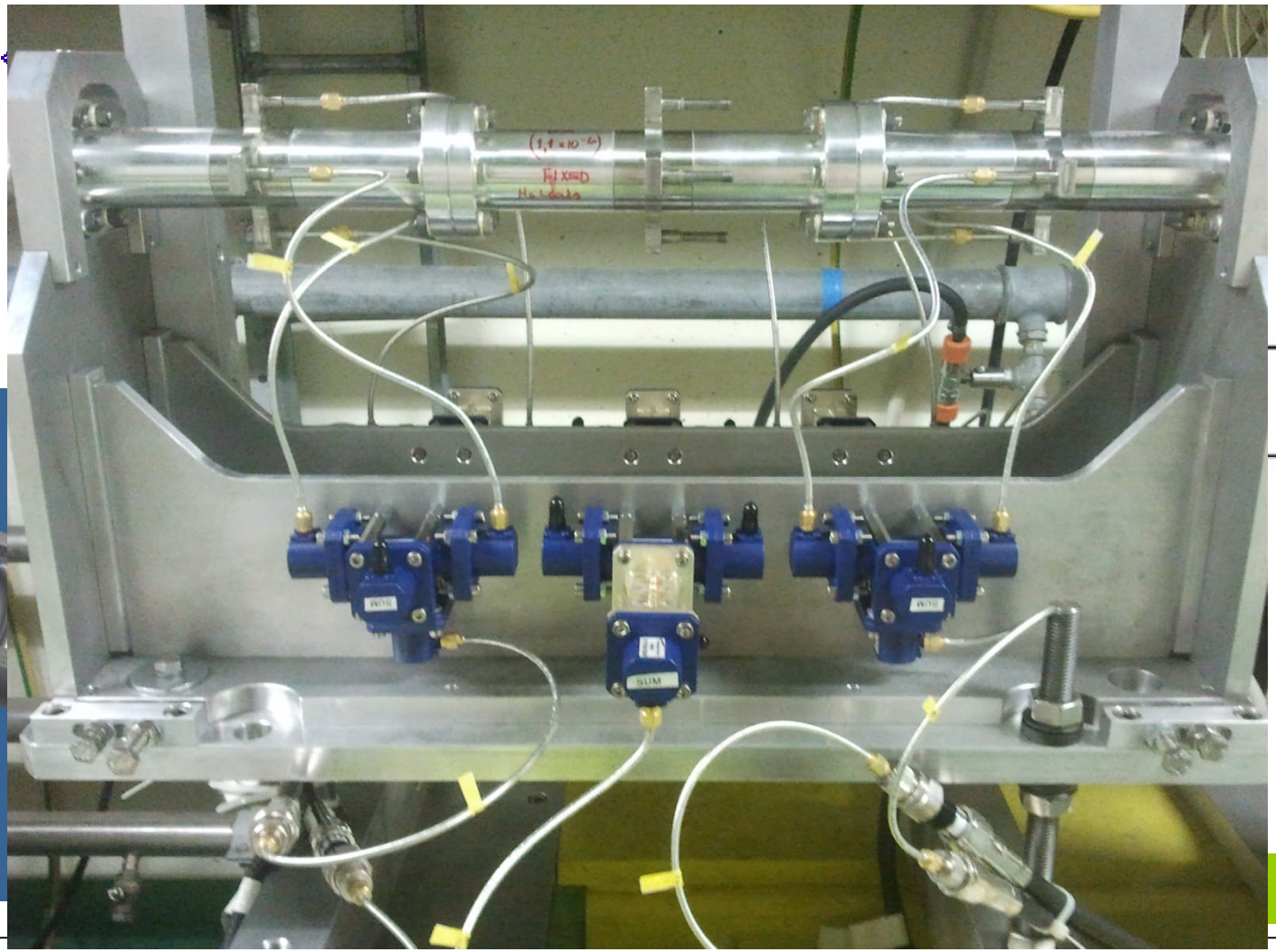
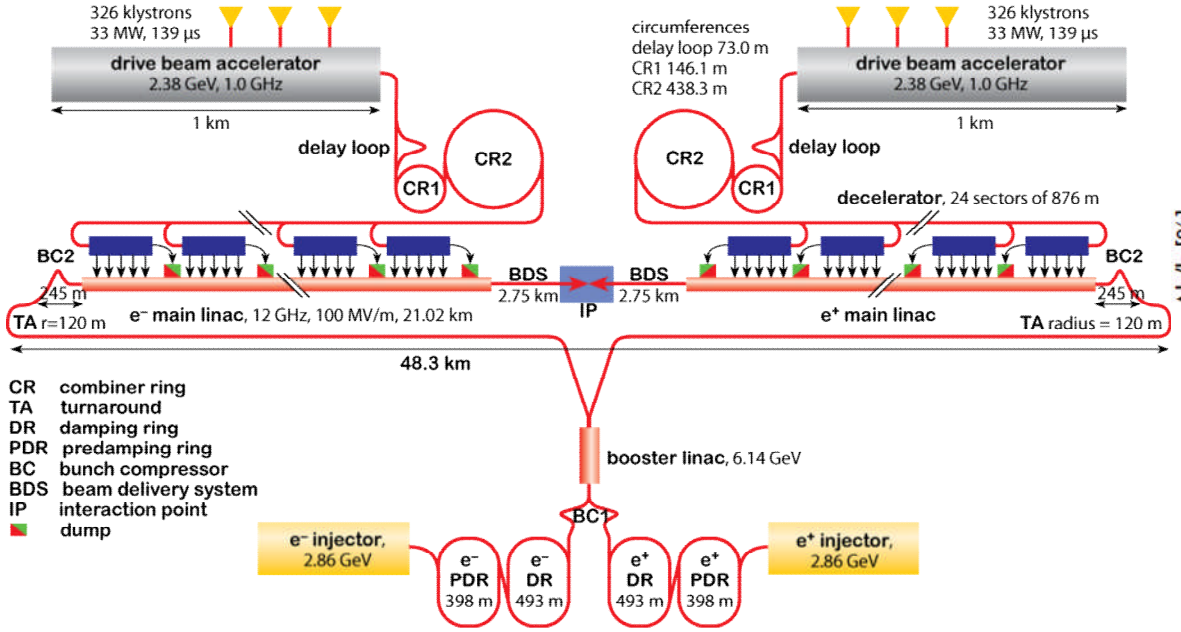
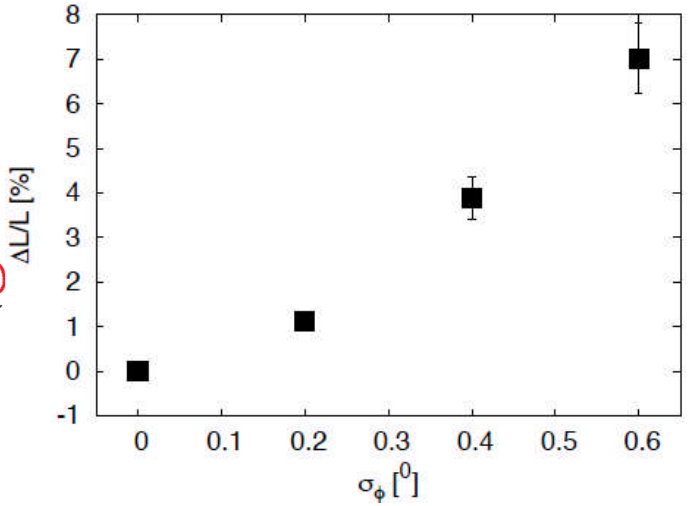
Phase Monitors

LNF/INFN Frascati



CLIC drive beam phase Feed-forward





- Problem: For efficient transfer of energy, phase of the decelerated drive beam should precisely match the arrival of the main beam at the cavities.
  - Phase error > 0.2º (46 fs @ 12 GHz) leads to luminosity loss > 2 %.
  - Goal: implement system to detect and correct phase error down to less than 46 fs.
  - Collaboration between CERN, JAI, and INFN Frascati

Amplifier & Kickers

Kicker drive amplifier (JAI, Oxford):

• Designed for high power and high bandwidth

•65 kW nominal peak power

•Designed for operation over full 1.2 μs un-combined pulse, although full performance guaranteed over ~400 ns portion

•Output droop limited to 10% across full pulse

•Bandwidth aim >50 MHz, although slew rate limited.

•Delivery expected late summer/ early autumn

Kickers (INFN):

•2 x ~1m long stripline kickers based on DAFNE design

•1 mrad deflection for ~1.3 kV drive at 125 MeV