The Development of Large-Area Psec-Resolution TOF Systems

Henry Frisch

Enrico Fermi Institute and Physics Dept

University of Chicago

With Karen Byrum and Gary Drake (ANL); Tim Credo, Harold Sanders, and Fukun Tang (UC)

What is the intrinsic limit for TOF for rel. particles?

Typical path lengths for light and electrons are set by physical dimensions of the light collection and amplifying device.

These are now on the order of an inch. One inch is 100 psec. That's what we measure- no surprise! (pictures swiped from T. Credo talk at Workshop)
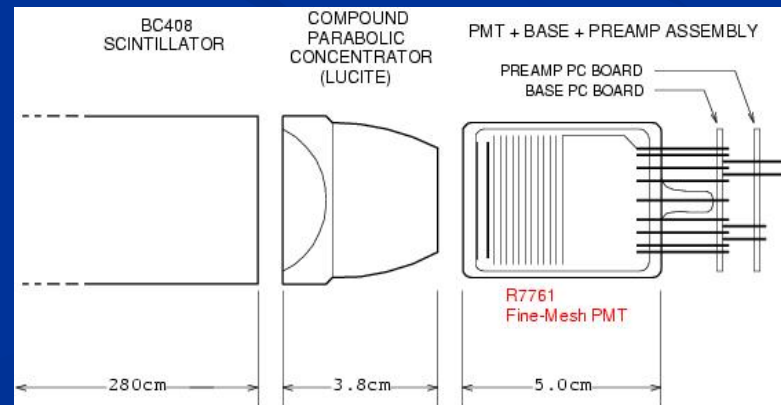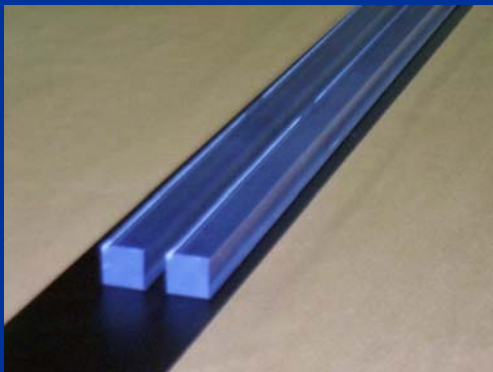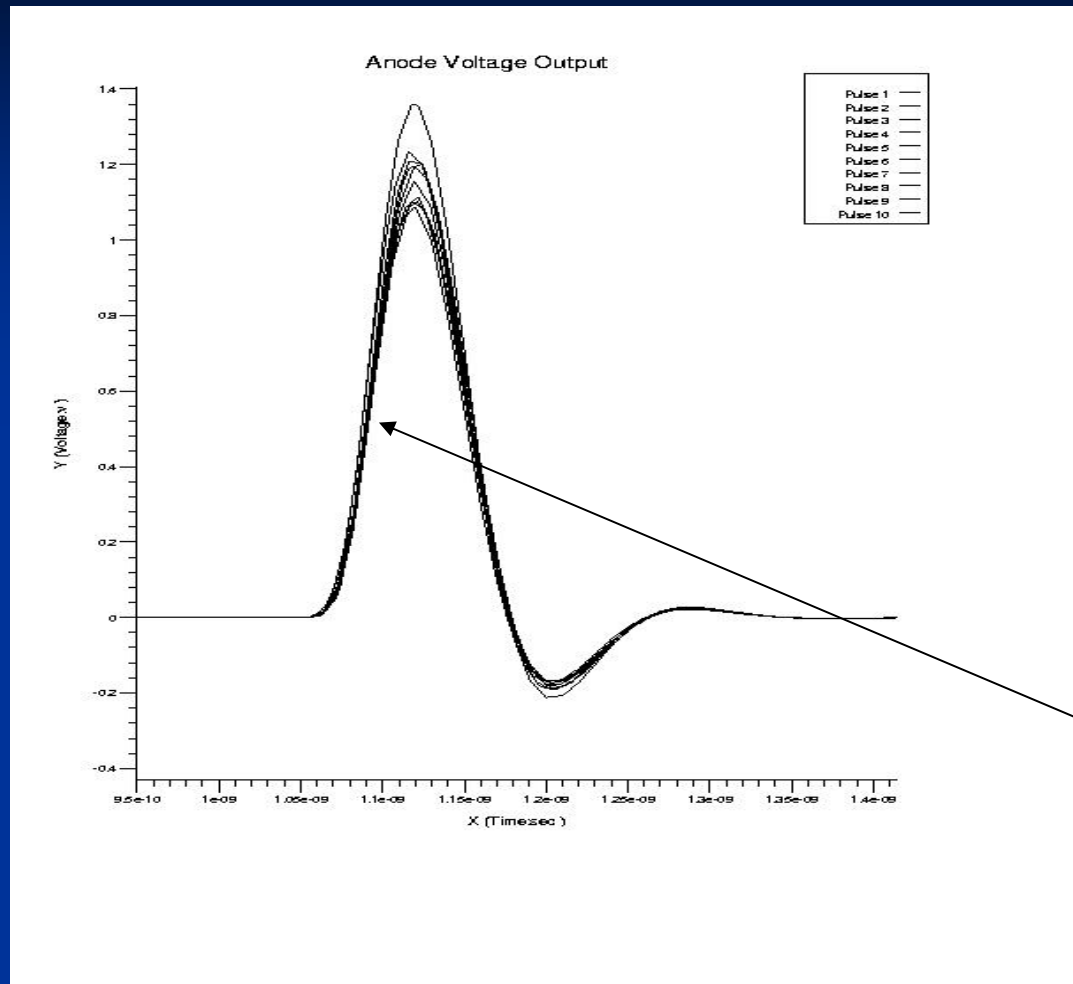
Major advances for TOF measurements:
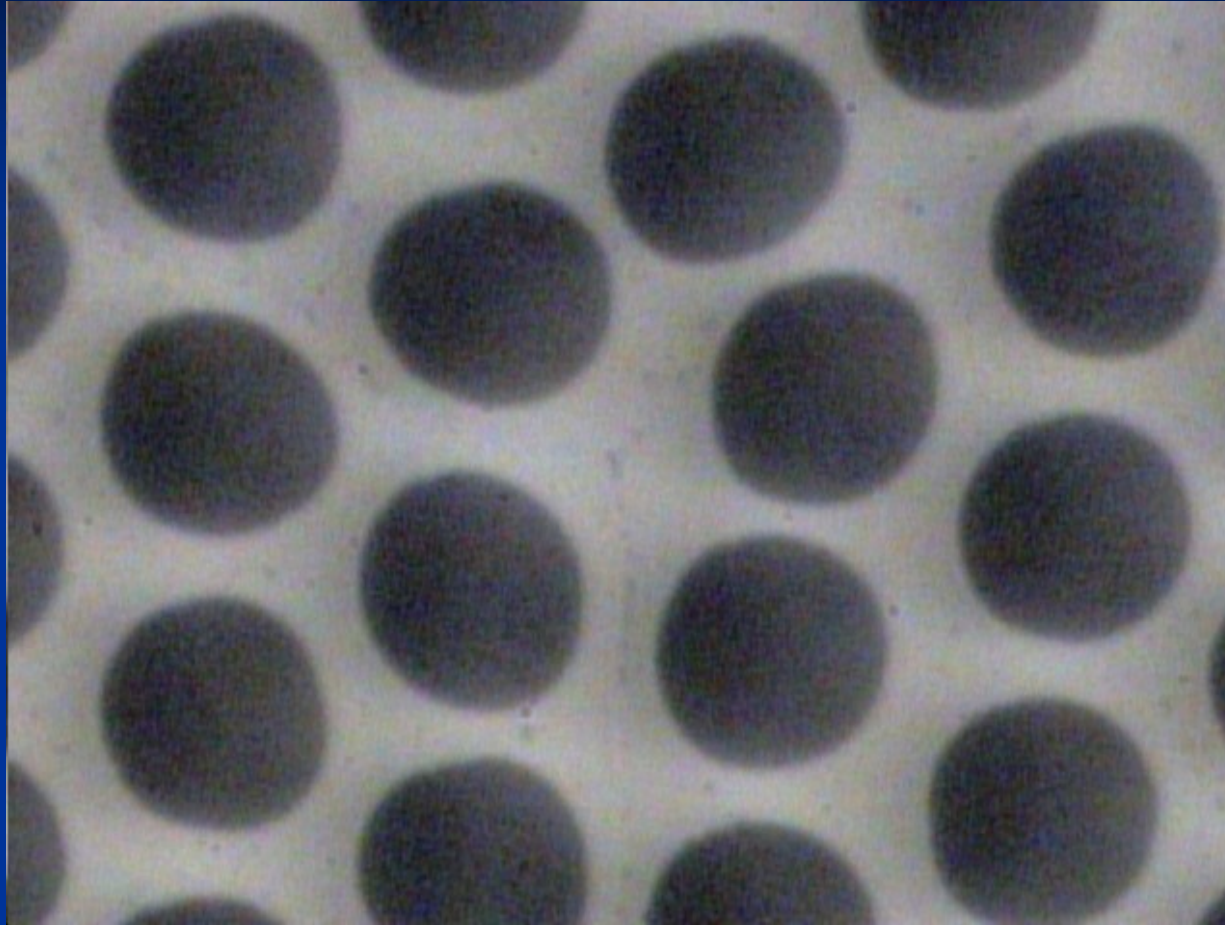
Micro-photograph of Burle 25 micron tube- Greg Sellberg (Fermilab)

1. Development of MCP's with 6-10 micron pore diameters

Major advances for TOF measurements:

Anode Voltage Output

Output at anode from simulation of 10 particles going through fused quartz window- T. Credo, R. Schroll
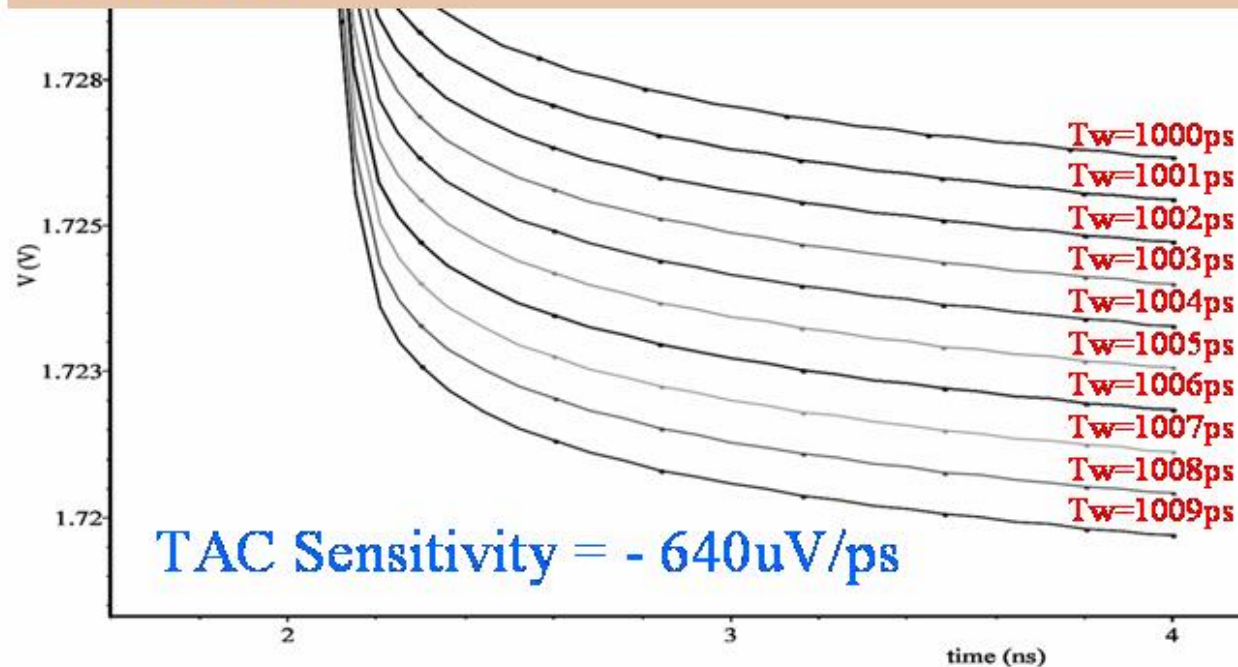
Jitter on leading edge 0.86 psec

2. Ability to simulate electronics and systems to predict design performance

Major advances for TOF measurements:

SIM-IV: TAC Outputs vs. Tw Inputs
Sweep Tw from 1ns to 1.01ns with 1ps Increment
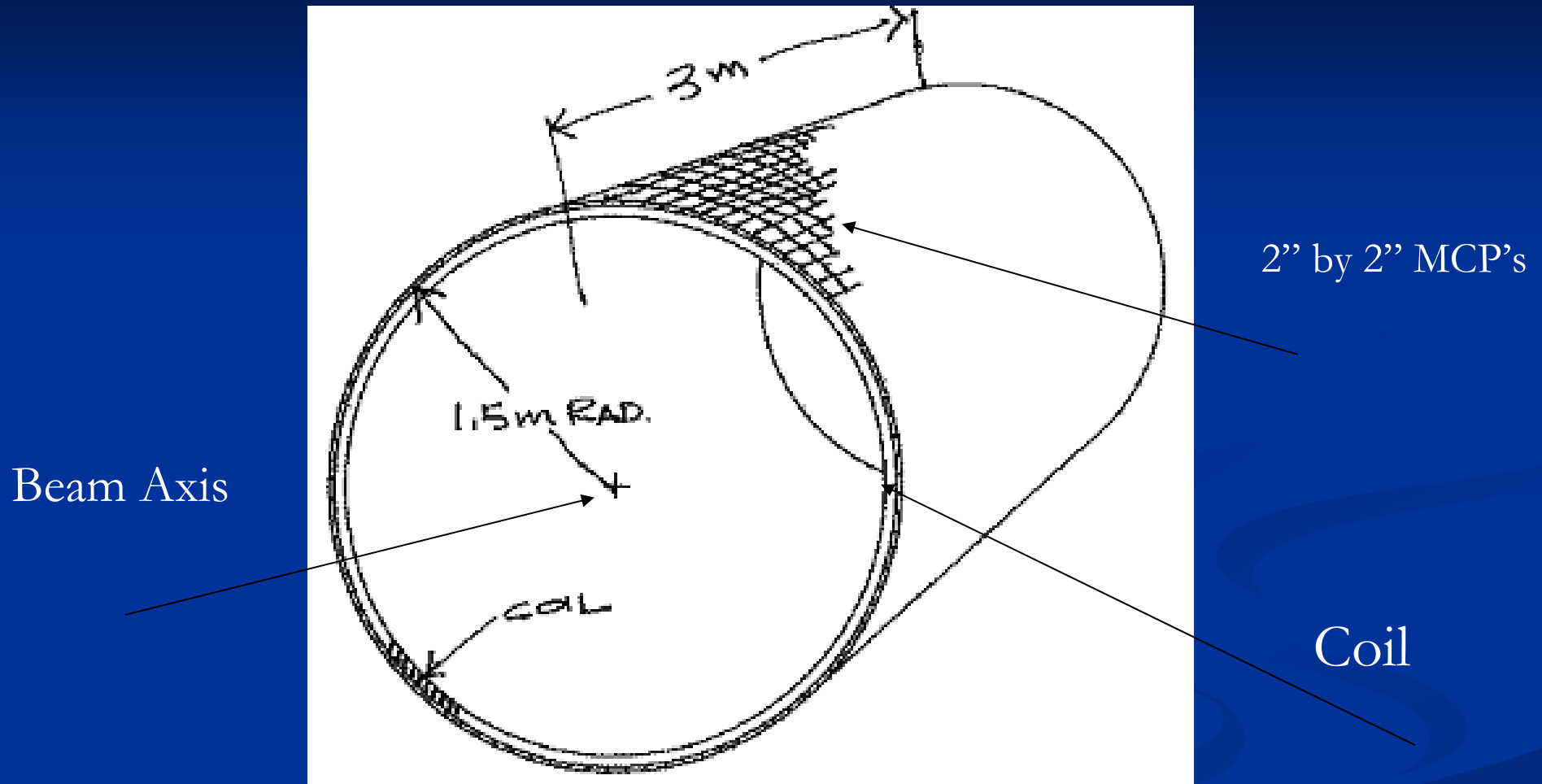
Tw=1000ps
Tw=1001ps
Tw=1002ps
Tw=1003ps
Tw=1004ps
Tw=1005ps
Tw=1006ps
Tw=1007ps
Tw=1008ps
Tw=1009ps

TAC Sensitivity = - 640uV/ps

Simulation with IHP process- Fukun Tang (UC)

3. Electronics with typical gate jitters << 1 psec

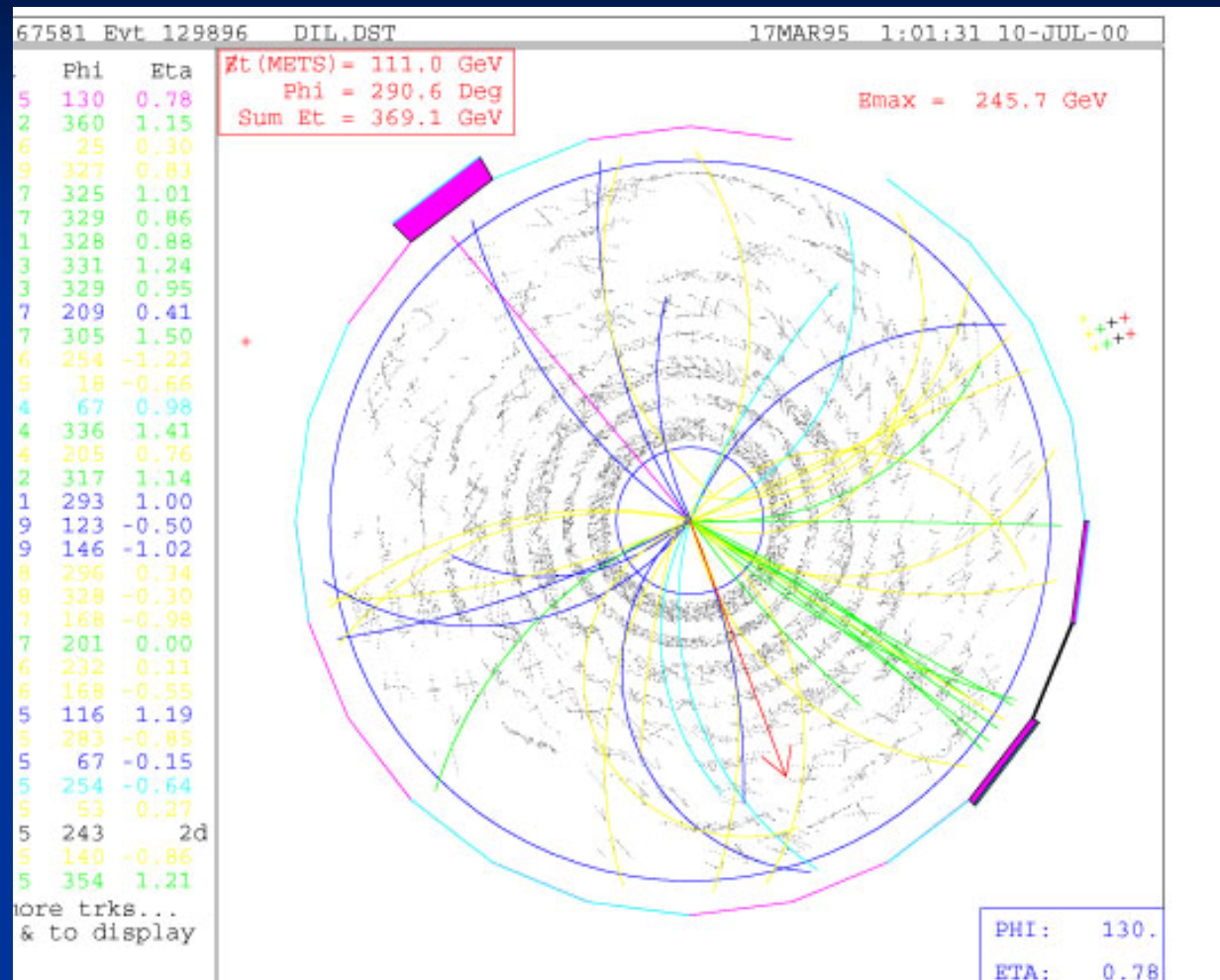# Geometry for a Collider Detector

Beam Axis

2" by 2" MCP's

Coil

"r" is expensive- need a thin segmented detector

Measure track length with high precision
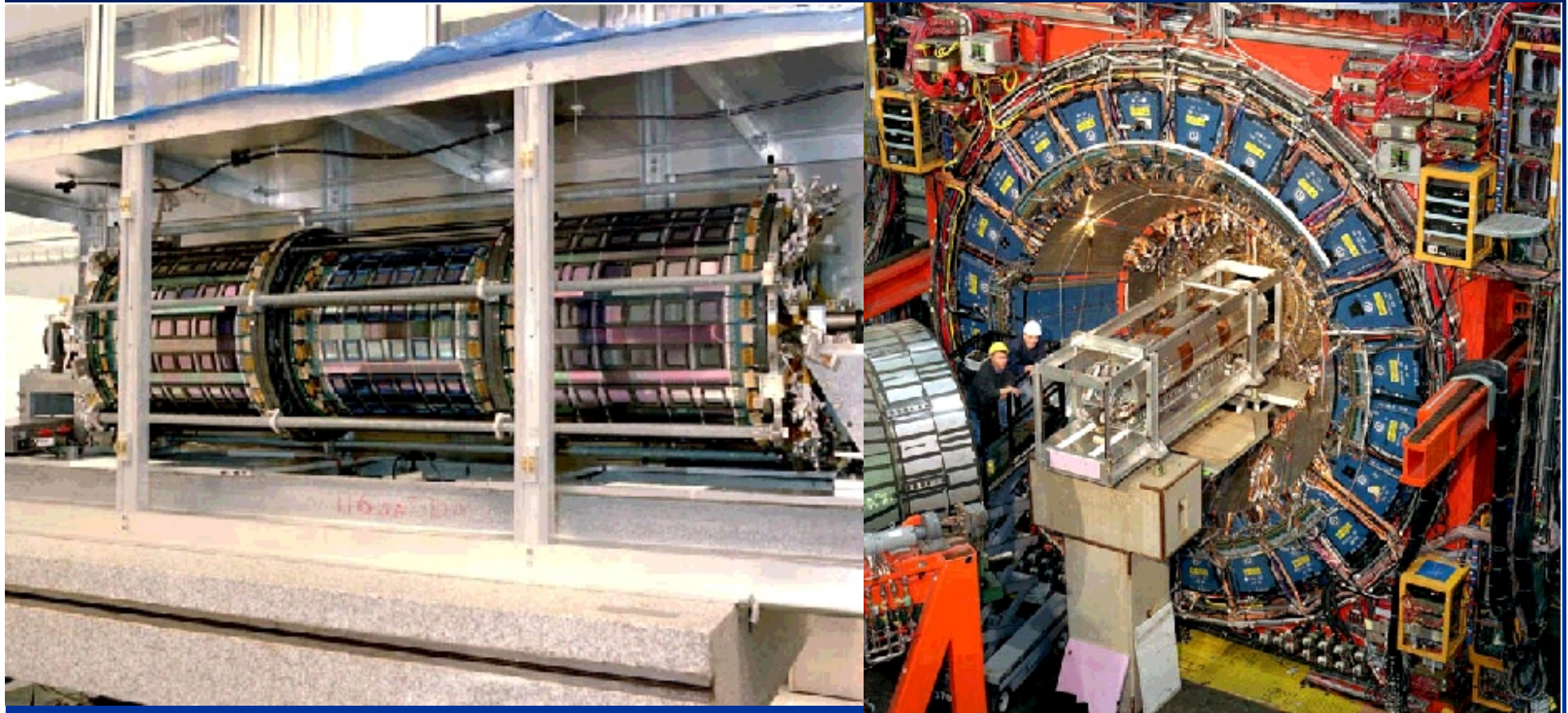
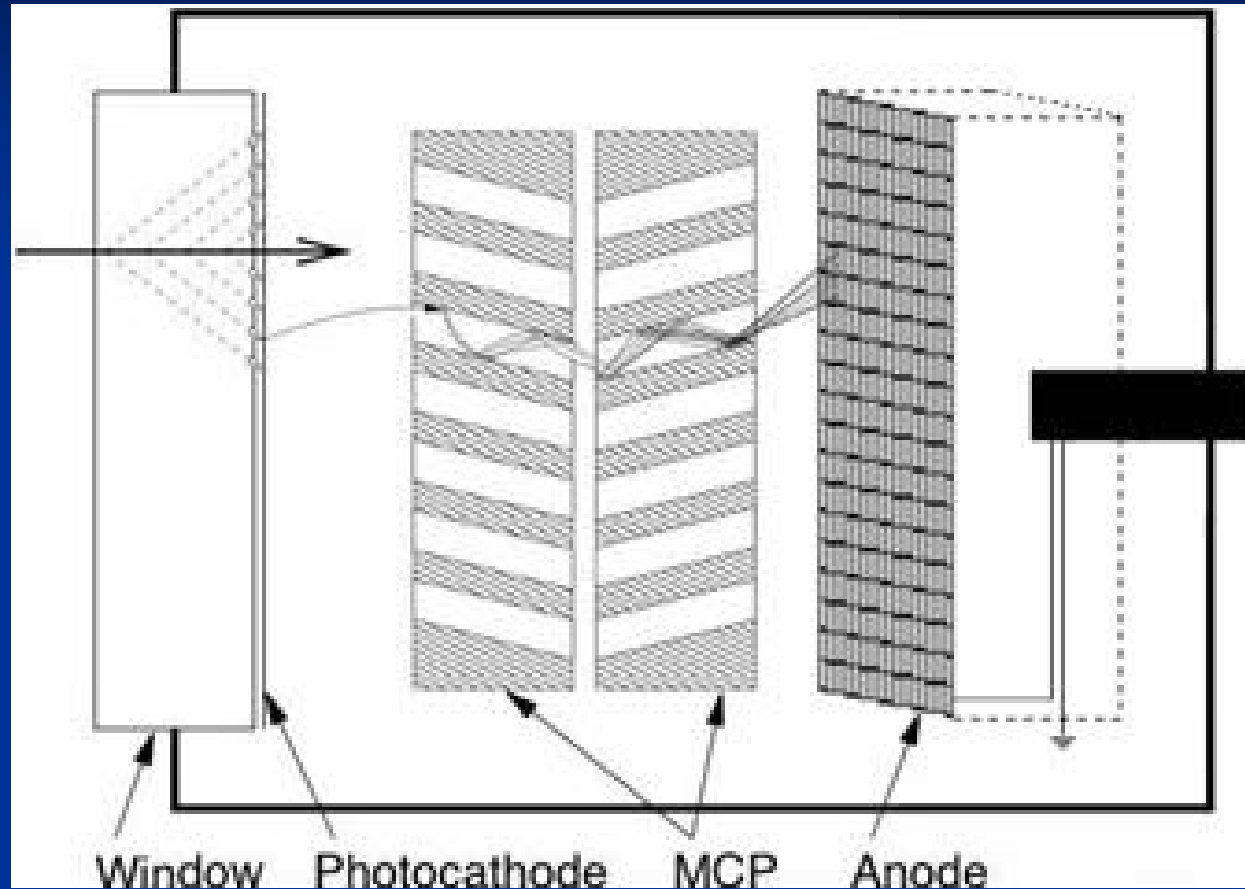Silicon Detectors with ~10 micron spatial resolution+ magnetic spectrometer

A real CDF event- r-phi view
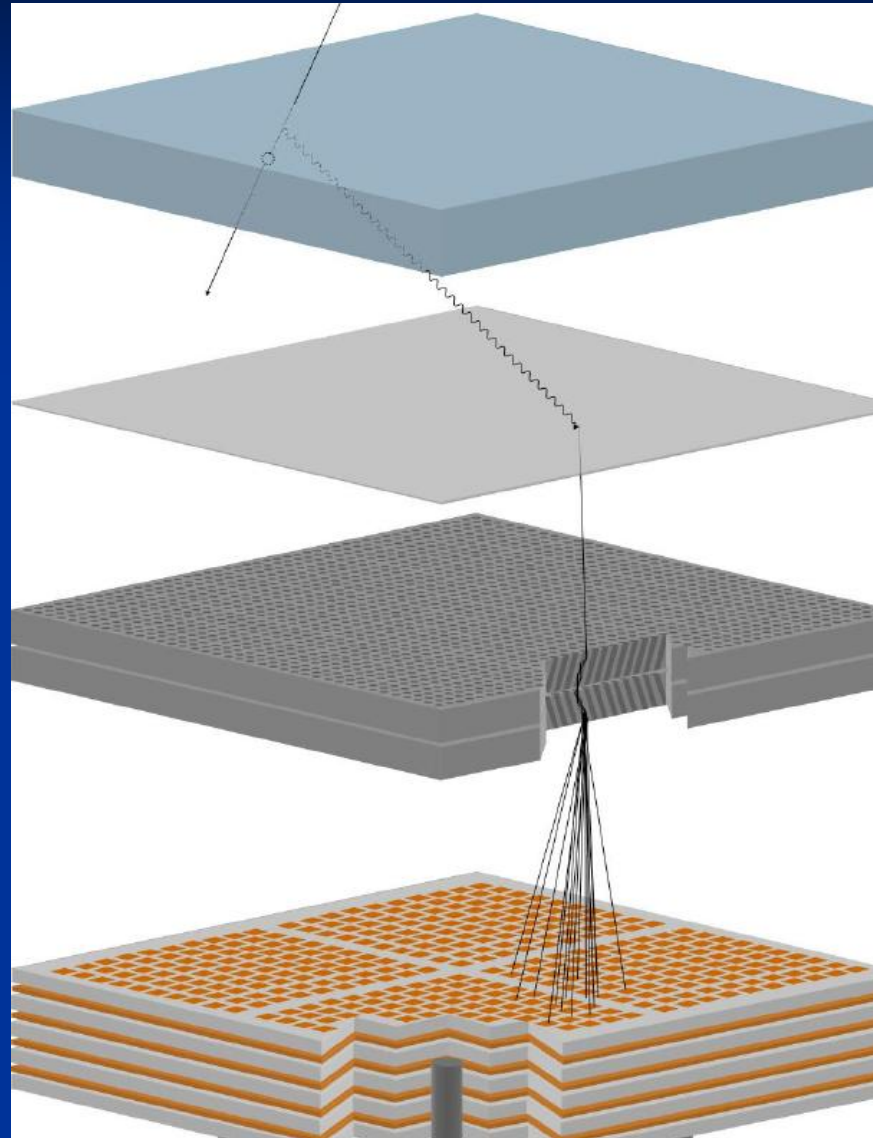

Key idea- fit t_0 (start) from all tracks

Generating the signal

Window   Photocathode   MCP   Anode

Use Cherenkov light - fast

Anode Structure

1. RF Transmission Lines

2. Summing smaller anode pads into 1" by 1" readout pixels

3. An equal time sum- make transmission lines equal propagation times

4. Work on leading edge- ringing not a problem if segmentation is fine enough (5 particles/unit rapidity/collision)

Mounting electronics on back of MCP- matching

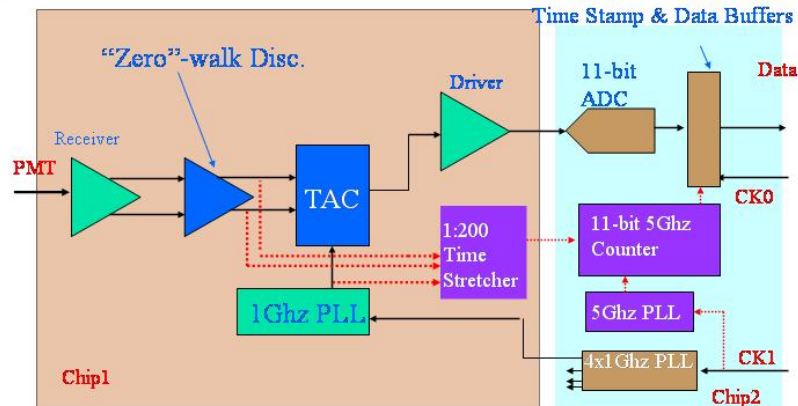Conducting Epoxy- machine deposited by Greg Sellberg (Fermilab)
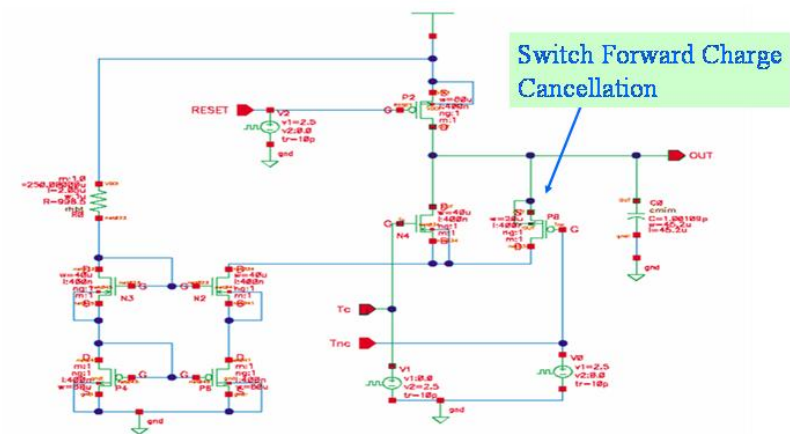
Harold's TOF System
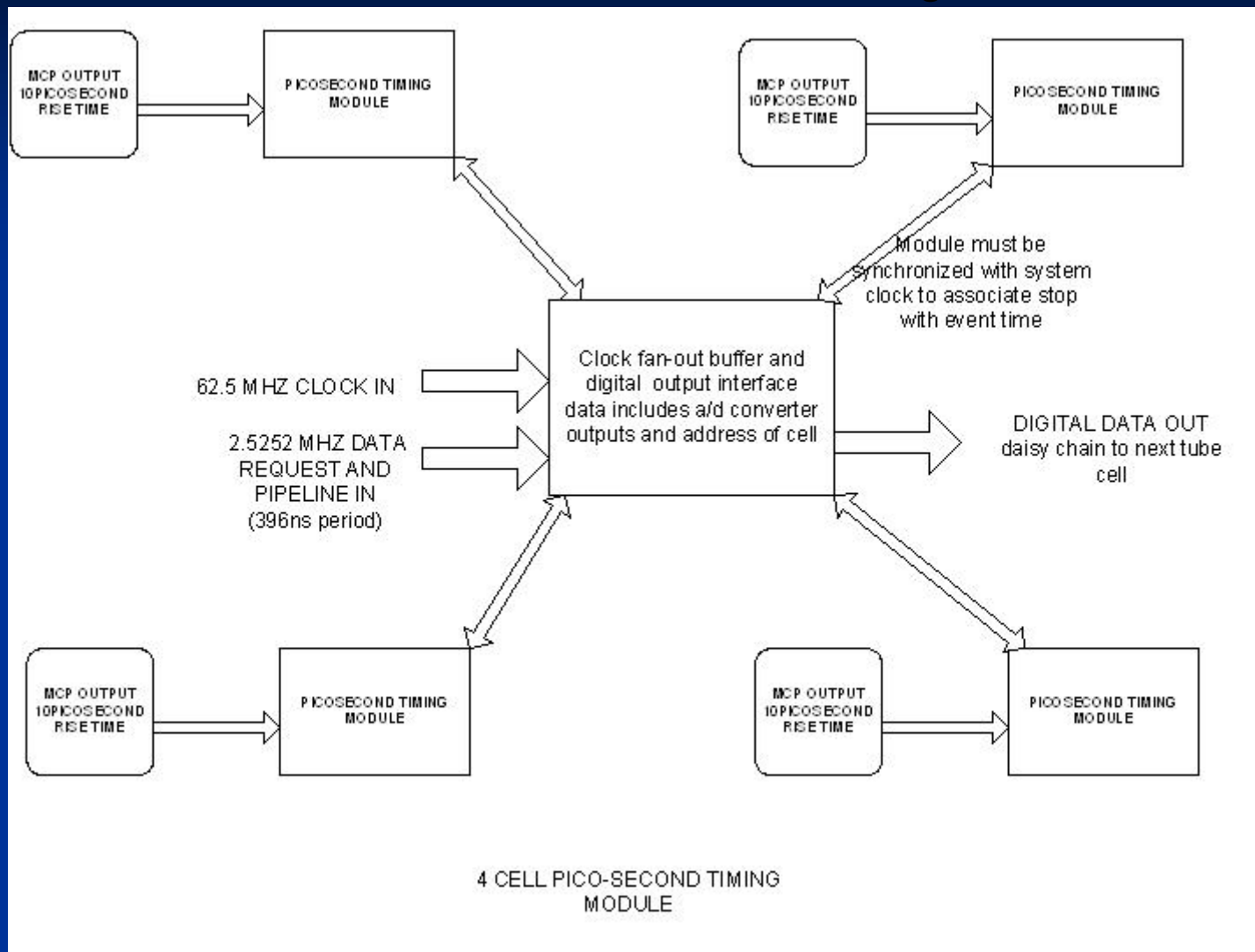
Tang's work in IHP design tools

Approaches & Possibilities
From Harold's talk, we will build two Chips for Tube Readout
(1) psFront-end   (2) psTransport

SIM-IV: Time-to-Amplitude (TAC) Schematics
Based on IHP 0.25μm BiCMOS Process

Switch Forward Charge Cancellation

SIM-II: Zero-Crossing Voltage Comparator Schematics
Based on IHP 0.25μm BiCMOS Process
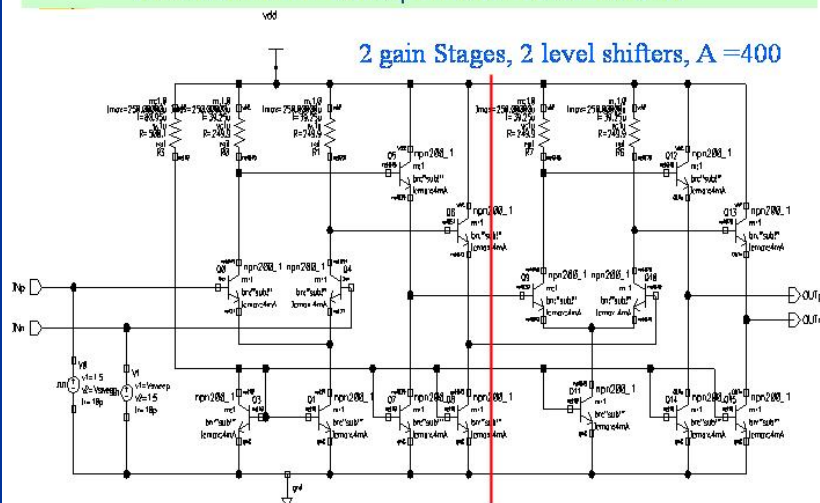
2 gain Stages, 2 level shifters, A =400

SIM-IV: TAC Outputs vs. Tw Inputs
Sweep Tw from 1ns to 1.01ns with 1ps Increment

Tw=1000ps
Tw=1001ps
Tw=1002ps
Tw=1003ps
Tw=1004ps
Tw=1005ps
Tw=1006ps
Tw=1007ps
Tw=1008ps
Tw=1009ps

TAC Sensitivity = - 640uV/ps
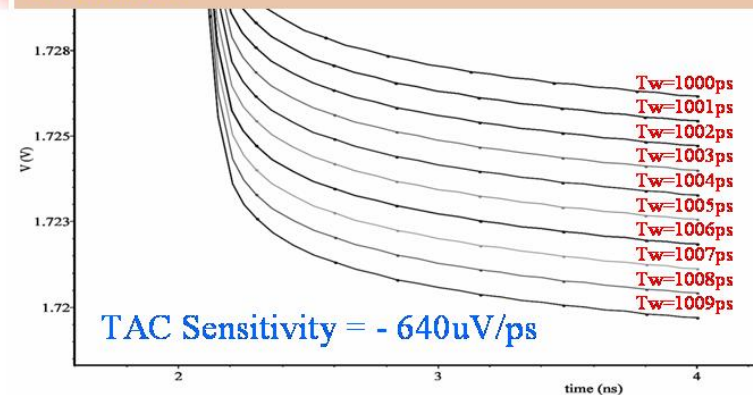
Tim's Equal-Time Collector

Equal time transmission-line trace
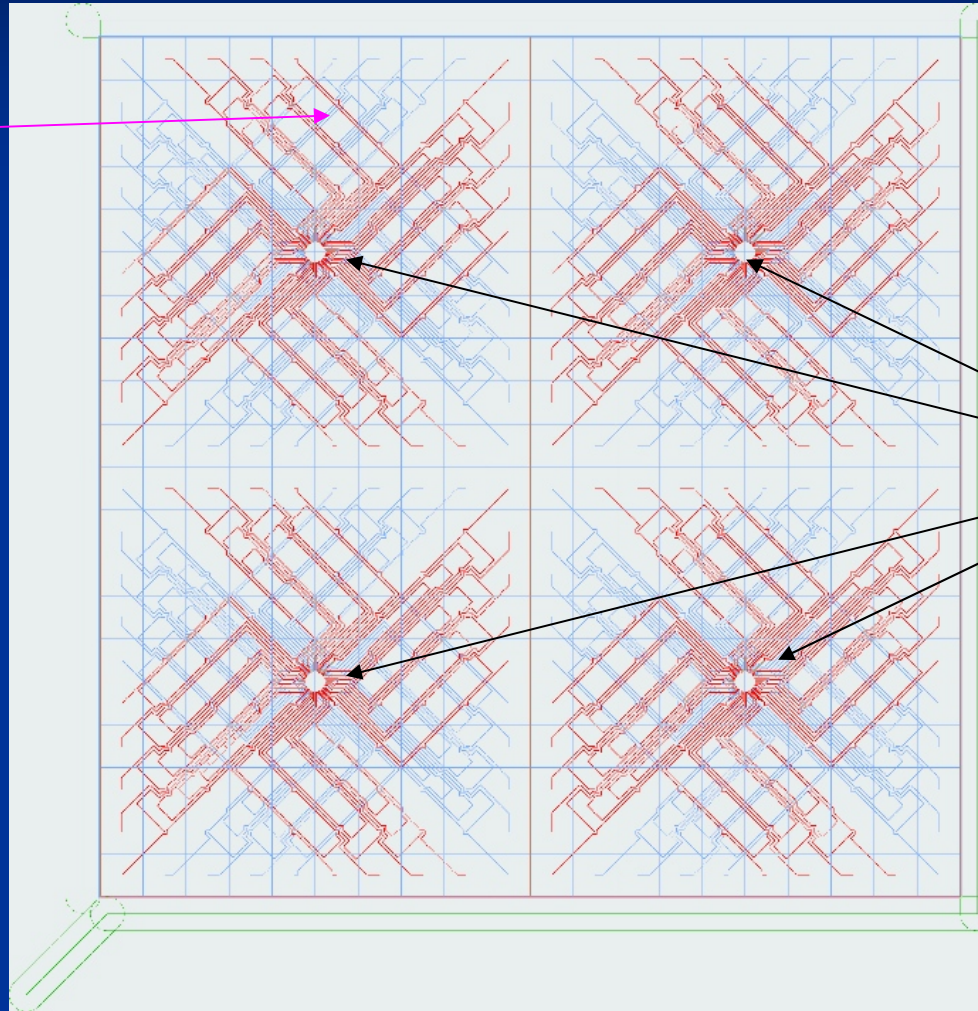
4 Output points each to a TDC chip

Whuffor?

• Kaon ID in same-sign tagging in B physics (X3 in power in CDF Bs mixing analysis)

• Separating b from b-bar in measuring the top mass (lessens combinatorics

• Identifying csbar and udbar modes of the W to jj decays in the top mass analysis (need this once one is below 1 GeV, I belive

• Separating out vertices from different collisions at the LHC in the z-t plane

• Identifying photons with vertices at the LHC (requires spacial resolution and converter ahead of the TOF system

• Locating the Higgs vertex in H to gamma-gamma events at the LHC (mass resolution)

• Fixed target geometries- LHCb, kaon experiments, etc.

• Super-B factory

• Etc.- this is an area that needs work in collaboration with theorists

• Non-HEP uses- PET, astro, nuclear, … (see UC workshop web page for examples)

Successes

1. Have a simulation of Cherenkov radiation in MCP- out to anode

2. Have placed an order with Burle- have the 1st of 4 tubes and have a good working relationship (their good will and expertise is a major part of the effort)

3. Have licence and tools from IHP working on our work stations- Tang is adept and fast working with them. Looks good (so far)

4. Have modeled DAQ/System chip in Altera (Jakob Van Santen- 4th yr).

5. ANL has put together a test stand with working DAQ, identified a laser and is ordering it, has made contact with advanced accel folks, etc.

6. We have 3D EM frequency-domain modelling software to find the Green's function for a duck, model the MCP/anode/collector, etc.

7. Harold and Tang have a good grasp of the overall system problems and scope, and have a top-level design plus details

8. Have found Greg Sellberg at Fermilab to offer expert precision assembly advice and help (wonderful tools and talent!).

The Hard Parts- Reality

1. Haven't yet plugged in a device- all simulation

2. Harold and Paul Mitchell (Burle) have taught us that the hard part is the return path from MCP-OUT to the Gd

3. Paul also says that capacitive coupling of the signal from MCP out is visible- we need to understand the circuit.

4. Haven't yet submitted a design to IHP- don't know the realities of making chips

5. Have no idea, and no equipment, on how to test these chips when we get them

6. Have ideas, but not real ones, on how to measure device performance when we actually get them.

Last week- got Burle MK-0 (our name)- many thanks!

- Paul Mitchell has done nice things- wonderful test bed for understanding
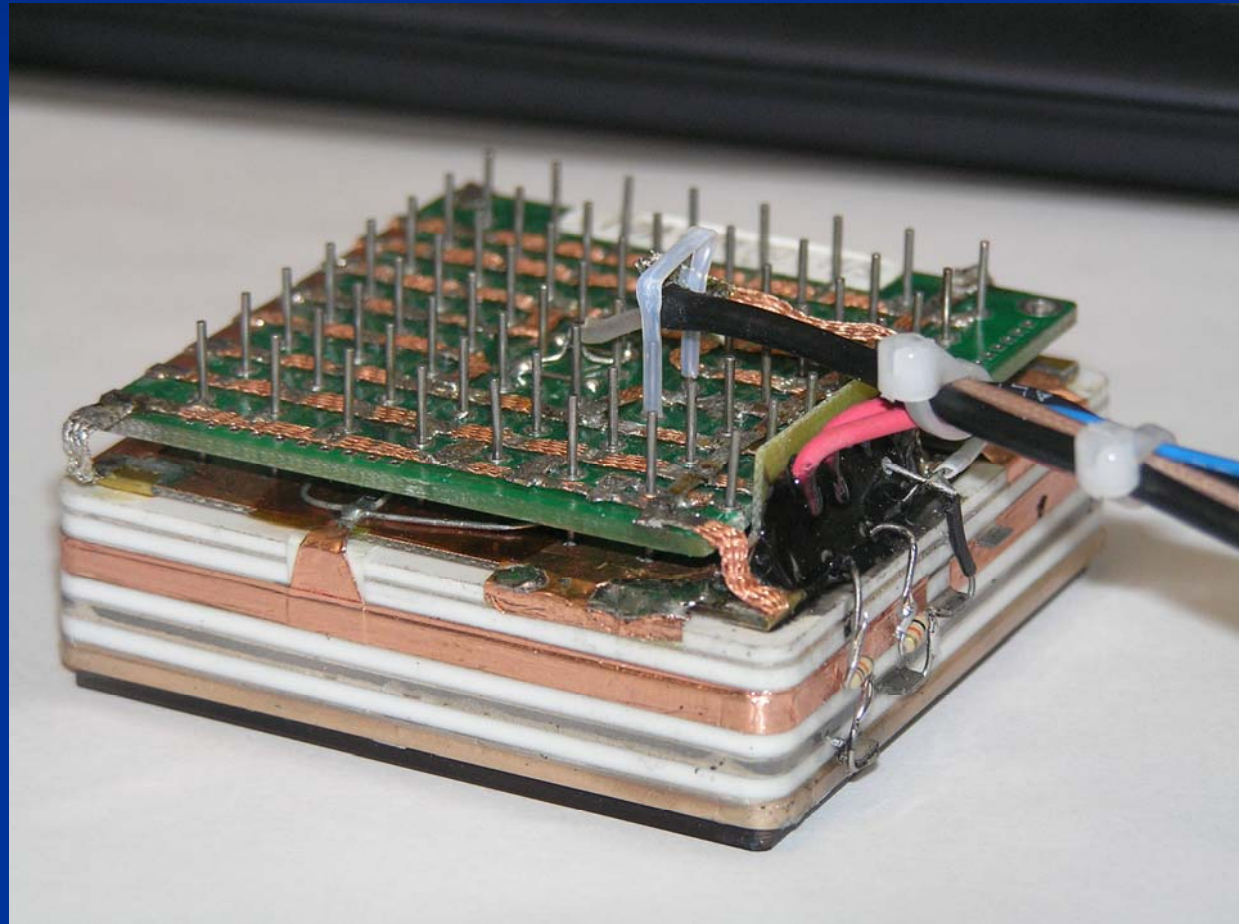
Simulating the Electrical properties of the MCP-OUT-anode world
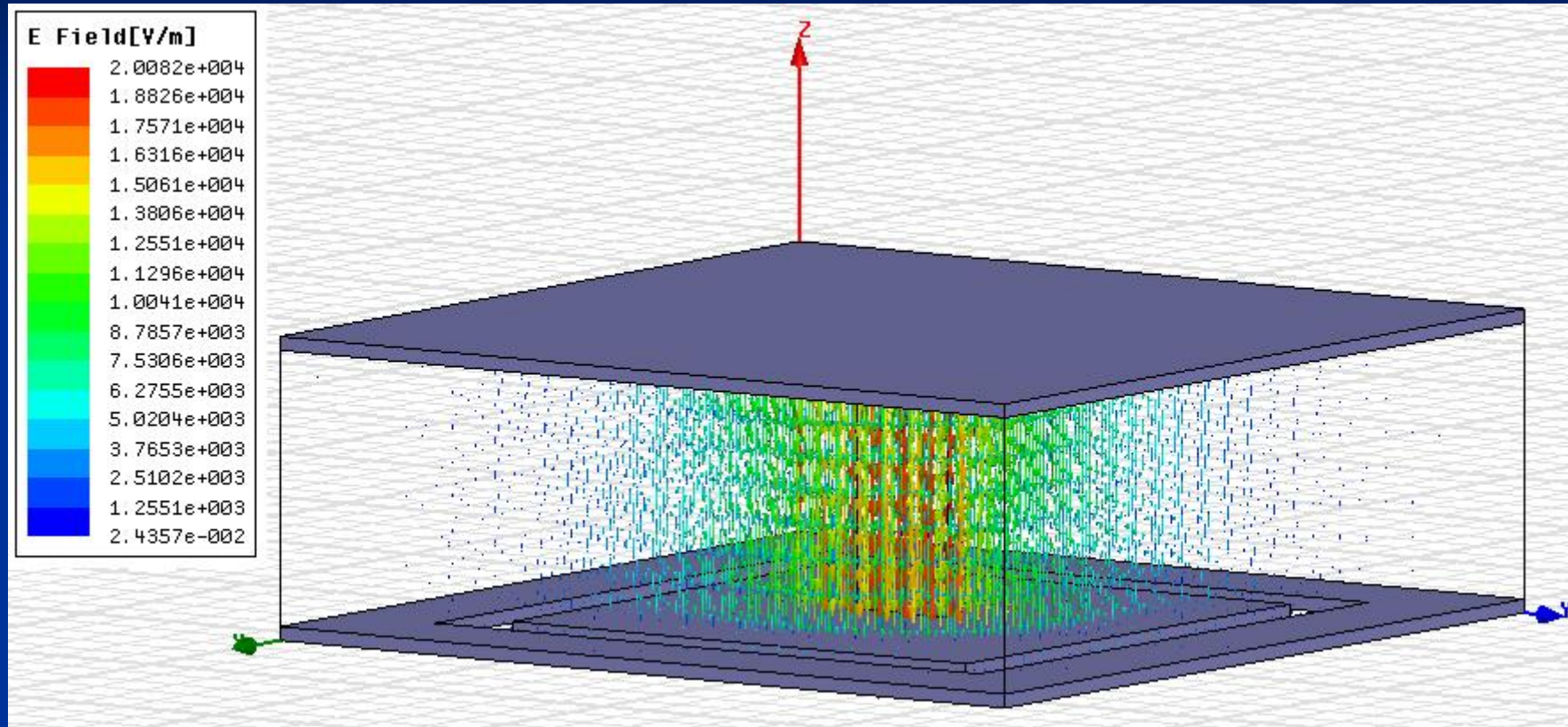
Courtesy of Tim and Ansoft: using the HFSS package- just to show we've started on this.. (this is ending on a happy note- no conclusions- The End!

Next Steps

1. Start testing the MK-0 device we have (ANL)

2. Understand the electrical circuit in the MCP and specify the next model (MK-I) we want
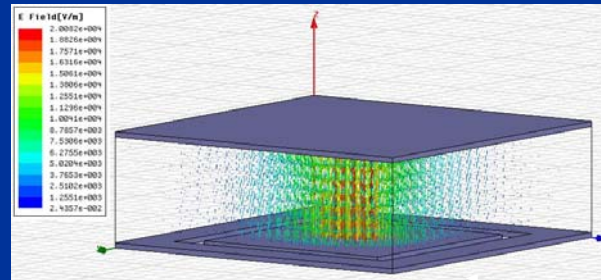
3. Finish the design and place the order to IHP for the 1ˢᵗ chip.

THE END