



The VMM1 MicroMEGAS readout ASIC

Preparation for the neutron irradiation tests

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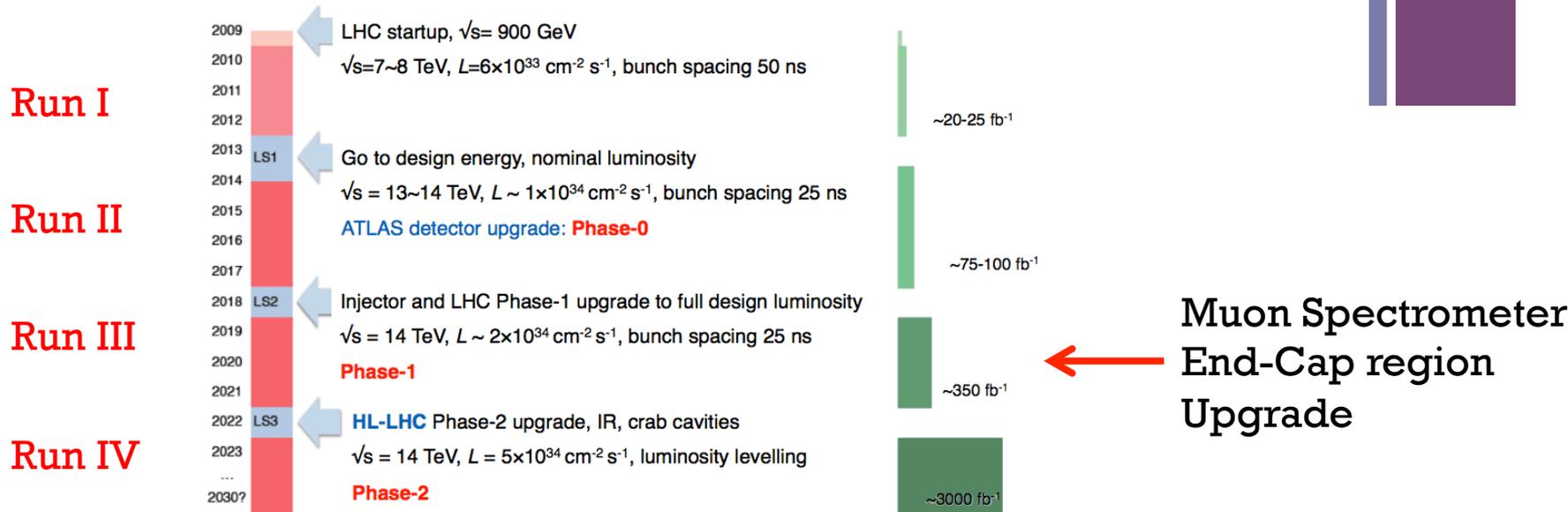


HEP 2014

Special thanks to: G.Fanourakis



ATLAS upgrade for the sLHC



Harsher radiation environment, higher detector occupancies!

Forward calorimeters, forward muon wheels affected the most

- Higher particle fluxes especially at large $|\eta|$ region at MS
- Radiation damage

Test stand at NCSR Demokritos for MicroMEGAS readout irradiation testing

+ VMM1 read-out chip

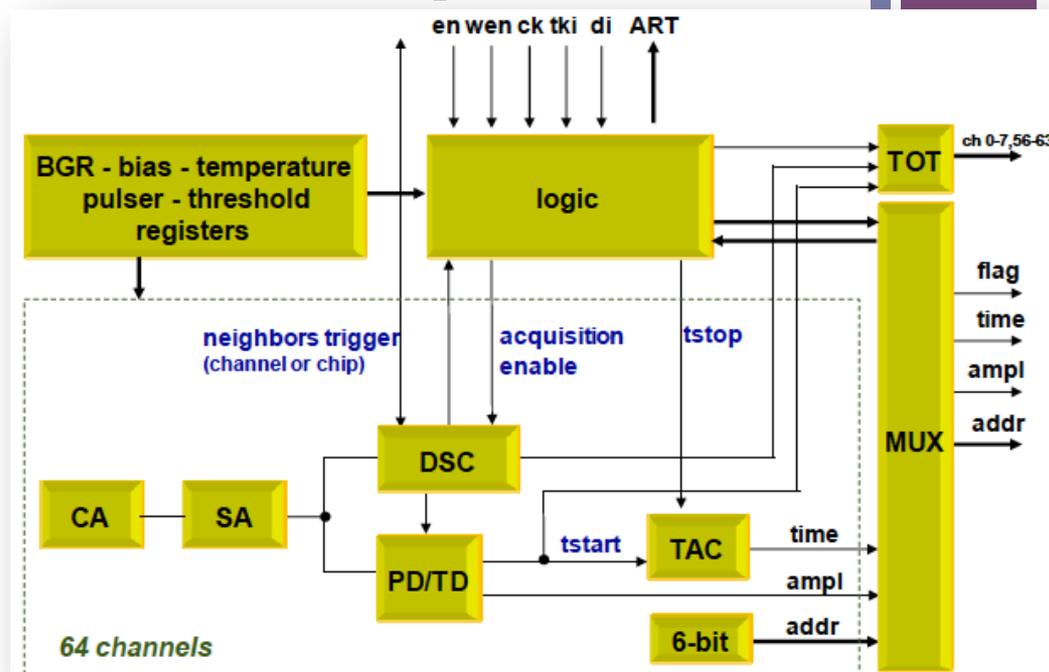
■ Architecture

- 64 channels
- Multiplexed analog time and amplitude outputs, trigger
- Internal features
 - Selectable gain
 - Integration time
 - Digital peak
 - Digital Threshold etc.

■ Modes of operation

- Configuration: **Global and channel registers accessible for configuration**
- Acquisition: Events are detected and processed (amplitude, time)
 - Charge amplification, discrimination, peak and time detection, fast trigger
 - Address in real time for first event, direct timing (ToT/TTP) per ch(16/64)
- Read-out: Sparse mode with smart token passing (ampl., time, address)

Developed in BNL





Irradiation test project

Goal

Irradiate the VMM1 chip with neutrons @NCSR Demokritos Particle Accelerator

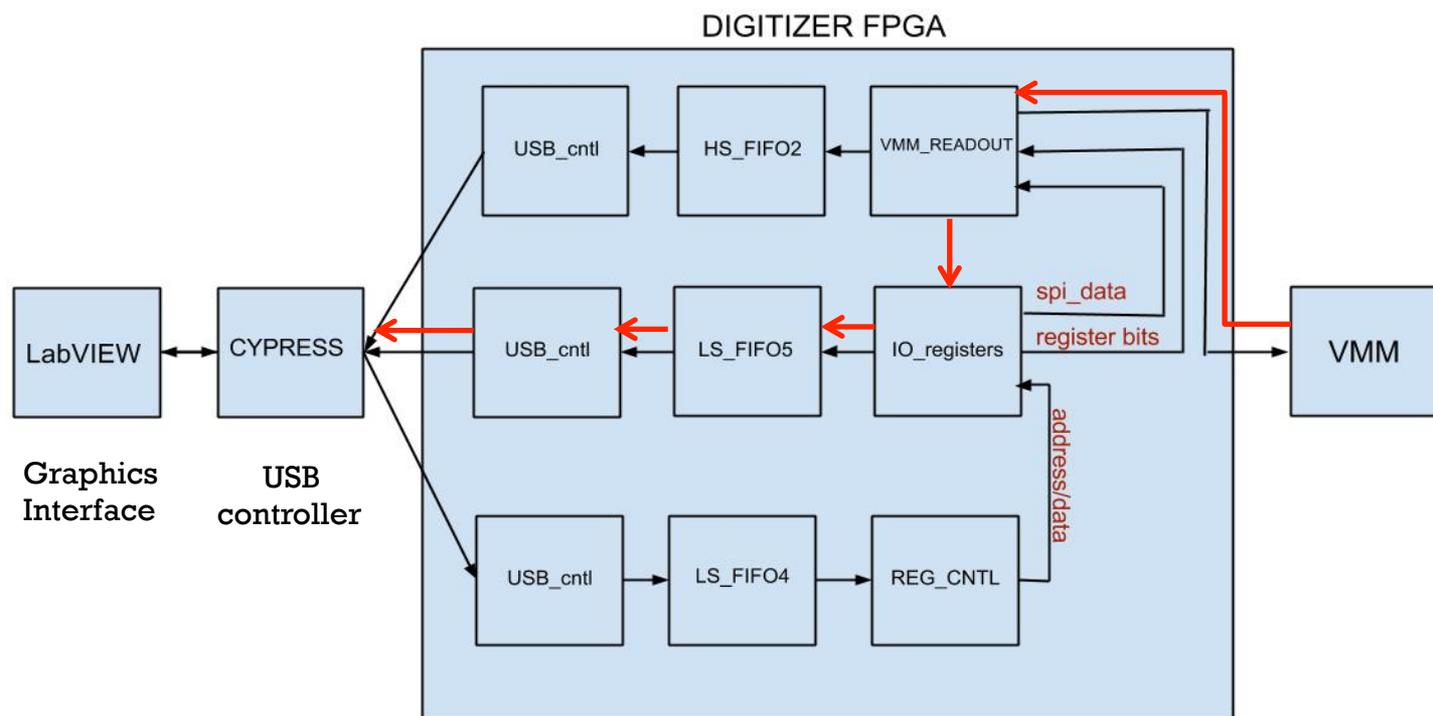
Preparation:

- Write the 1072 configuration registers (LABView -> Digitizer ->VMM1)
- Read these registers (VMM1->Digitizer->LABView) **LVDS signals**
- Test the programs and cables
- Experimental Setup



Irradiation test project

Software overview



Modifications to read the 1072 configuration registers

+ Graphics Control - LABVIEW

File Edit Operate Tools Window Help

VMM READOUT SPI WRITE THRESHOLD TEST SPI READ USB Control

CHIP B -
CHIP A -

PATH TO WRITE REGISTERS
C:\Users\friedr\Desktop\test2.txt

Save Registers in Text?
OK

WRITE
RESET
TST CLK

Use SEU testing values on the config. registers?

STOP TESTING

QUICK SET
S P C L T M SD S M X
negative 0mV
SET

Read
6

SEU 1_0 SEU 0_1
0 0

IO_VMM READ

1 negative 0mV
2 negative 0mV
3 negative 0mV
4 negative 0mV
5 negative 0mV
6 negative 0mV
7 negative 0mV
8 negative 0mV
9 negative 0mV
10 negative 0mV
11 negative 0mV
12 negative 0mV
13 negative 0mV
14 negative 0mV
15 negative 0mV
16 negative 0mV
17 negative 0mV
18 negative 0mV
19 negative 0mV
20 negative 0mV
21 negative 0mV
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51 negative 0mV
52 negative 0mV
53 negative 0mV
54 negative 0mV
55 negative 0mV
56 negative 0mV
57 negative 0mV
58 negative 0mV
59 negative 0mV
60 negative 0mV

SG
GAIN 9 mV/fC
PEAKING TIME 100 nS
Neighbor trig
TAC slope 1 uS
SDP
disable-at-peak
SM monitor CHN 15 SCMx
SFA ART enable mode timing at threshold SFAM
analog output buffers SBFM SBFP SBFT
SSTP TAC stop setting ena-low
ssh sub-hysteresis discrimination STTT STOT mode threshold-to-peak
S16 makes ch7 neighbor to ch56
SRST acquisition self resets about 40 ns after
SDT threshold DAC 350
SDP_ test pulse DAC 650

Write in 32-bits
0 FFFFFFFF
ReadoutBitByBit WithLabview
0 FFFFFFFF
Comparison
0 FFFFFFFF

Read every 10 minutes

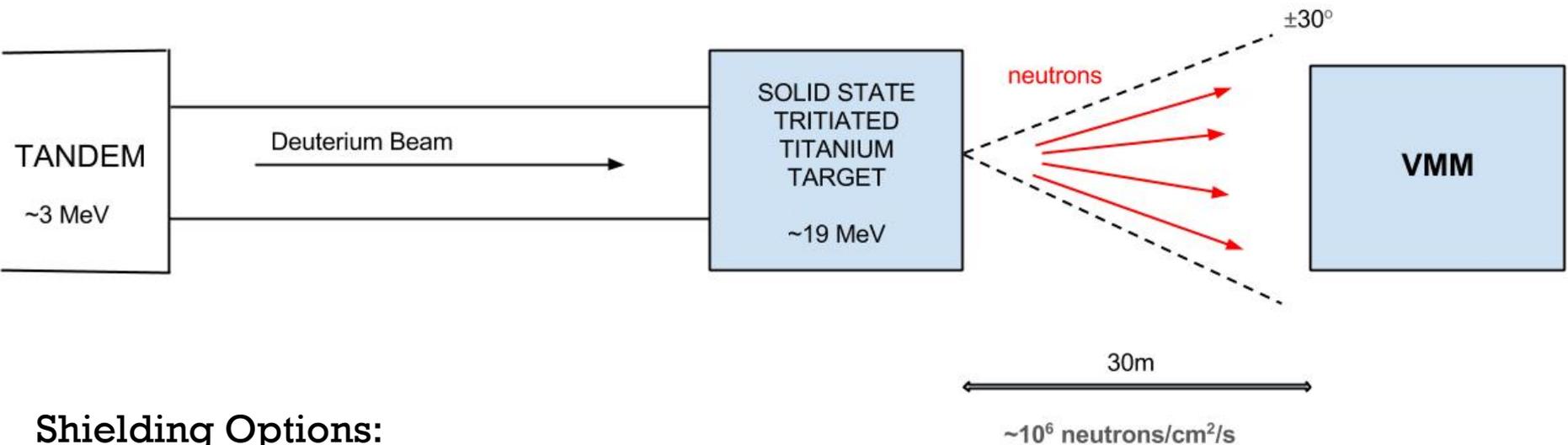
+ Experimental setup

Tritium target (10 ci):

$\sim 10^6$ neutrons/cm²/s of 18-20 MeV energy

Testing:

~ 2 weeks $\rightarrow 5 \times 10^{11}$ neutrons/cm²



Shielding Options:

1. Move digitizer away from the accelerator area
2. Keep digitizer close to the accelerator and shield it

Connectors, long cables available (to be tested)

+ Conclusions

WORK UP TO NOW:

- **Modifications for the VMM irradiation tests at the NCSR Demokritos laboratory**
 - **The read-out firmware (digitizer)**
 - Read the 1072 configuration registers (bit by bit reading)
 - Send information to LABView (in 32-bit registers)
 - **LABView graphics interface**
 - Read configuration reg., display/save information (SEU upset info)
 - Automate control to read/write pre-defined 1072-bit words every 10 mins

NEXT STEPS:

- Cable testing
- Shield determination and testing
- Irradiation tests (1st week: 26/5)



Thank you!