Calorimeter Upgrade Meeting

Wednesday 11th December 2013

Electronics session

1 Analog electronics update

ICECAL

- Pin-out of the ICECAL chip is ready
- some modifications of the design implemented (for lower consumption for example)
- next iteration sent for production in February 2014

Delay line

- standard SPI is now implemented
- Faraday chamber for shielding
- dt step ~ 996ps – to be solved in the next iteration by adding 90um in the clock path
- A discussion on SPI could be useful to check the homogeneity of the protocol on the board

DC-DC and power consumption

- Next proto :
  - 1 DC-DC for the ASIC
  - 1 DC-DC for the ADC
  - Hence, 2 DC-DC at least per board
  - 2 FEB prototypes → 4 DC-DC as a whole
- The V_ref may be produced internal and not require any DC-DC converter

2 Firmware of the FEB board

- Modification wrt previous implementation are removal of the Latency+derandomizer part. The I2C will be replaced by a SPI protocol.
- We had 2 pedestal subtractions in the previous implementation. We should probably keep this implementation but the ASIC would require subtraction of the minimum of the 2 previous samples for each integrator. Moreover, the 0 energy value, which corresponds to 256 in ADC value in the present design should correspond to a different ADC value in the future so that less bits flip when the data fluctuate around 0.
- We would like to use a USB port on the FEB. A specific small board could be connected to the FEB to provide it. Usage of this system in a test beam (with an extension cable) should be thought of.
- The LLT will be a copy of what is in the present L0 FPGA of the FEB. There will be some more functionalities (new parameters used by the LLT).
- Power consumption : the +5V and -5V are not used any more by the FEB. We could re-use those input. This may have some implications on the LEDTSB (plan a discussion during

February meeting)

- It is important to keep a pulsing system on the front-end board, independent for each channel. It should be able to reach a value >> 2048 (bit 12).
- space on the FEB (and the front-face) is an issue that should be solved will a large priority.

3 Design of the Control Board

- 2 GBT-X on the board → this is not completely clarified. Federico mentioned that a GBT-X could drive up to 17 GBT-SCA. To be checked.
- SLVS-LVDS translators usage before driving the signals to the backplane is the default.
- clock distributed on the 3U backplane after SLVS → LVDS conversion
- Should we have -5V to produce the NIM signals. Do we need NIM output/input on the board. Can we use another standard ?

ECAL Modules

- Response of the modules is ~ the same whatever the channels → 32 spares are fine
- 2 modules have a broken fibre. This leads to a 6 % light loss → not a big problem
- Other inner part modules left
  - 2 irradiated modules in the tunnel (one removed definitely and the other back in in 2015)
  - 2 irradiated modules in Protvino (low irradiation but some administrative trouble if we want to bring them back)

Performances

1 Cluster reconstruction

- The algorithm does not deal with energy deposit on the frontiers of the areas (by the way, at present and by default we have no clustering on the borders...)
- What is the spill over configuration for the Monte-Carlo sample used for the analysis ? It seems that the sample used is now already old.
- 2x2 seems as good as 3x3 in term of resolution (cross is a bit worst). 2X2 and cross better than 3x3 for pile-up.
- We need to
  - test on electrons
  - determining the proper corrections (for electrons/photons)
  - how do we measure the position ?

2 Bs → phi gamma channel study

- The constrain on the proper time is ~5fs for the upgrade precision expected
- There is a good consistency between the proper time shift and the energy calibration from K* gamma

- the proper time used to be biased by several parameters. After the proper calibration, the photon estimator still bias the proper time. This is even more crucial for the upgrade where the precision expected is far better.
- The proper time resolution is slightly better with the upgrade samples than with MC2012. The origin of the improvement is not really understood : the photon ? The phi (tracking) ?
- Photon identification should not be used on upgrade sample as it relies on SPD/PS information which are missing in those samples.

AOB

- Meeting at Orsay in February : power scheme of the crate
- Discuss the availability of the GBT-SCA. Can we replace it with another chip (FPGA)
- The number of GBT-SCA that can be connected to a single GBT-X is not well-defined. Is it 16 or 17 ?