UNIVERSITAT DE BARCELONA

Institut de Ciències del Cosmos

Analog Electronics

Update on ICECAL3 and delay unit

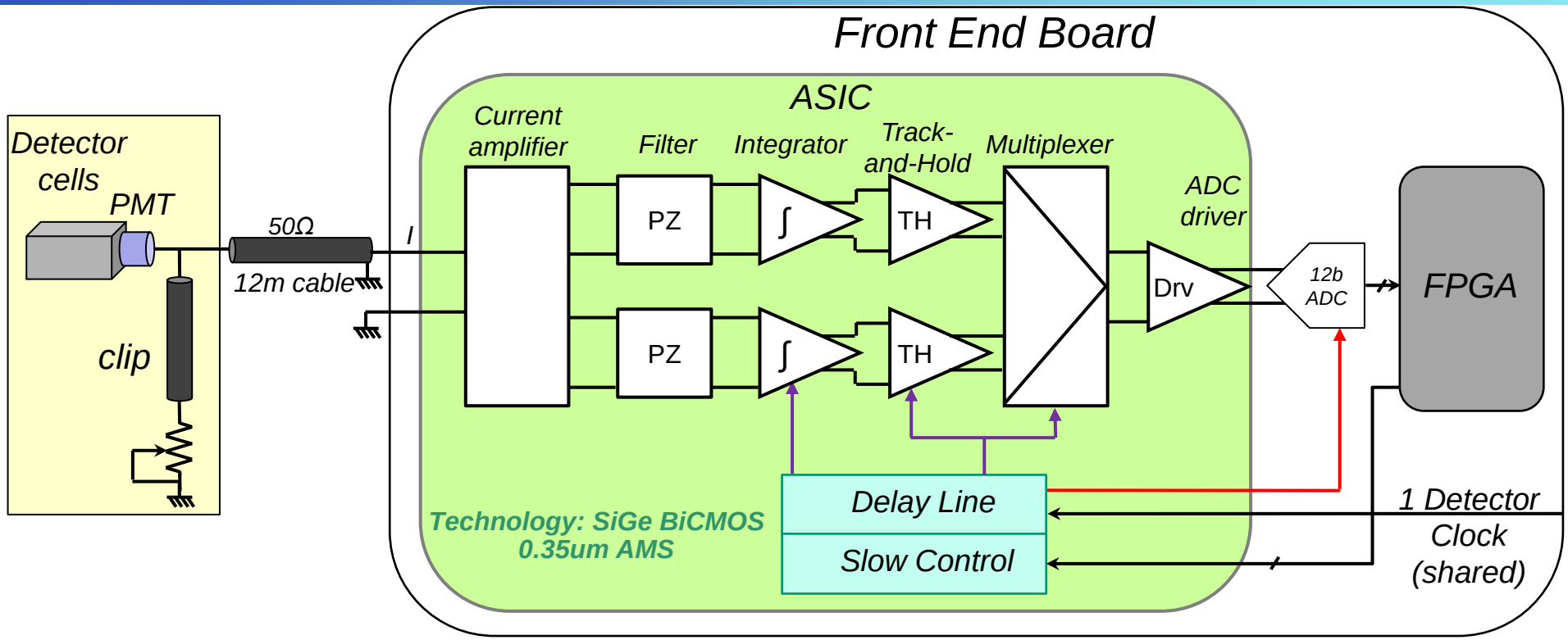
J. Mauricio, E. Picatoste

Universitat de Barcelona

Institut de Ciències del Cosmos ICC-UB

Calorimeter Upgrade Meeting – October 16th 2013

ICECAL3

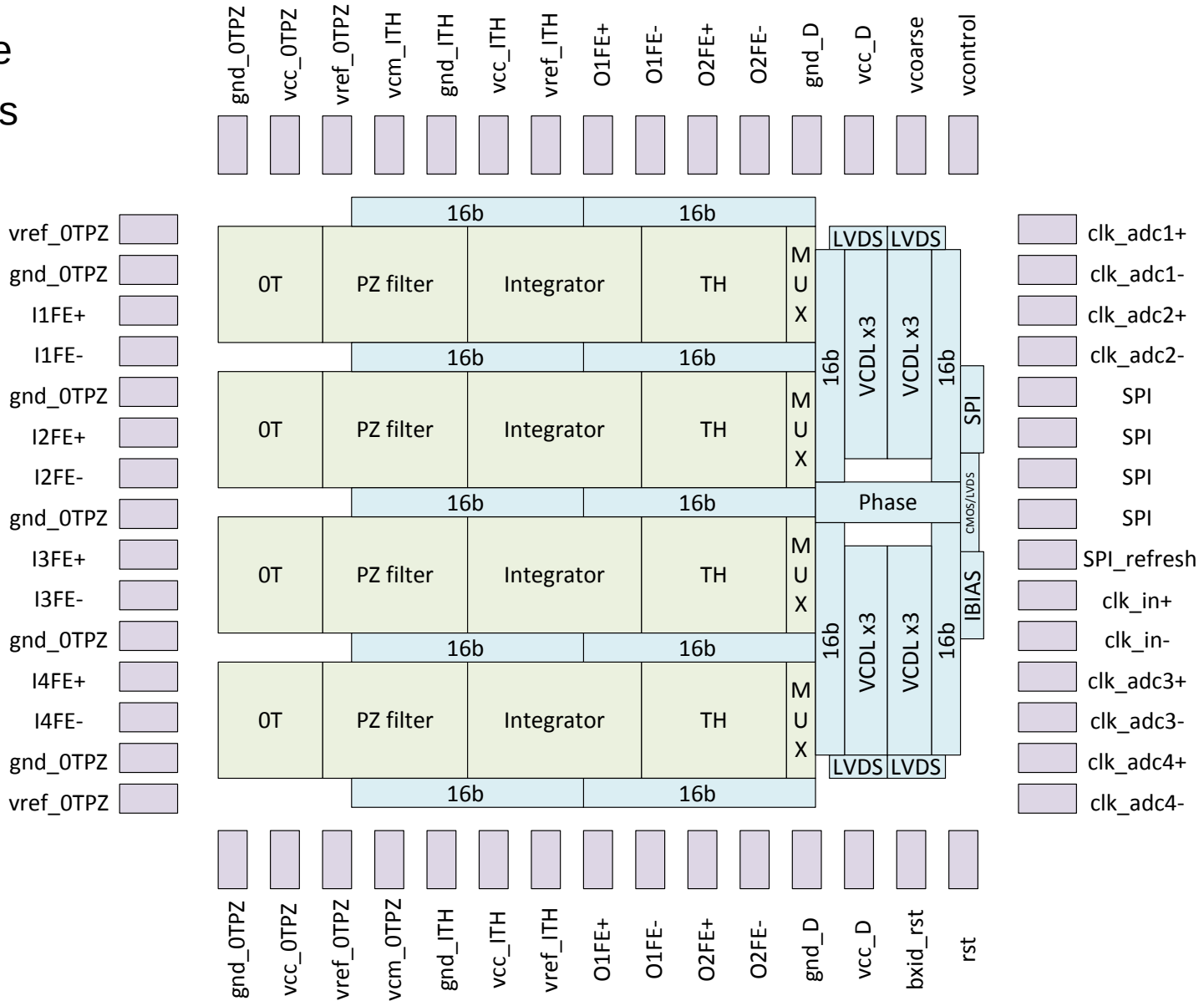


- Full chip for the analog electronics of the Calo Upgrade
  - 4 channel with tuneable parameters
  - Delay lines
  - Digital block
    - Configuration registers
    - SPI

ICECAL3: pinout

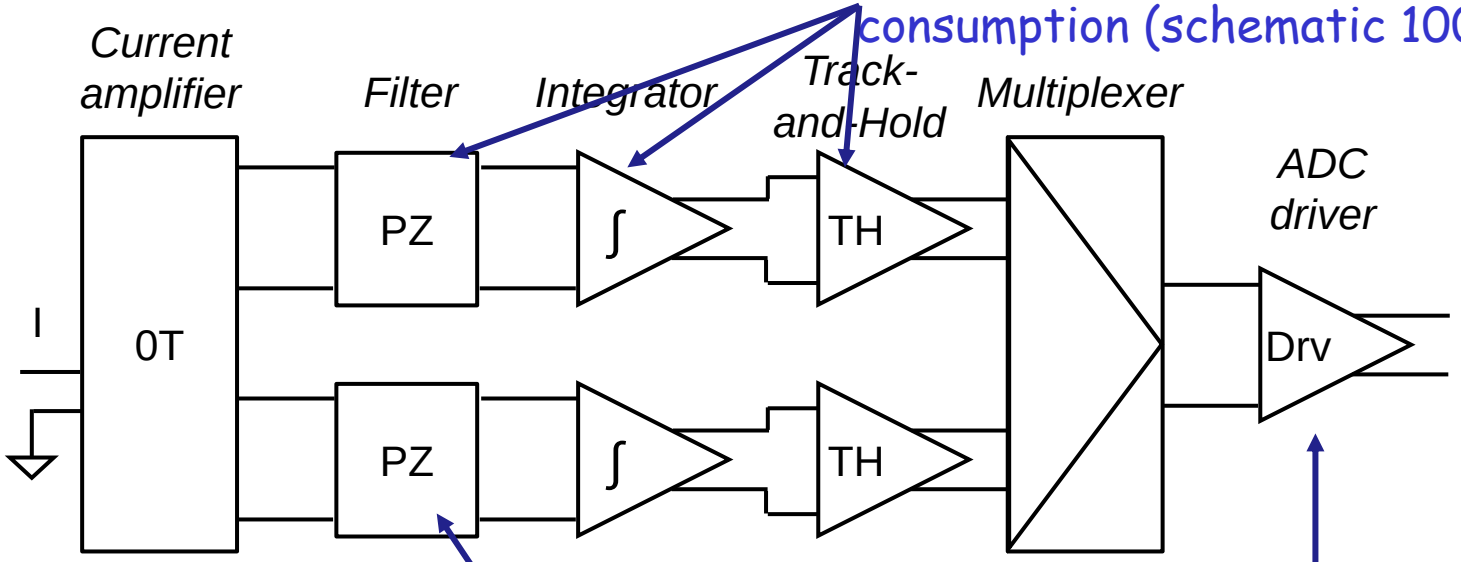
15 p/side

⇒ 60 pins

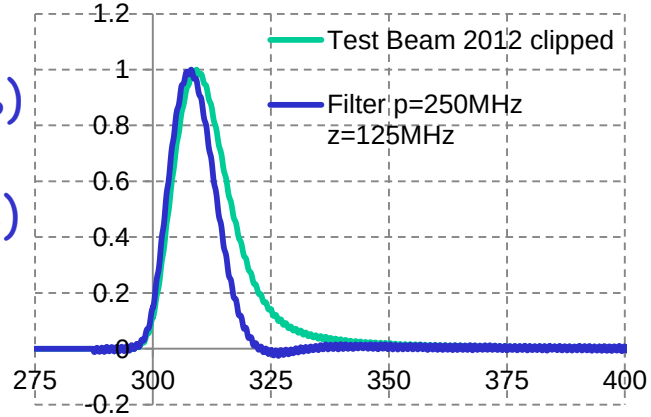


Channel changes for ICECAL3 status

Modified OpAmp for reduced power consumption (schematic 100%)



PZ filter to compensate for cable and clipping effects



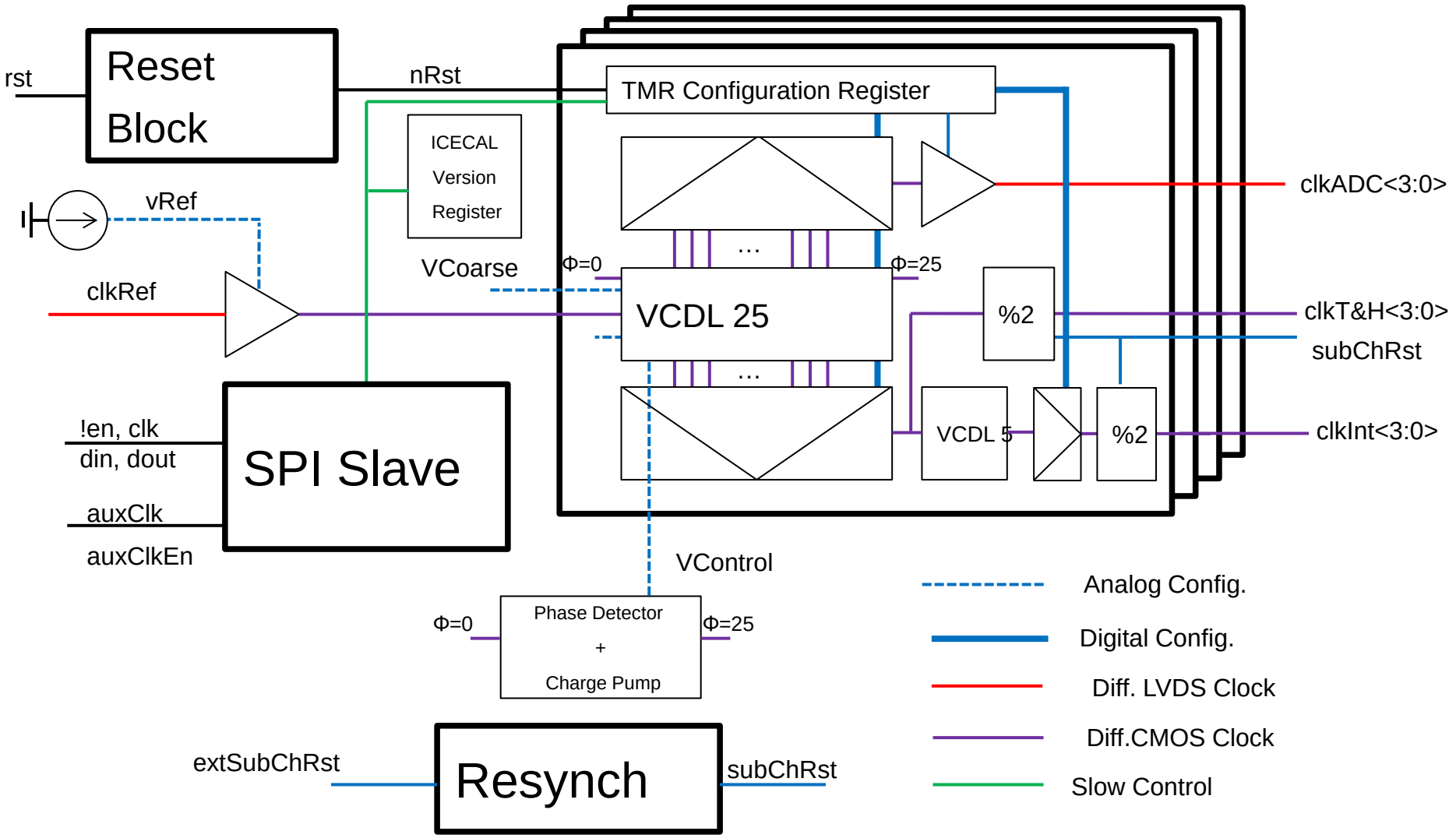
Adjustable parameters:

- Zin (to be done)
- Offset (schematic 90%)
- PZ (schematic 100%)
- RC int (schematic 100%)

Other blocks:

- Multiplexer (schematic 100%)
- ADC driver (to be done)

ICECALv3 Delay Chip Block Overview



Delay Block Status

- Schematic: 100% done
- Layout: 100% done.
- Also the Faraday chamber.
  - 25um of M1-M2-M3-M4 shielding.

- Functional models:
  - VCDL 3 channels.
  - SPI Slave.
  - TMR Registers.
  - ICECAL Version Register.
  - CMOS 2 LVDS.

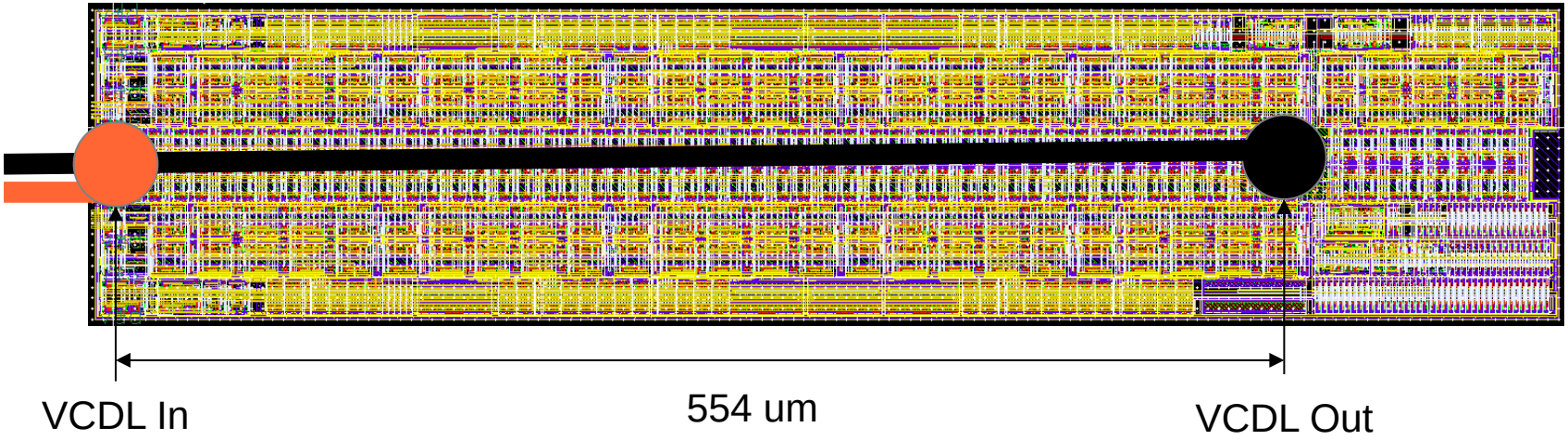
Delay Block Simulations

- Slow Control:
- Functional models:
  - SPI works nice at even more than 20 Mbps.
  - SPI is now "standard".

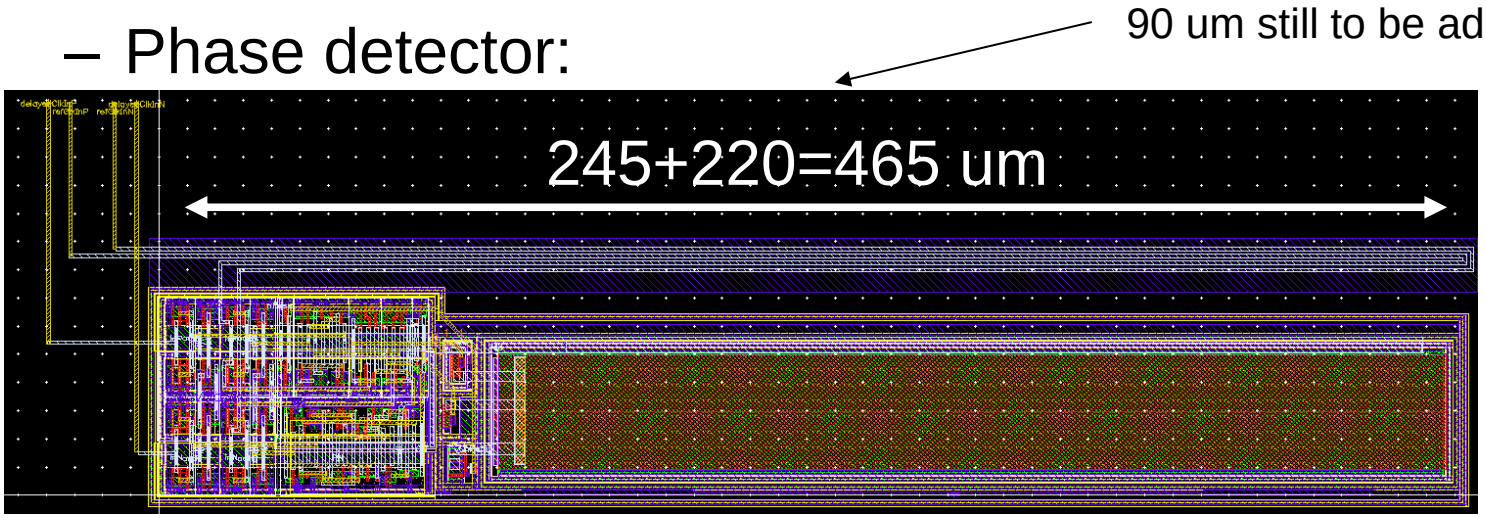
- Delay Line:
  - Works as expected.
  - VCDL to Phase detector signal track compensation:
    - Current delay per stage (when DLL is locked): 996 ps.
    - To be compensated…

VCDL to Phase detector signal track compensation

– VCDL:

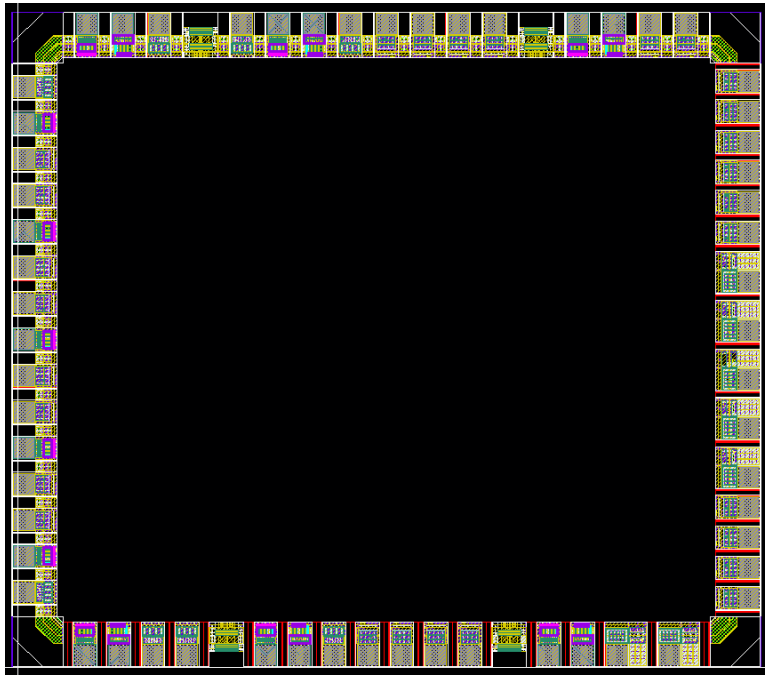


– Phase detector:



Chip Integration

- Digital block is done.
- Pad ring is done.
- Analog channels under construction…
- Extracted simulations expected to start before Christmas.
- Chip to be submitted on February 2014

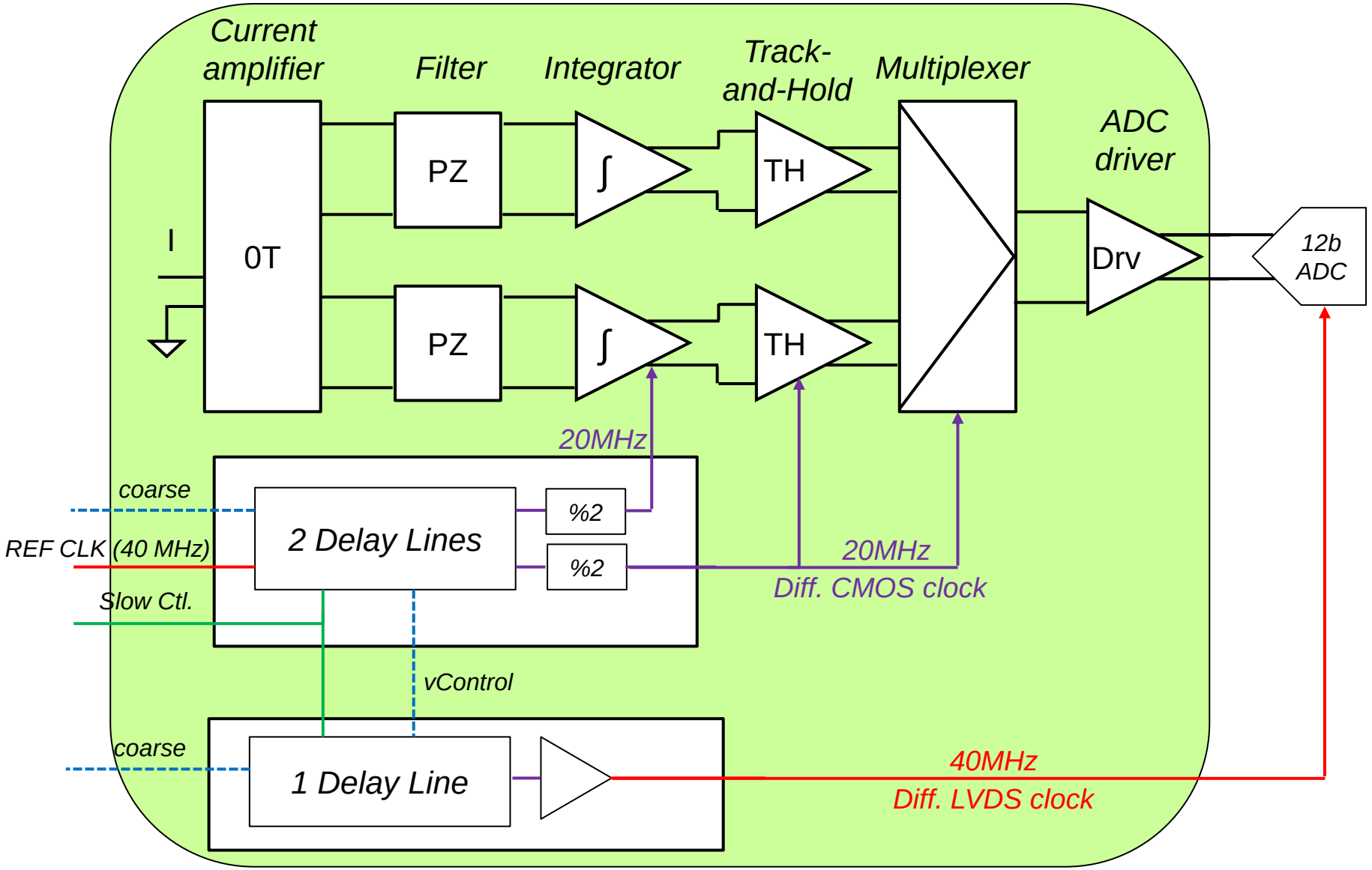


Power consumption and DC-DC requirements

- ASIC
  - Analog channel ~40mA x4 (at 3.3V)→ ~530mW
    - A V_{ref} = 1.65V is also needed, but
      - Low power (160mA) ⇒ no DCDC needed
  - Digital+DLL block ≤ 50mW
  - 1 DCDC
- ADCs
  - V = 3.3V, I_{load} = 1,9A → 1 DCDC
- At least 2 DCDC prototypes at Barcelona (3.3V)

Backup

Clock generation



Delay Chip Standalone Overview