LHCb Calorimeter Upgrade : CROC board architecture overview

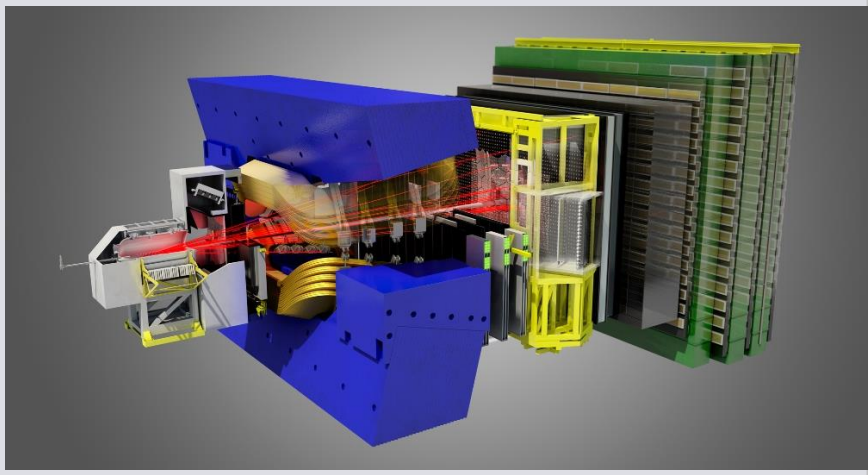
ECAL-HCAL font-end crate

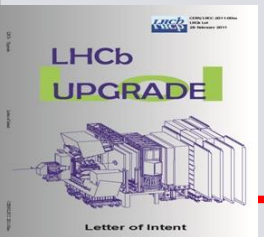
- Short reminder

Control Board architecture

- Clock distribution – Slow control distribution – DC-DC converter and Delatching control – Trigger and Data path

Conclusion

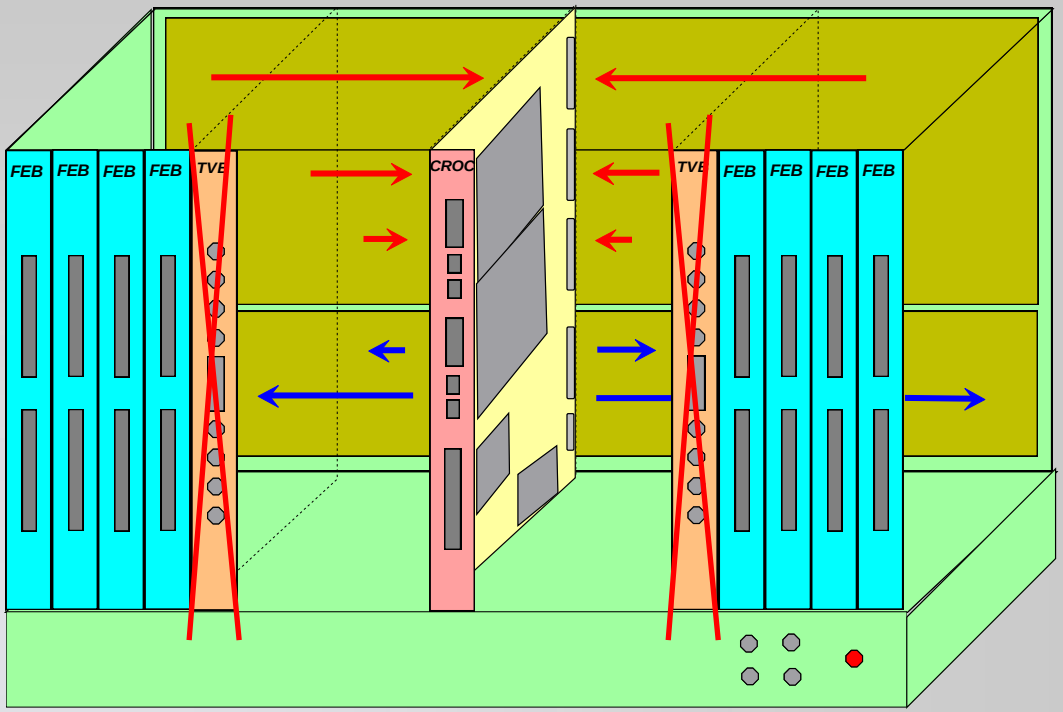




ECAL-HCAL Front-end crate

- Front-end crate
  - Same backplane
    - 3U ⇨ power supply, clock distribution, …
    - 6U ⇨ links between boards inside the same crate
  - New Front-end Board
  - New Control Board
  - Remove TVB

    Add an extra LLT fiber on the FEB

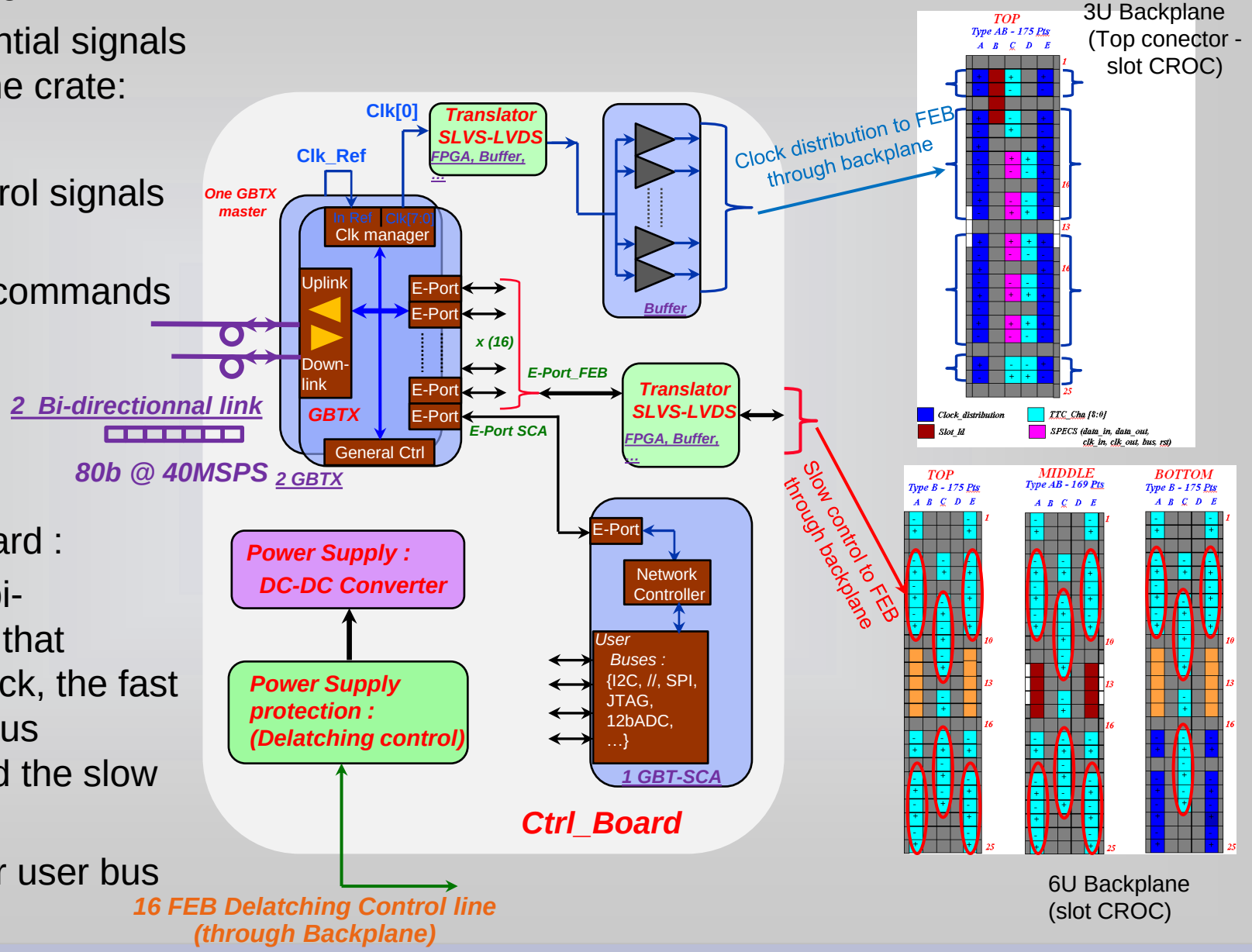


- Signal distribution inside Front-end crate
  - Clock distribution from the CROC to all front-end board inside the same crate through backplane
  - Slow control through 6U backplane
  - Fast command (BxId Reset, FE Reset, …) through 3U backplane

- Crate Power supply
  - Used Marathon equipment with adjustable output voltage *(6 modules)*
  - Need to define precisely the power supply requirement for all the board in the crate

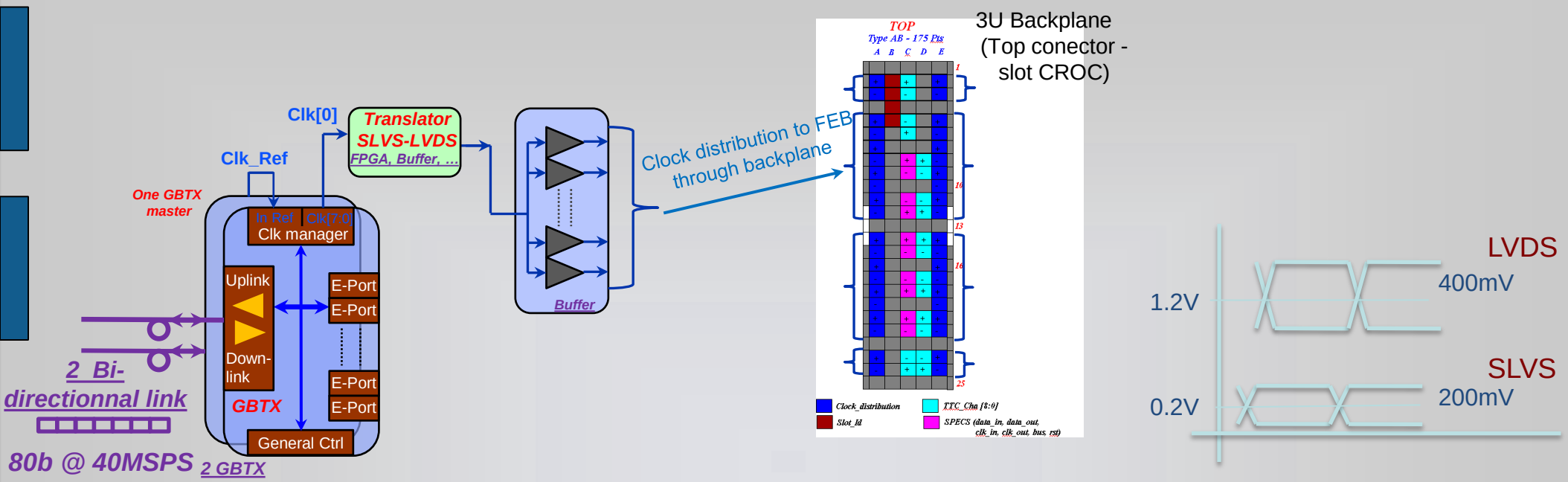
Control board global architecture

- Located in the central slot of the Front-end crate
- It distributes essential signals to the boards of the crate:
  - The clock
  - The slow control signals
  - The fast and synchronous commands



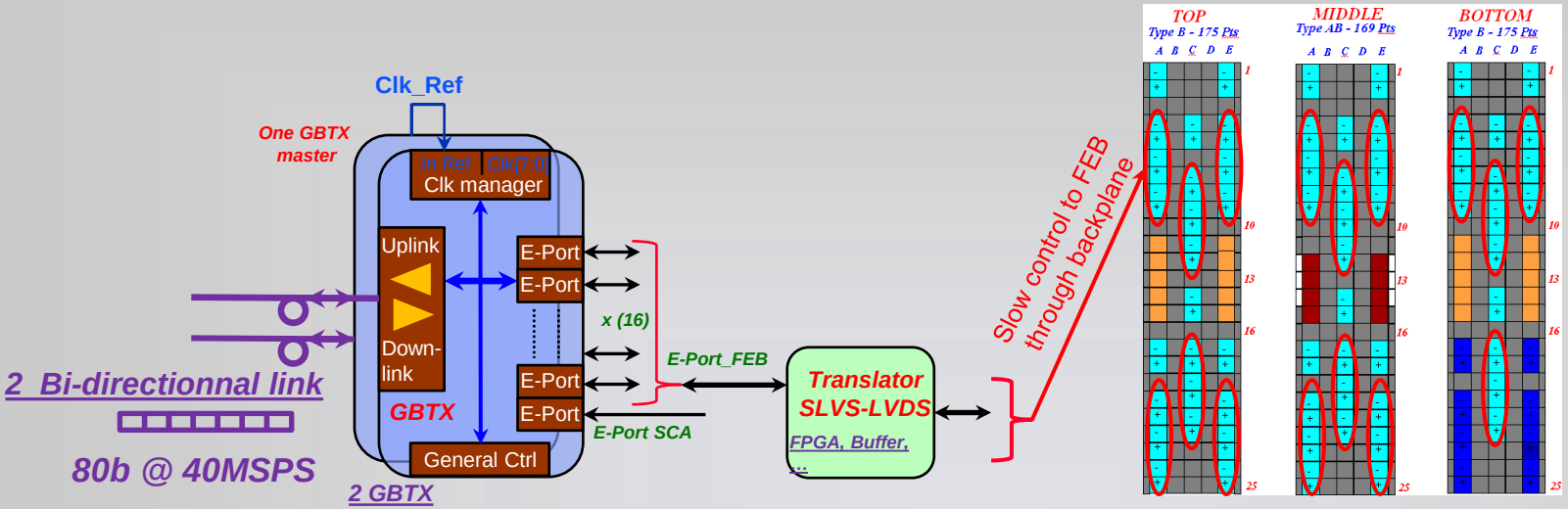
- On the Control Board :
  - 2 GBT with 2 bi-directional link that provide the clock, the fast and synchronous commands and the slow control signals
  - 1 GBT-SCA for user bus of the CB.

Control board : Clock distribution



- The GBTX “master” receive the clock from its optical link and will provide it to the second GBT through the PCB
- It will also provide the clock to the other board inside the same crate
  - Output of the GBT in SLVS
  - SLVS to LVDS translator (FPGA)
  - Buffering
  - Clock distribution to all FEB inside the same crate through 3U bacplane

Control board : Slow control distribution



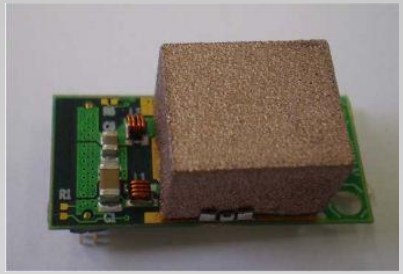
The number of active E-Links and their data rate are programmable (x40 ?)

- The GBTX receive the slow control from its bi-directional
- 17 e-links are necessary in a crate:
  - 16 e-links for the FEB inside the same crate
  - 1 e-links for the Control Board
  - Necessity of 2 GBTX on the Control Board
  - SLVS to LVDS translator (FPGA)
  - Slow control distribution to all FEB inside the same crate through 6U backplane

(We re-used the data link of 6U backplane to the current architecture)

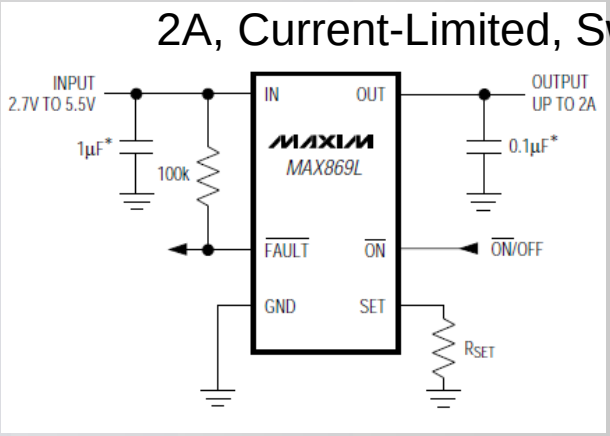
Control board : DC-DC converter and Delatching control

- DC-DC converter
  - *http://project-dcdc.web.cern.ch/project-dcdc*

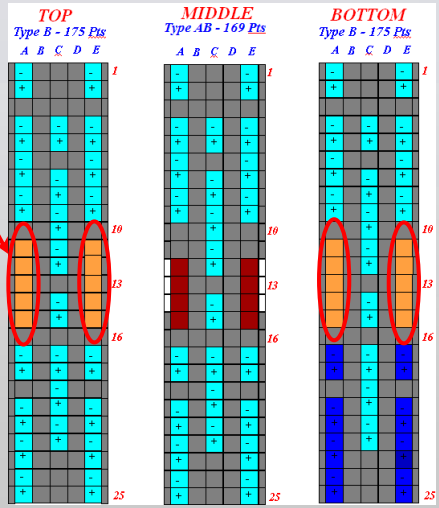


- Delatching control and protection
  - It will be concern FEB and Control Board
  - Implementation of one or several MAX869 on each board
  - If a Single Event Latchup (SEL) occur the MAX869 switch OFF the curent off the board during fews ms
  - Dedicated 16 connections on the 6U backplane between the FEB and the CB, to inform the CB that a problem occurred on one FEB
  - The CB can also switch ON/OFF individually each FEB or a part of CB.
- The same protections was implemented in the current Front-end electronics

2A, Current-Limited, Switch

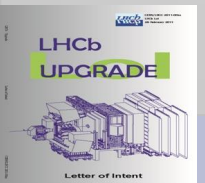


Hight speed current increase
⇨ Output is switched off during few ms

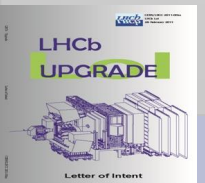


Conclusion

- Global architecture of the Control Board is well-defined for us
  - Two bi-directional links, and 2 GBTX for Slow Control distribution
  - Used DC-DC converter
- 2014 : Control Board Prototype
  - Define precisely the output level of the “marathon”
  - Disponibilies of the components prototype : GBTX, GBT_SCA, DC-DC converter, …
  - First prototype end of the year



Thank you



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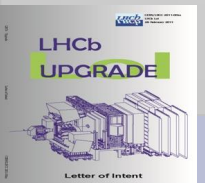
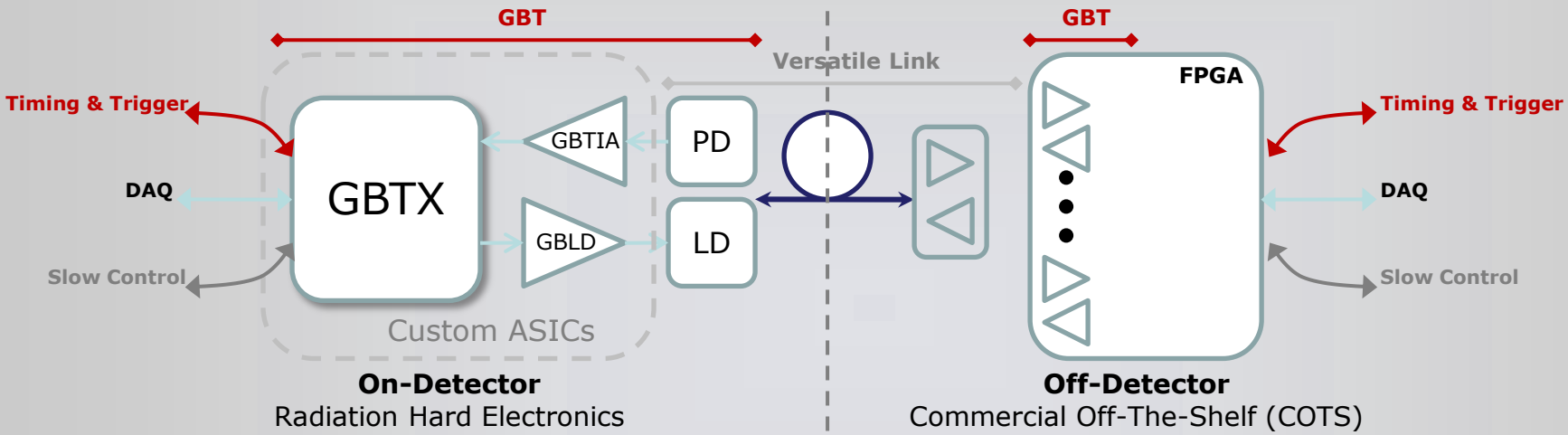
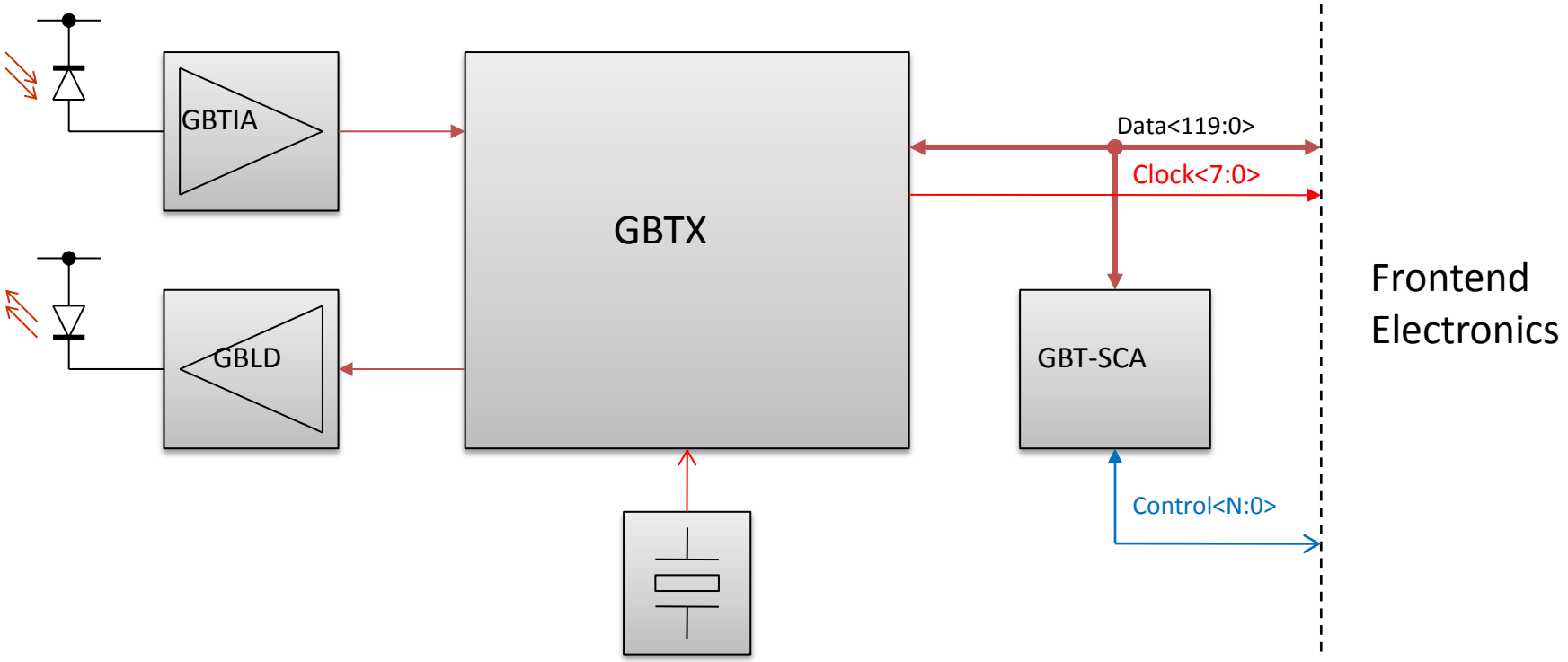


Radiation Hard Optical Link Architecture

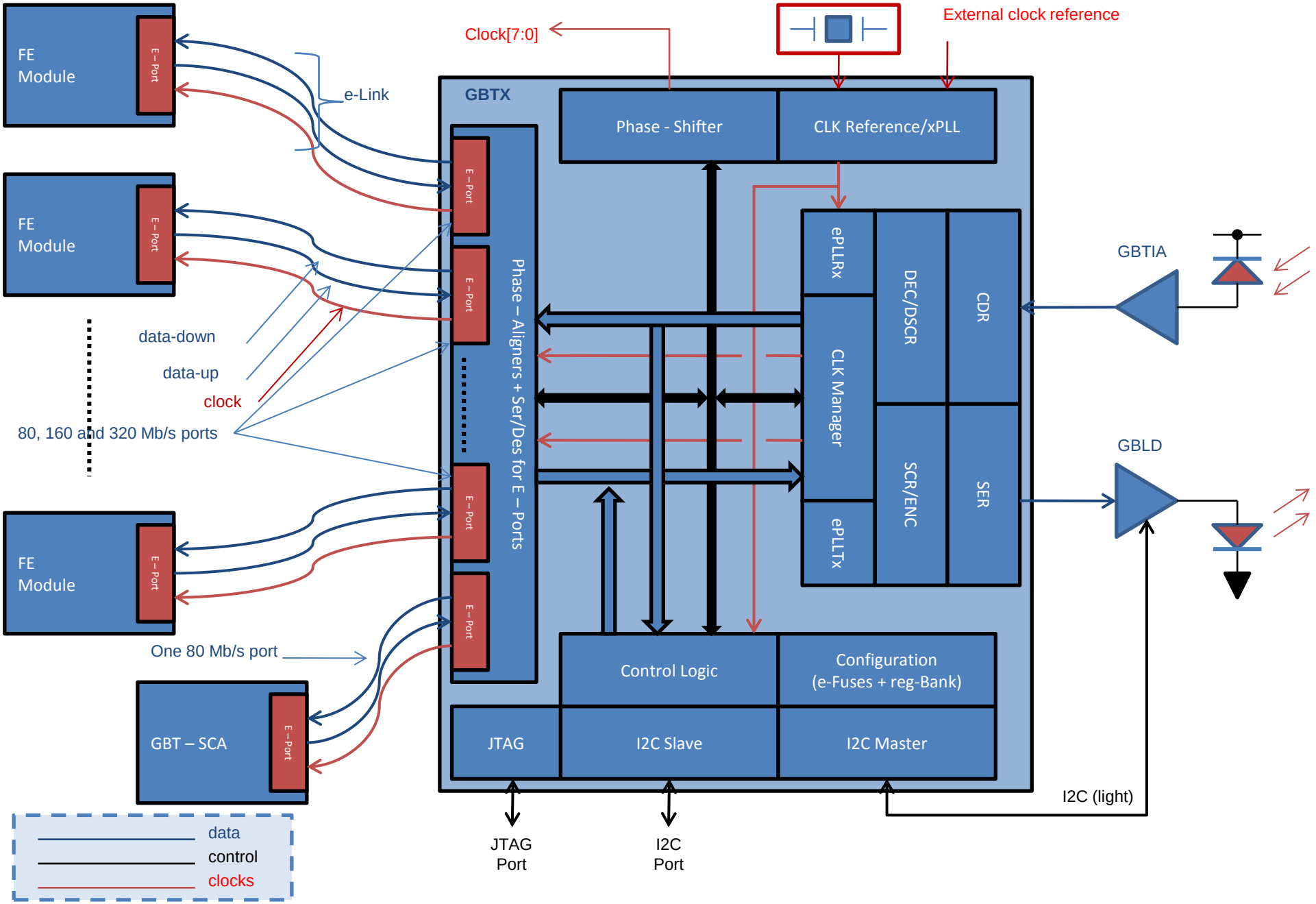


The GBT Chipset

- Radiation tolerant chipset:
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and Timing Transceiver
  - GBT-SCA: Slow control ASIC
- Supports:
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s
- The target applications are:
  - Data readout
  - TTC
  - Slow control and monitoring links.
- Radiation tolerance:
  - Total dose
  - Single Event Upsets

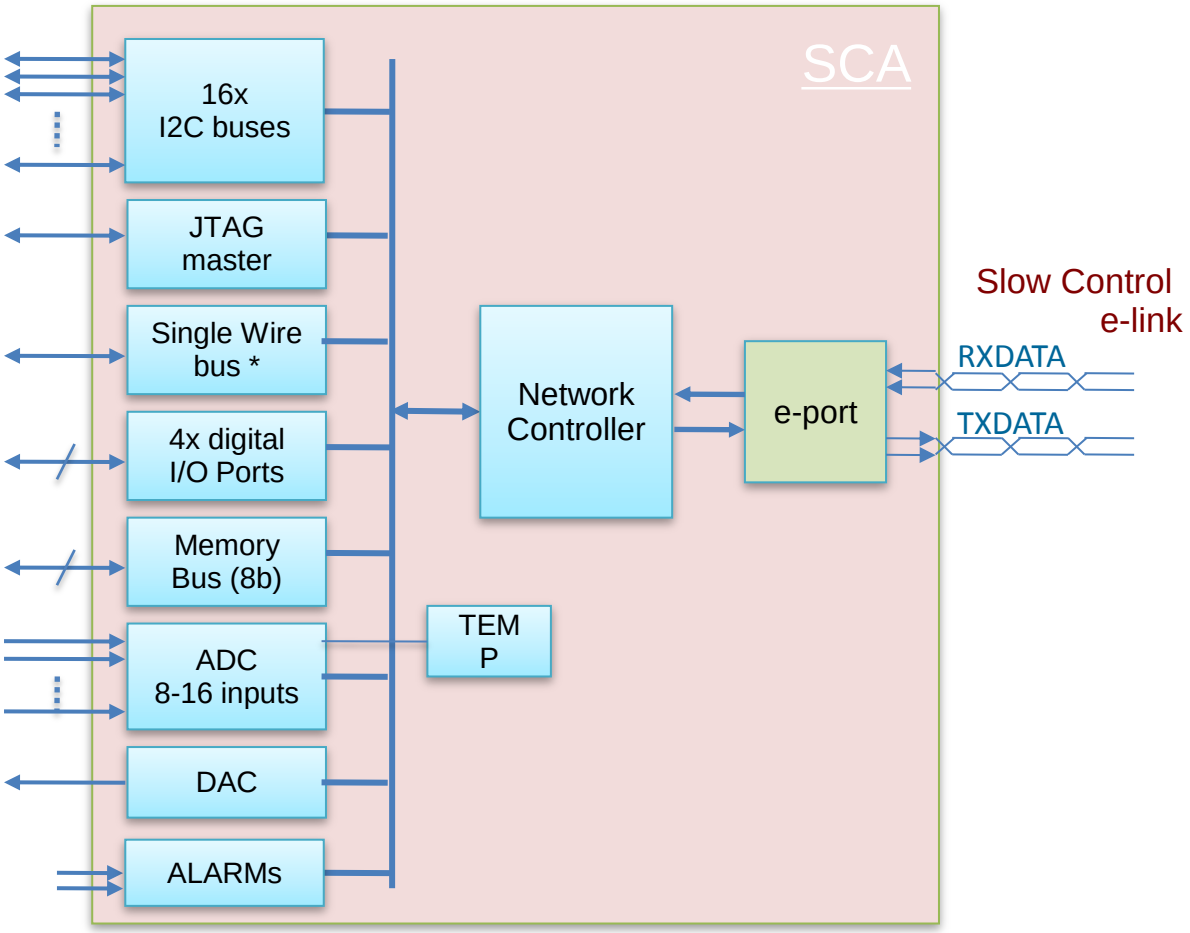


The GBT System



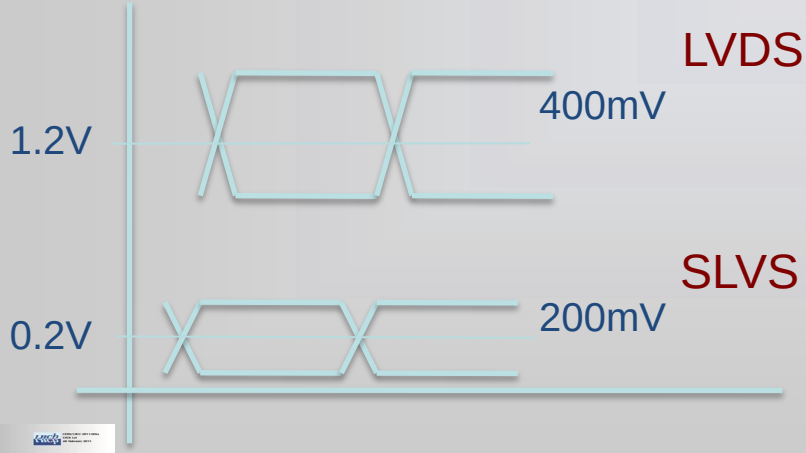
The Slow Control Adapter ASIC

- ASIC dedicated to slow control functions.
- System Upgrades for SLHC detectors.
- Replacement for the CCU & DCU ASICs
  (Communication Control Unit & Detector Control Unit in CMS).
- It will implement multiple protocol busses and functions:
  - I2C, JTAG, Single-wire, parallel-port, etc…
- It will implement environment monitoring and control functions:
  - Temperature sensing
  - Multi-channel ADC
  - Single channel DAC
- Flexible enough to match the needs of different FE systems.
- Technology: CMOS 130nm using radiation tolerant techniques.



SLVS standard

- SLVS (Scalable Low Voltage Standard)
  - JEDEC standard: JESD8-13
  - Differential voltage based signaling protocol.
    - Voltage levels compatible with deep submicron processes.
    - Typical link length runs of 30cm over PCB at 1Gbps.
    - Low Power, Low EMI
  - Application in data links for Flat Panel displays in mobile devices.
    - Mobile Pixel Link, MPL-2 (National semi.)



SLVS specifications brief
2 mA Differential max
Line impedance: 100 Ohm
Signal: +- 200 mV
Common mode ref voltage: 0.2V