General comments

The Fe board will have a firmware general architecture close the actual design

The FE board was designed with 2 different kinds of FPGA and 4 different references :

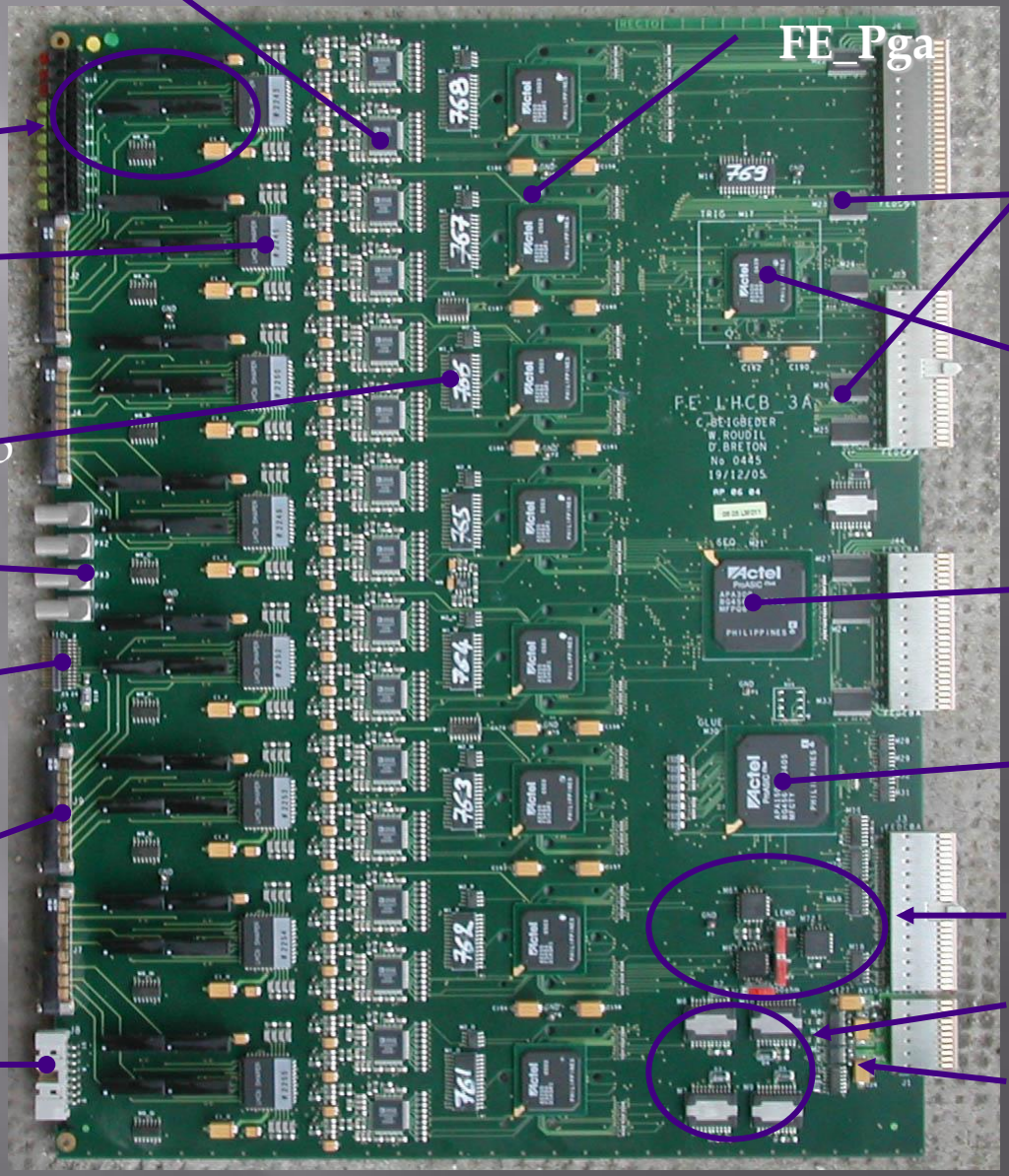
9 non-reprogrammable Actel AX500 and AX 250

2 reprogrammable : Actel APA 150 and APA300

The new version will be fully equiped with reprogammable device APA3E Actel family devices.

The whole crate will be reprogrammable without external components which is a drawback of the actual design.

Fe board



ADC

Delay lines

Analog chip

Delay chip

Lemo (Probes)

APA connector

Analog input connectors

AX connector

Serializers + Deserializers

Trig_PGA

Seq_Pga

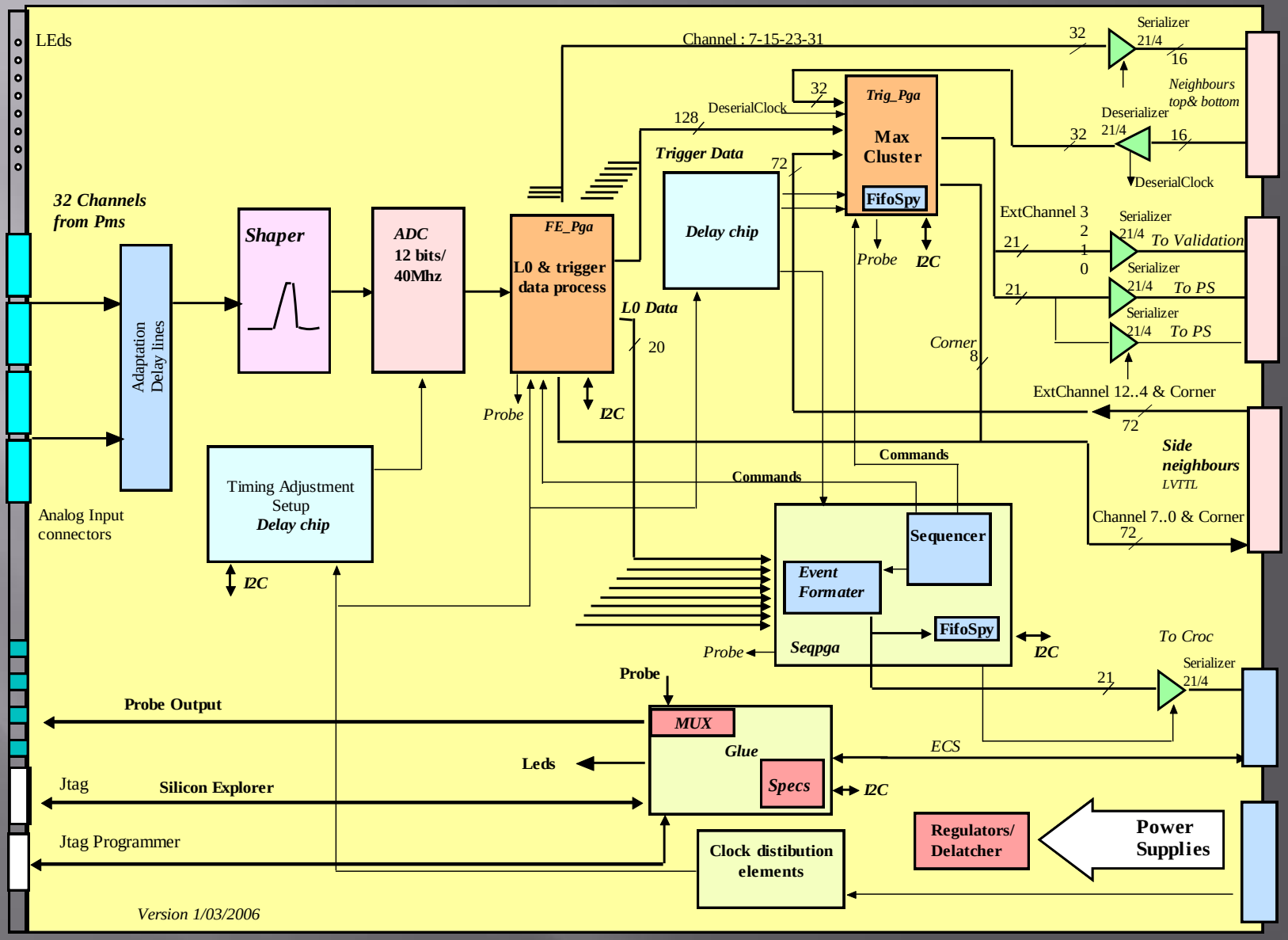
Glue_Pga

Clock Receiver/driv

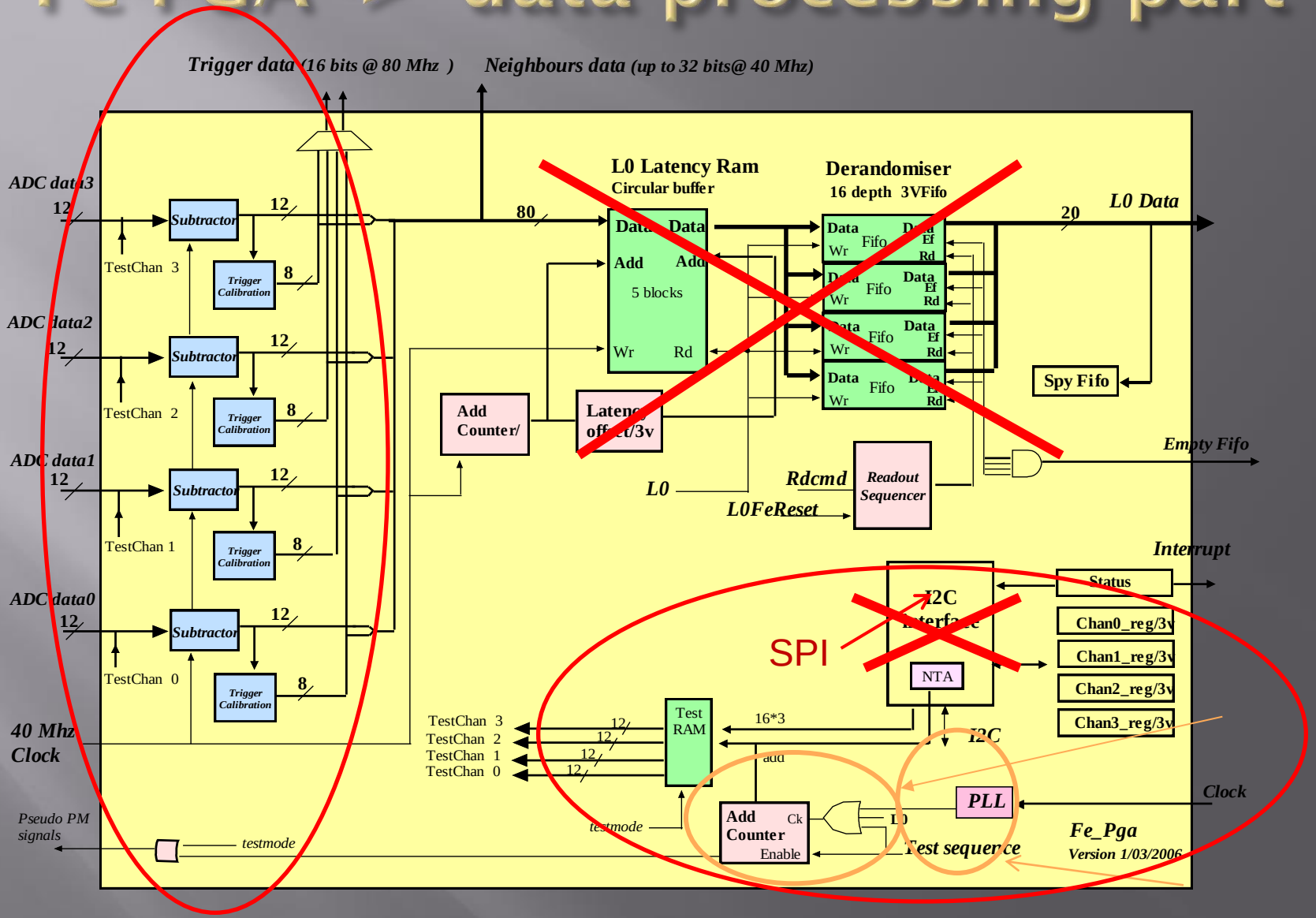
Rad-hard regulator +5Vanalog/dig,+3.3 5V

Delatchers

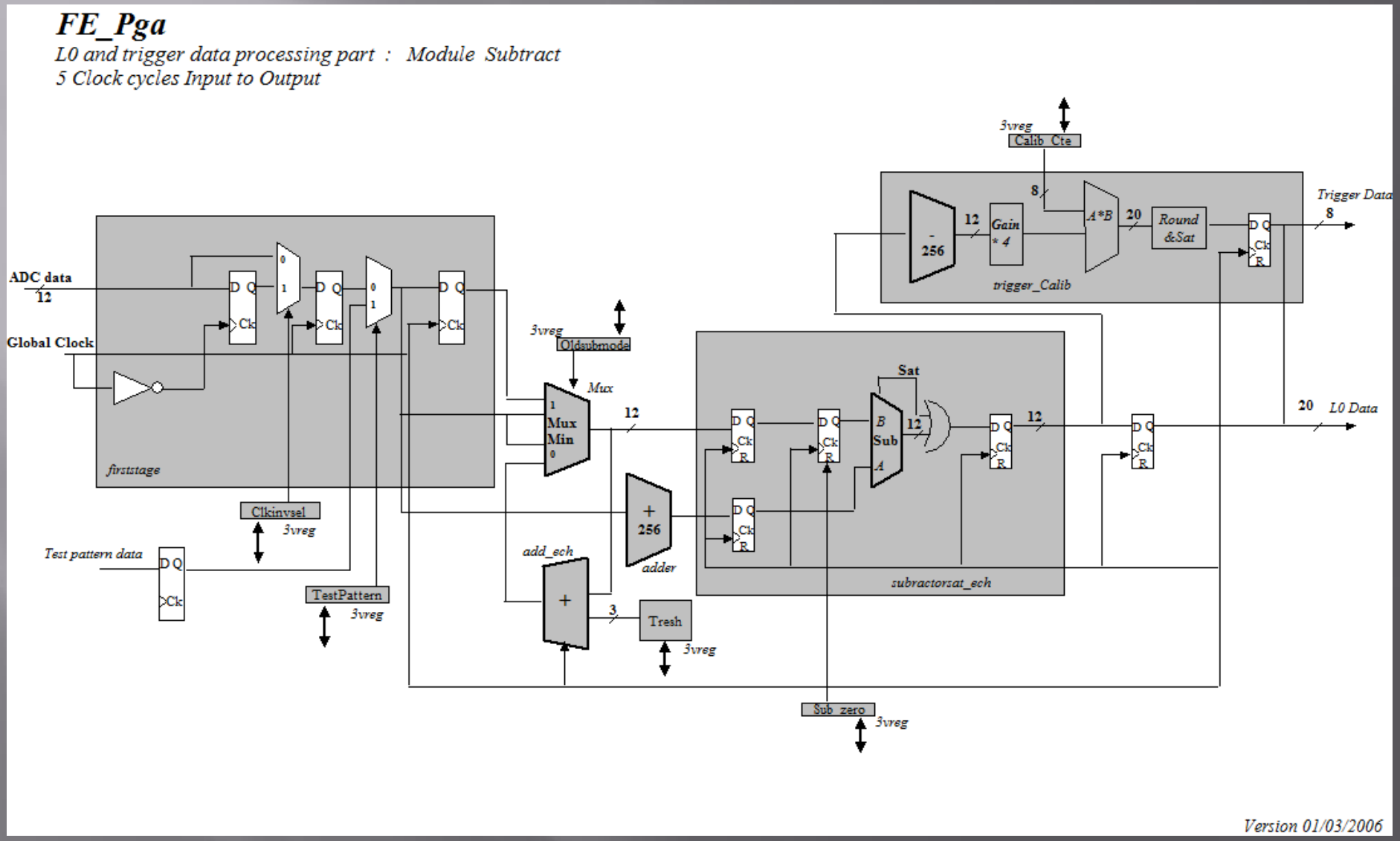
Block diagram of the FE board.



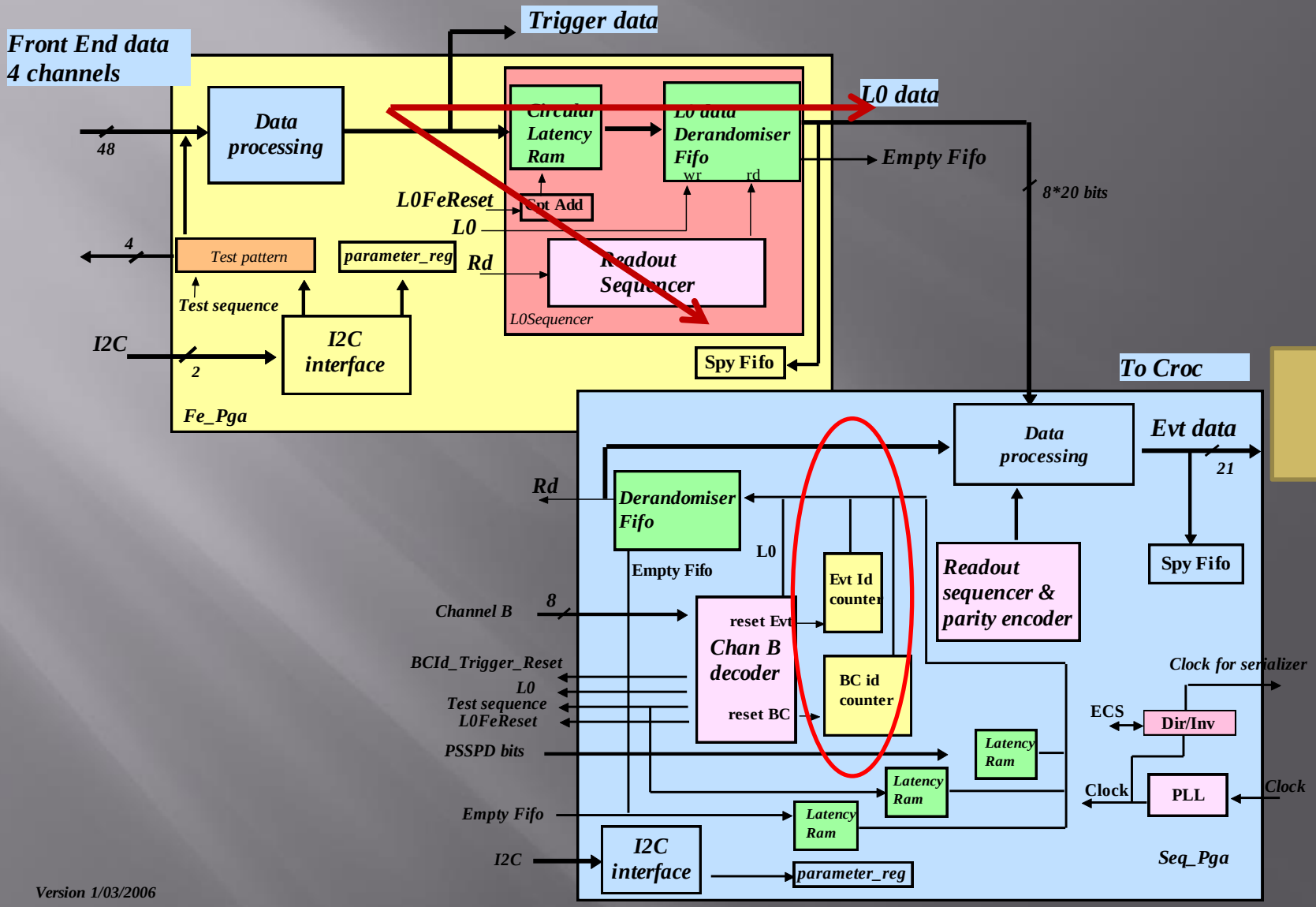
Fe PGA -> data processing part



Fe PGA -> Data processing part

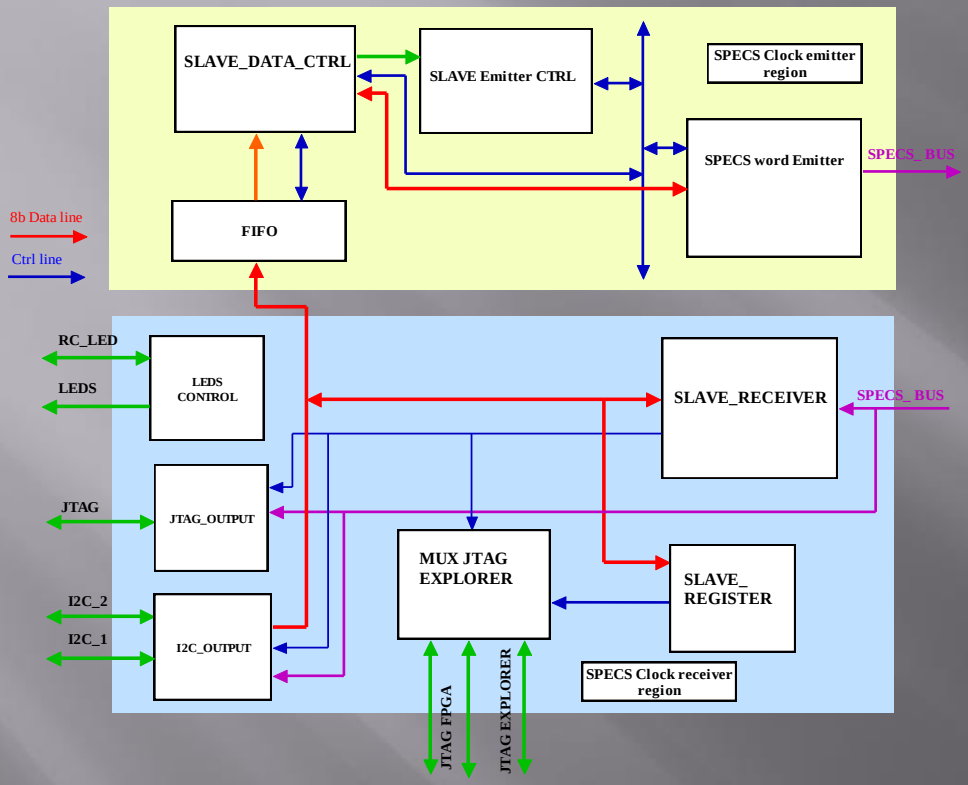


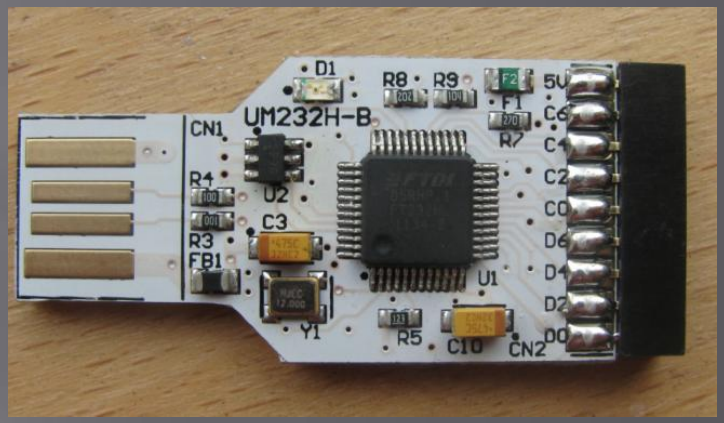
Front-end PGAs



Version 1/03/2006

Glue PGA -> GBT SCA or GBT decoder and USB 2 and glue logic





FTDI USB decoder cannot be implemented on the board. Use the UM 232 H with the Glue PGA to generate parallel bus , JTAG and I2C for test purpose.

Can we decode the GBT protocole to the SCA inside the GLUE and generate the JATAG and SPI .

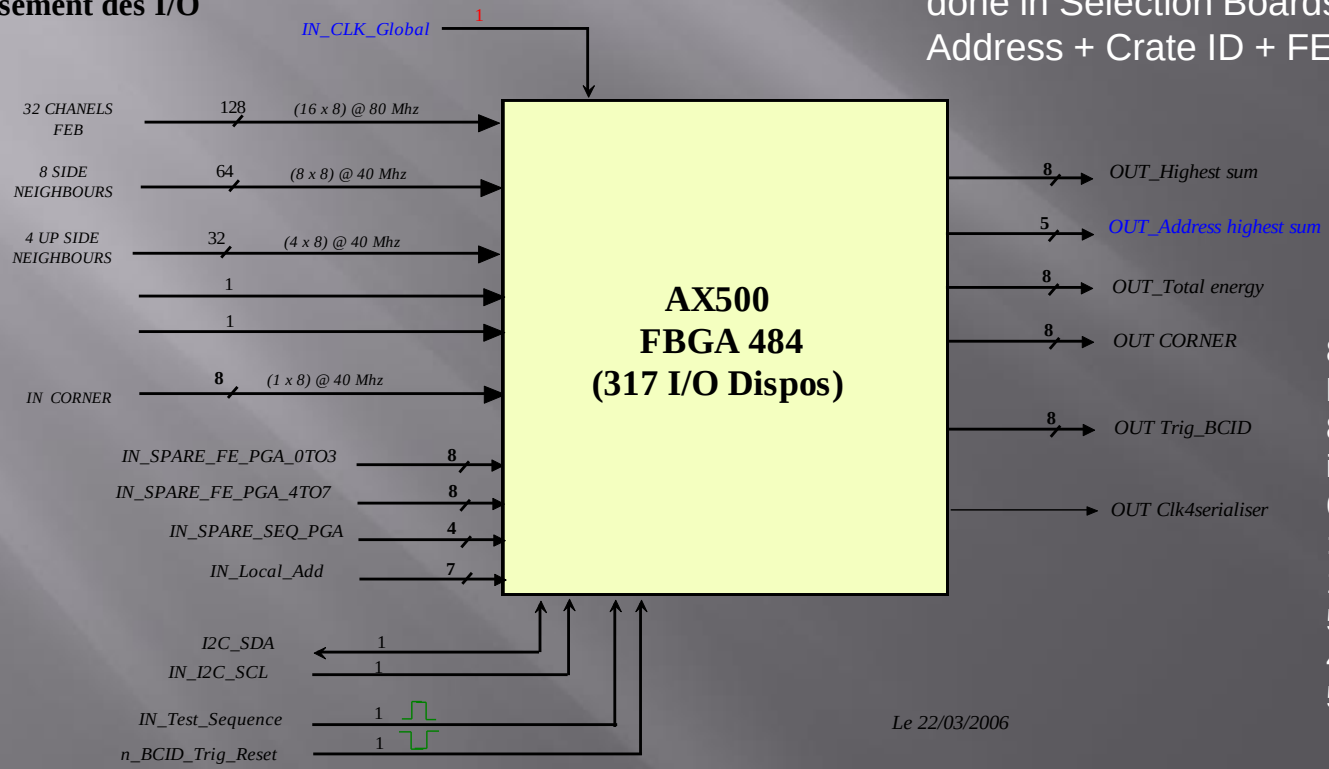
LLT data

The TrigFPGA on the FEB computes a local address (cell id between 0 and 31)
A more detailed address is needed :

- To match HCAL and ECAL related cells to be able to sum their ET (was done in TVB before)
- Absolute « official » address needs to be build for each address sent to « L0DU » and to the DAQ, in the format [Detector, Area, Row, Col] (was done in Selection Boards before, using Local Address + Crate ID + FEB ID)

Trig_PGA : AX500 - FBGA 484 (317 I/O Dispos)

Recensement des I/O



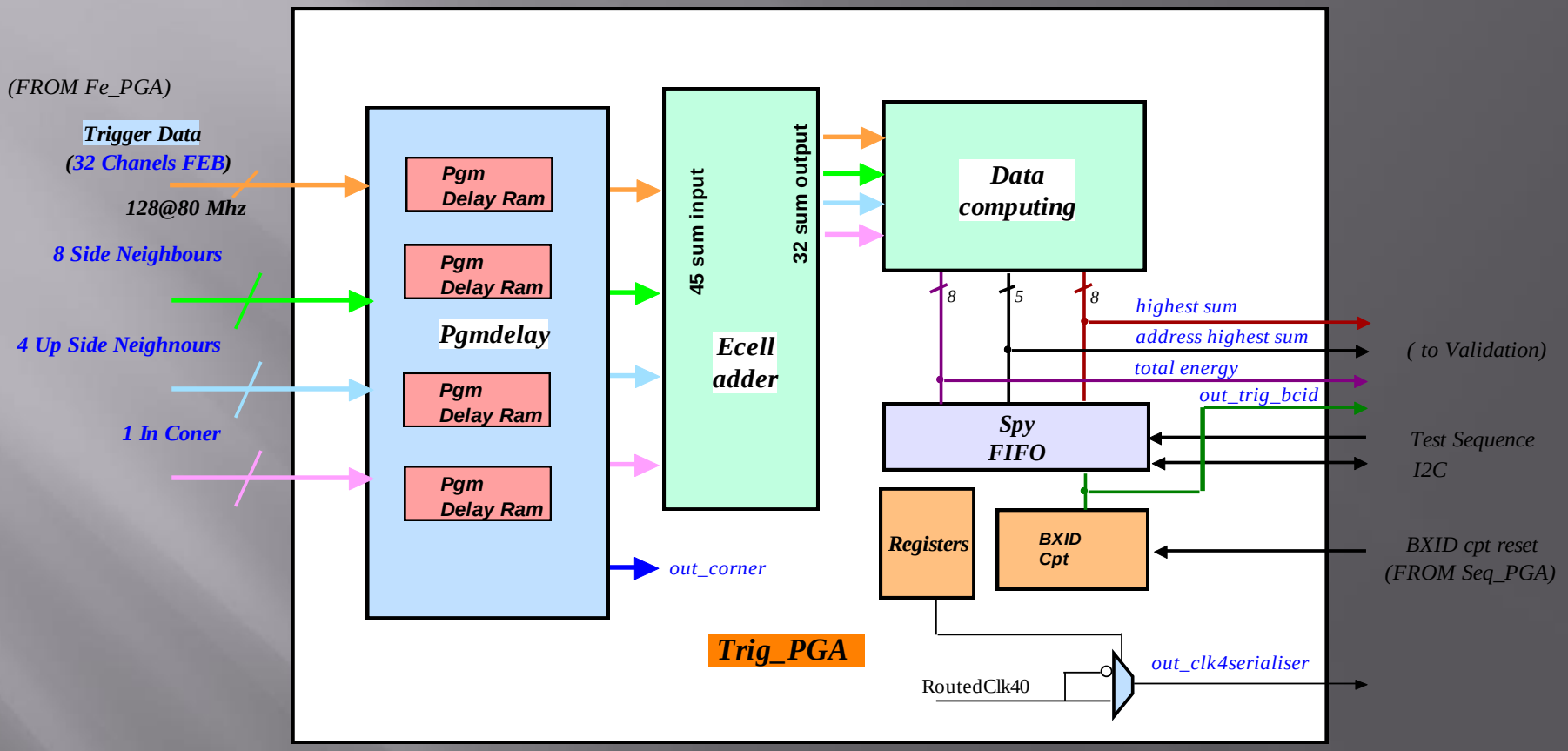
8b MaxET : Trig40 selects the highest over all inputs
8b SumET : Trig40 adds all inputs
6b Mult_ECAL or Mult_HCAL : Trig40 adds all inputs
12b BXID
5b local address
4b FEB ID
5b Crate ID

I/O Used : 306 - Total : 317 Whose 266 inputs, 39 outputs, 1 bidirectional.

Fonctionalities kept

- Since channels come from different locations, they have to be ***time-aligned*** before the computation:
  - Each different source (card cells, up, side and corner neighbours) can be ***delayed independently*** by 25 ns steps in the range 0 – 15x25 ns.
  - Neighbours via backplane arrive first, then channels on the same board (because they are multiplexed at 80 MHz), then neighbour via cables and the corner.
- A BxId counter is incremented and sent with trigger candidates. The reset of the BxId is ***delayed*** by a delay coded on 12 bits (0<delay<4096) and loaded by ECS.
- All input channels can be ***individually masked*** in order to remove them from the trigger computation. By default, at start-up, all channels are masked. They are then un-masked loading registers by ECS.
- The calibration command (activating the writing of 256 consecutive events in the Spy RAM) can be ***delayed*** by: 0<=delay<4096.

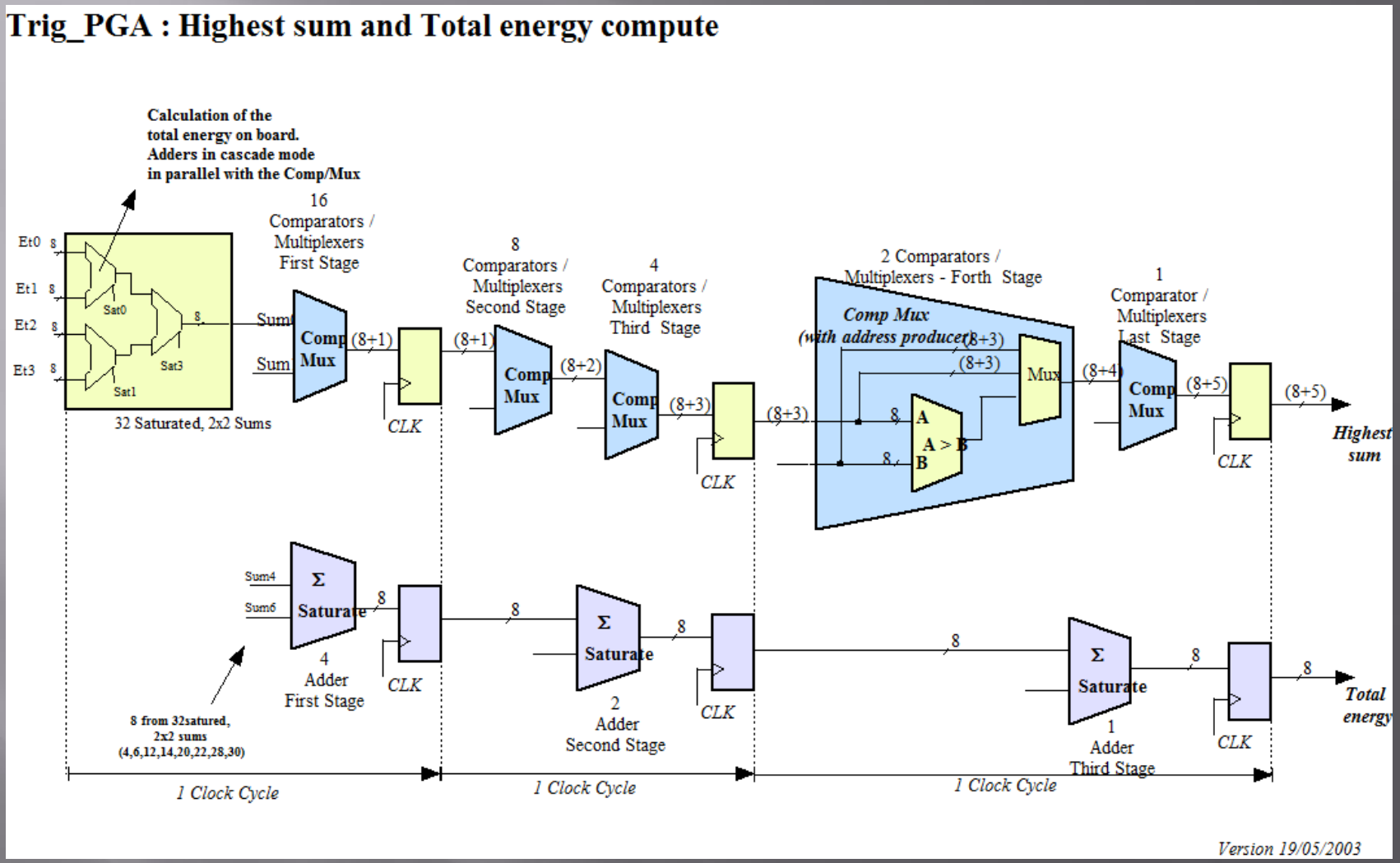
Global View of Trig_pga



Global View, Trig_PGA

Version 22/03/2006

Detail View


Trig_PGA : Highest sum and Total energy compute
Calculation of the total energy on board. Adders in cascade mode in parallel with the Comp/Mux
16 Comparators / Multiplexers First Stage
8 Comparators / Multiplexers Second Stage
4 Comparators / Multiplexers Third Stage
2 Comparators / Multiplexers - Forth Stage
1 Comparator / Multiplexers Last Stage
Et0
Et1
Et2
Et3
Sat0
Sat1
Sat3
32 Saturated, 2x2 Sums
Comp Mux
(8+1)
(8+2)
(8+3)
(8+4)
(8+5)
CLK
Comp Mux (with address producer)
Mux
A
B
A > B
Highest sum
Sum4
Sum6
Saturate
4 Adder First Stage
2 Adder Second Stage
1 Adder Third Stage
8 from 32satured, 2x2 sums (4,6,12,14,20,22,28,30)
Total energy
1 Clock Cycle
1 Clock Cycle
1 Clock Cycle
Version 19/05/2003

Power distribution

Board Consumption :
+5 V = 4A
+3.3V = 2 A
-5V = 1 A