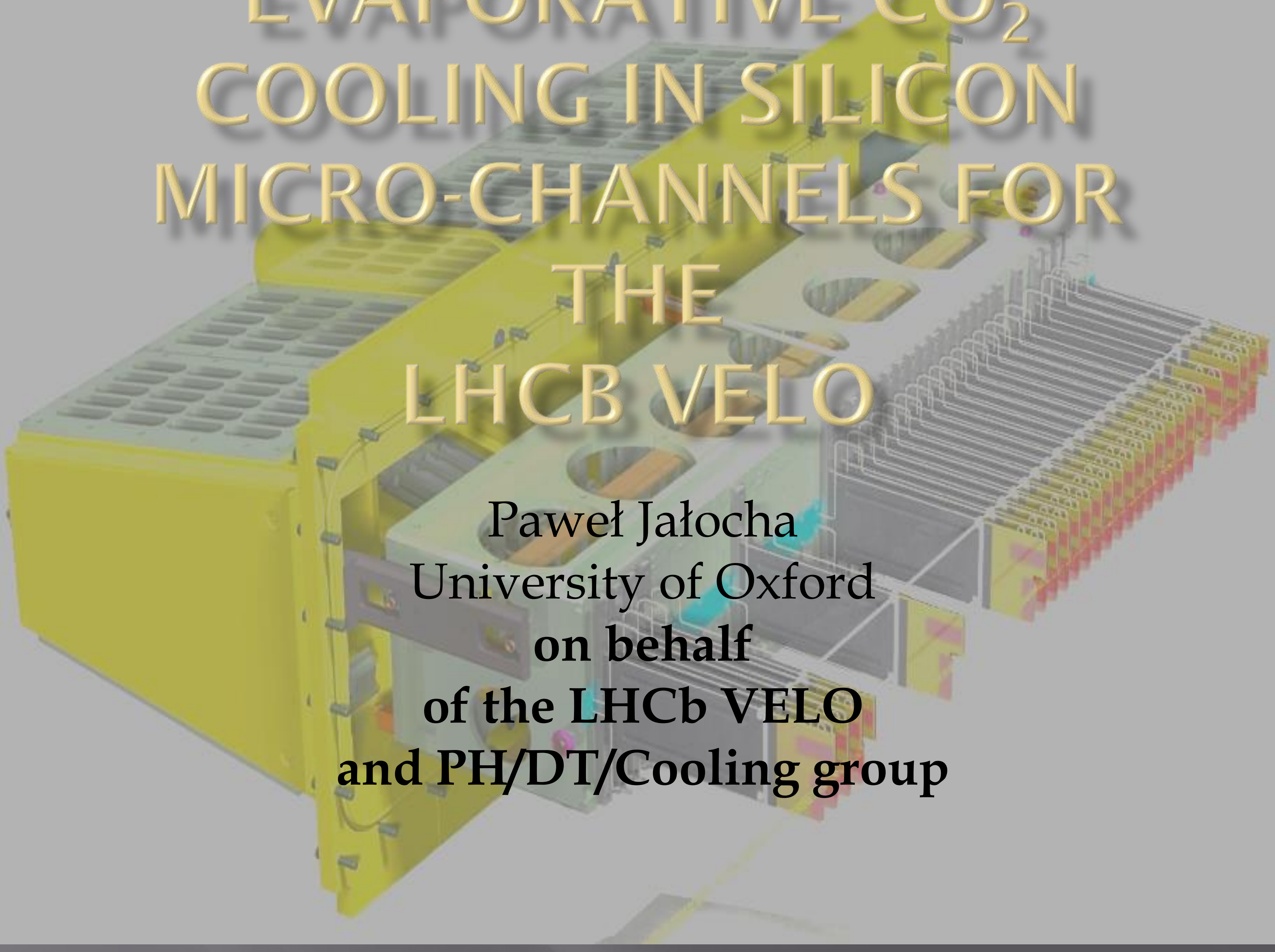
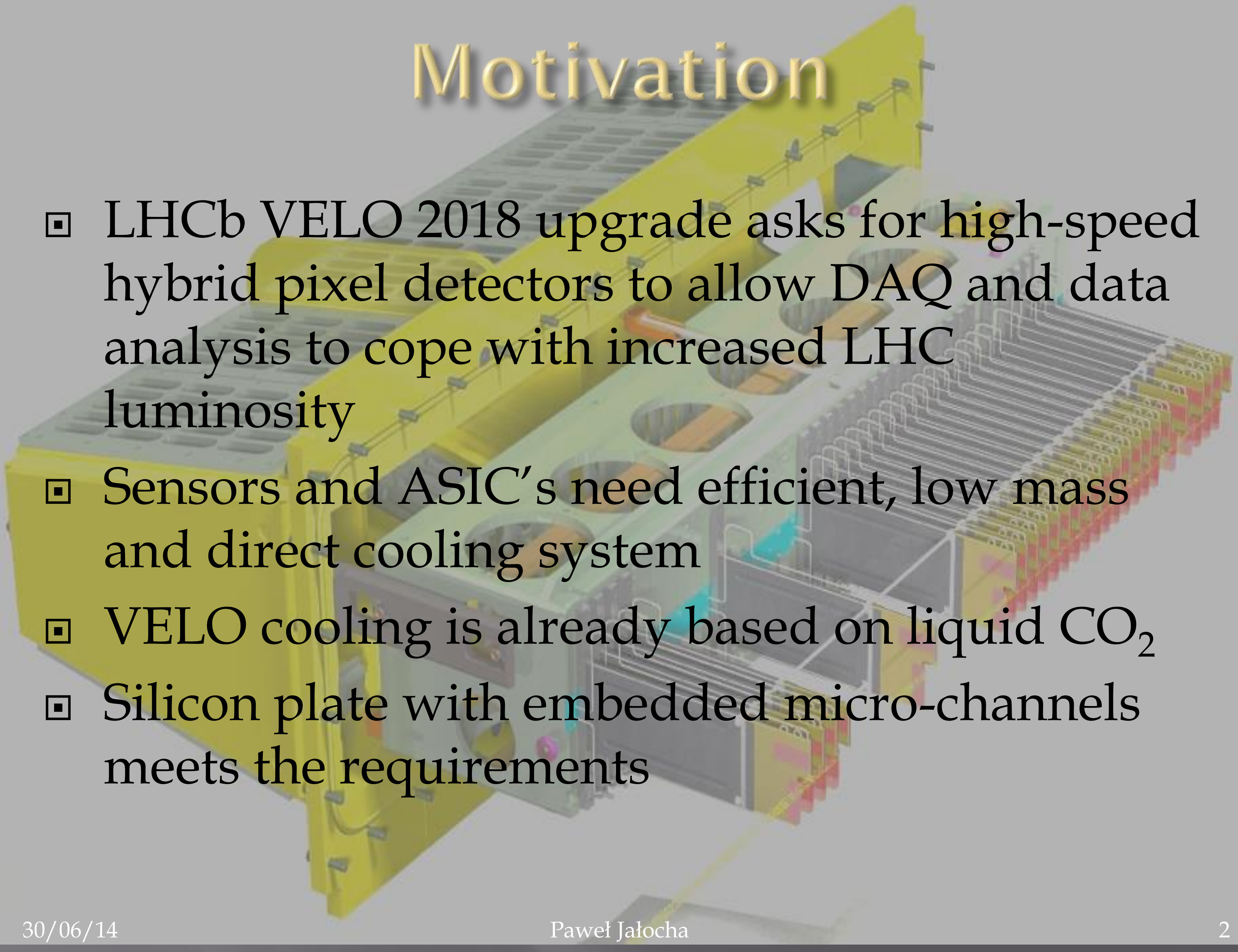
EVAPORATIVE CO$_2$ COOLING IN SILICON MICRO-CHANNELS FOR THE LHCB VELO

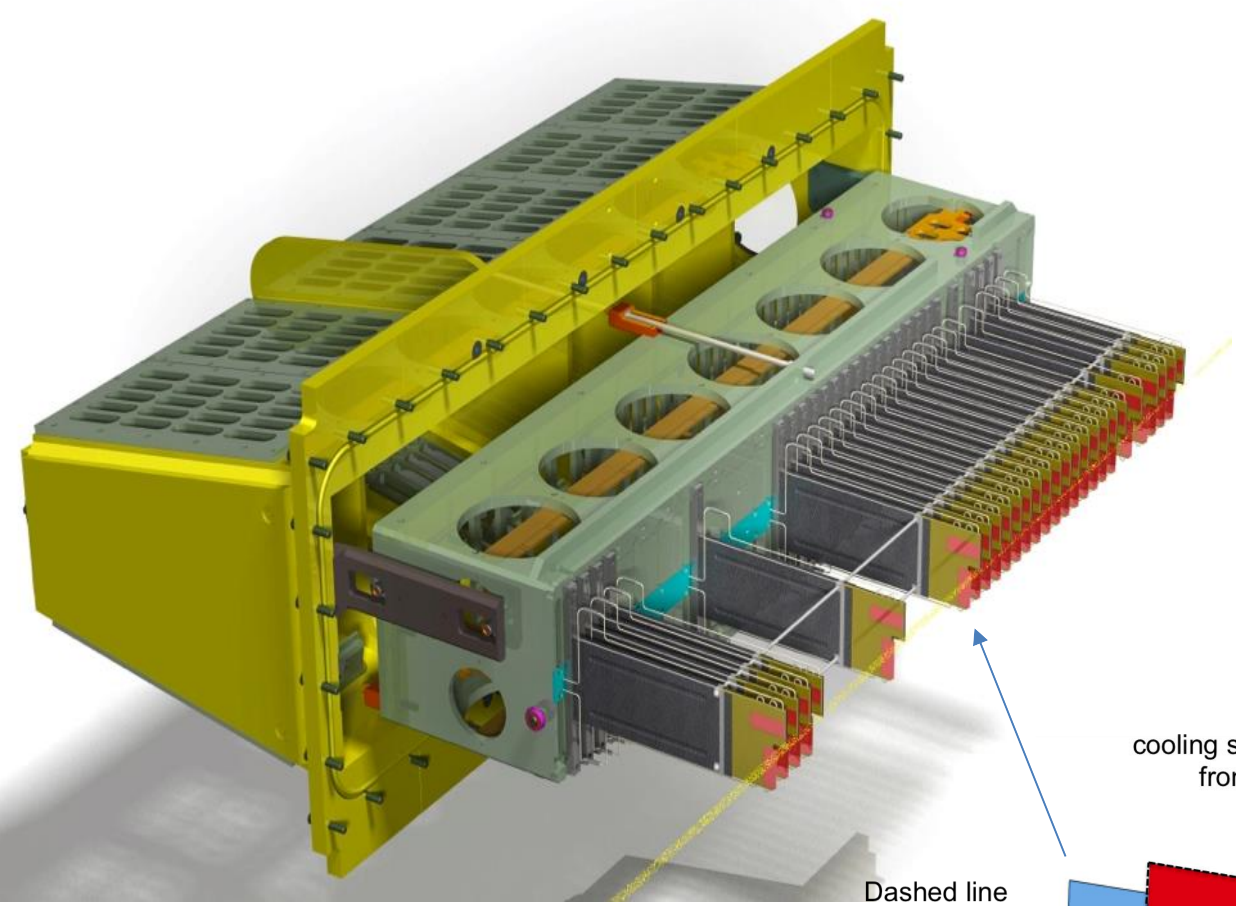


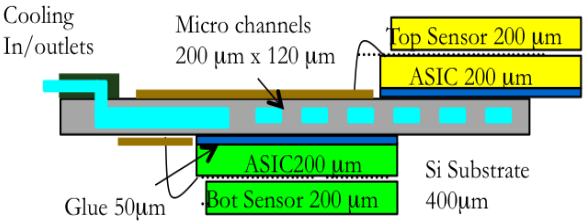
Paweł Jałocha
University of Oxford
on behalf
of the LHCb VELO
and PH/DT/Cooling group

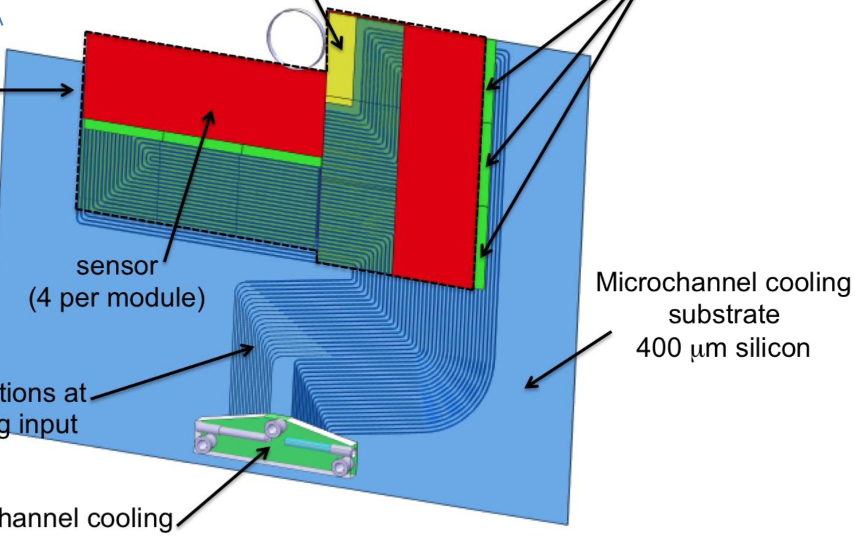
Motivation

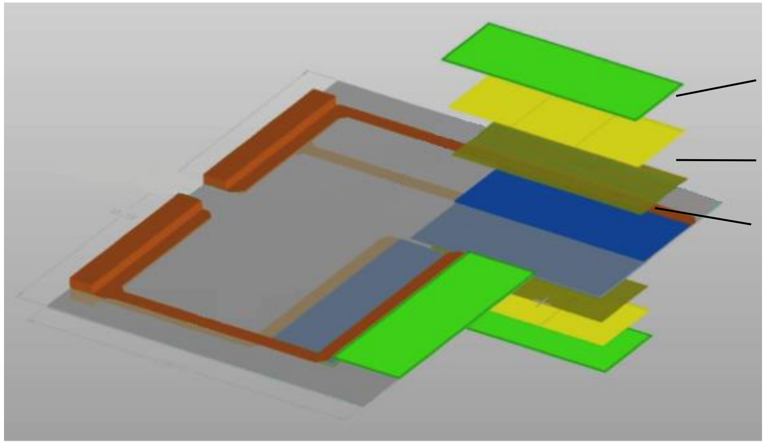


- LHCb VELO 2018 upgrade asks for high-speed hybrid pixel detectors to allow DAQ and data analysis to cope with increased LHC luminosity
- Sensors and ASIC's need efficient, low mass and direct cooling system
- VELO cooling is already based on liquid CO_2
- Silicon plate with embedded micro-channels meets the requirements



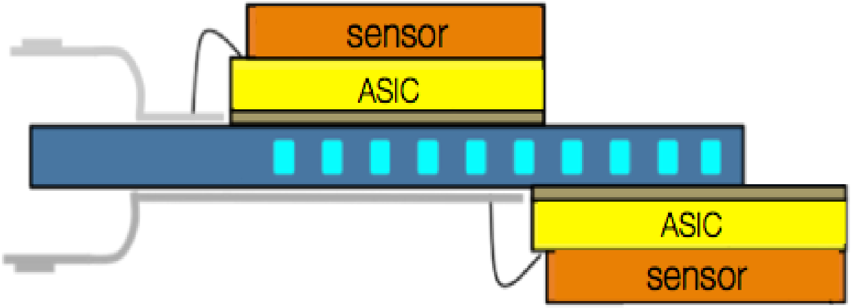

Cooling In/outlets
Micro channels 200 µm x 120 µm
Top Sensor 200 µm
ASIC 200 µm
ASIC200 µm
Bot Sensor 200 µm
Glue 50µm
Si Substrate 400µm

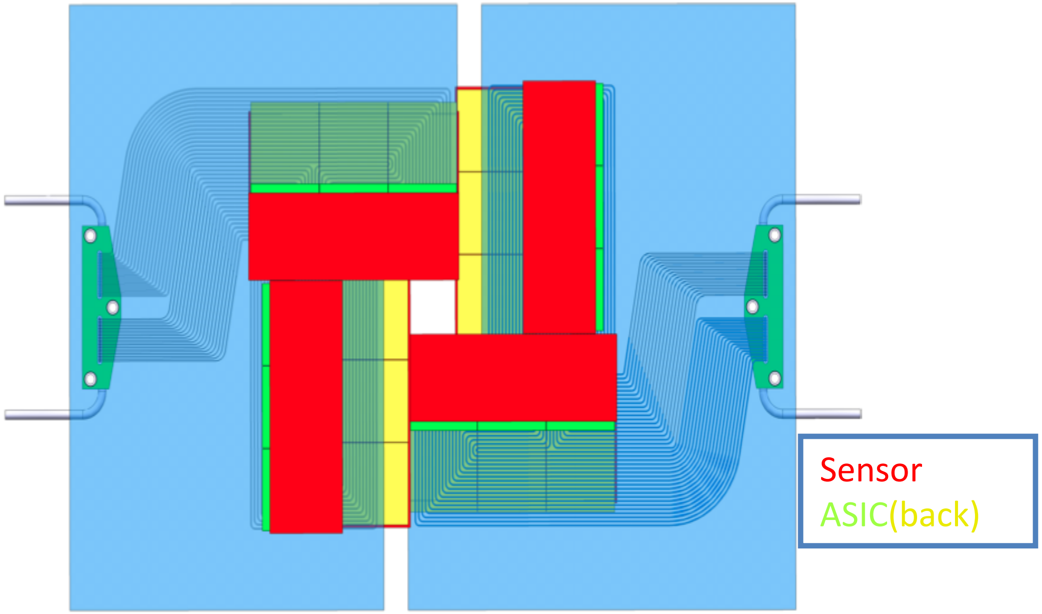

cooling substrate retracted from module tip
3 ASICs per sensor
Dashed line indicates sensitive region
sensor (4 per module)
Microchannel cooling substrate 400 µm silicon
restrictions at cooling input
Microchannel cooling connector


sensor
ASIC
glue

Cooling requirements for VELO

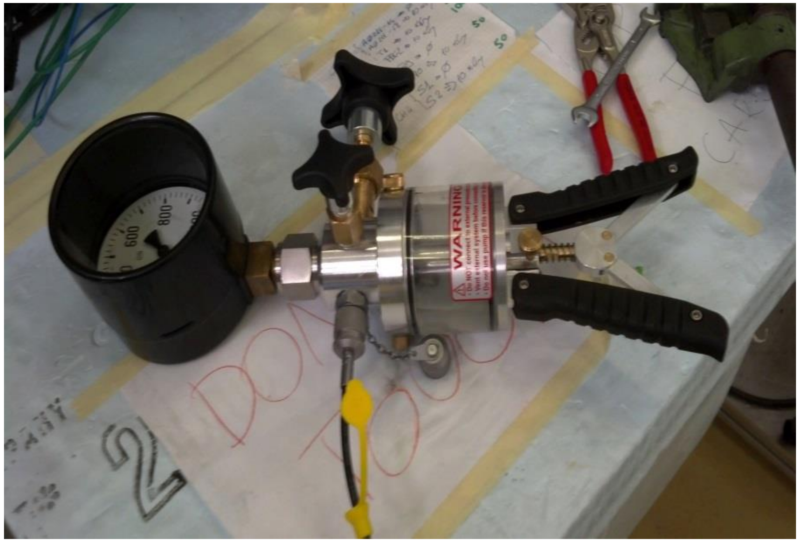
- Keep sensor temperature below -20˚C to minimize the effect of radiation damage and to avoid thermal runaway.
- Bring cooling power directly where it is needed using least amount of material (detector tip is the hottest spot)
- The total power per module is ~26W (2W per ASIC and ~2W on the innermost sensors)
- Cooling active area (24cm^2)
- Power area density: 1.1W/cm^2
- 5mm of uncooled ASIC/sensor (overhang) close to the beam to reduce the amount of material



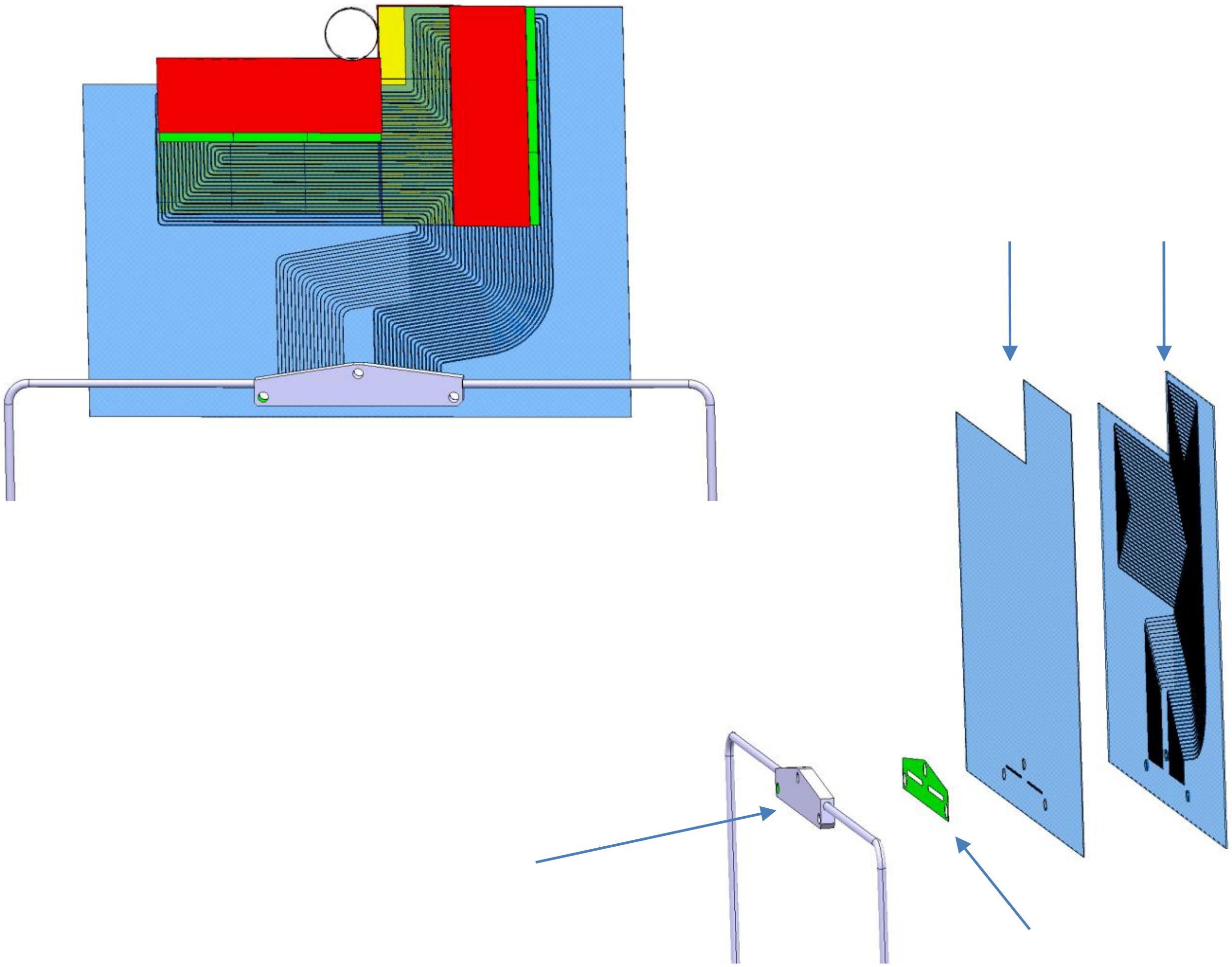


Mechanical requirements

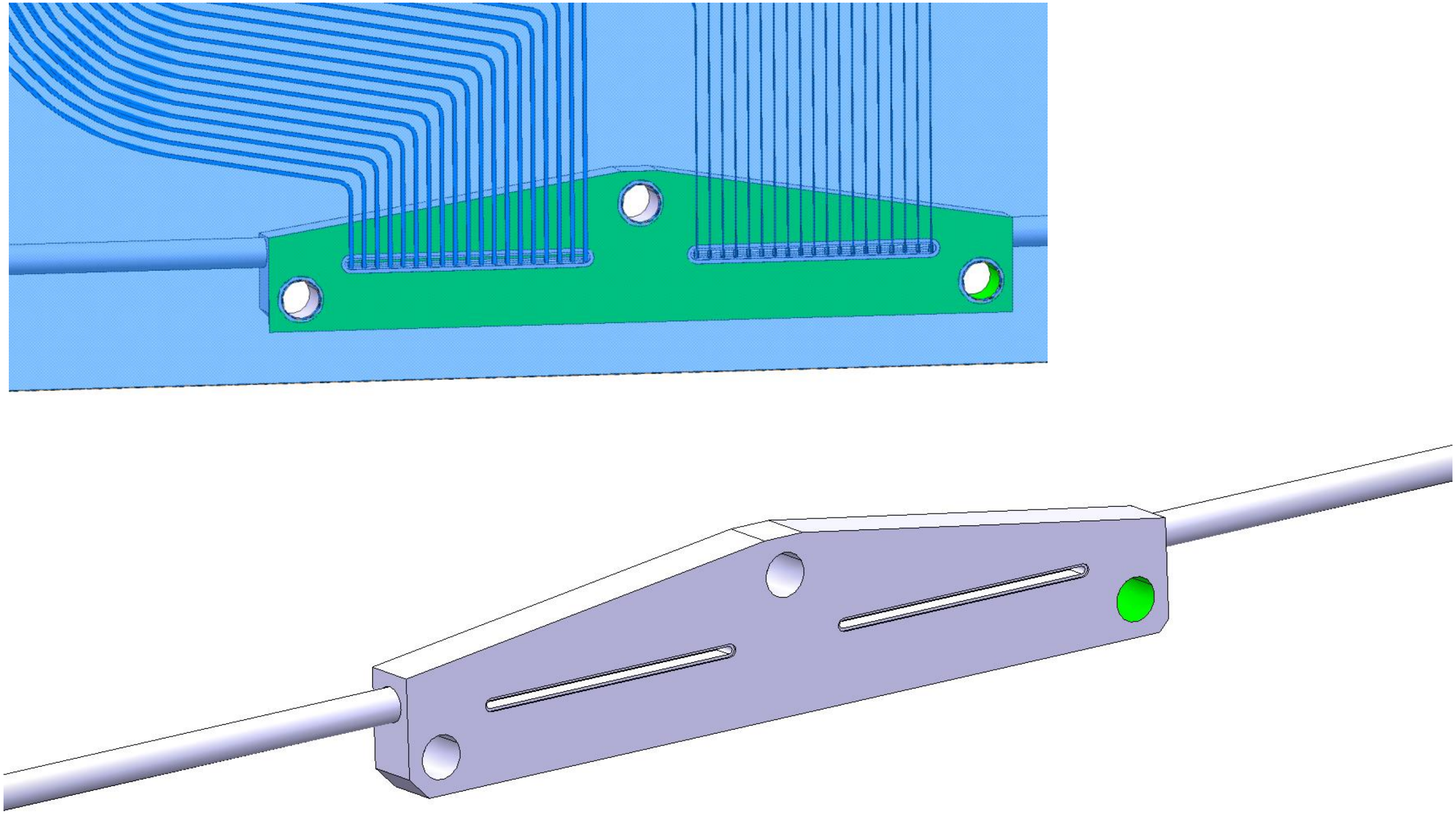
- Leak tight (secondary LHC vacuum !)
- The saturation CO_2 pressure is 65 bars @ 25˚C
  - Minimum pressure of 170 bars (factor 3 safety margin)
- Long term reliability
  - Cyclic pressure and temperature cycles



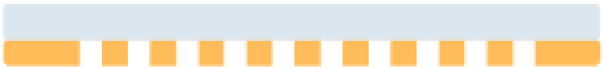
Micro-channel wafer layout



Micro-channel wafer layout: connector, inlets and outlets

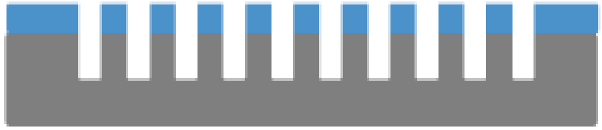


Micro-channels fabrication

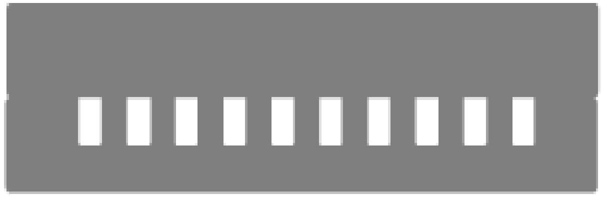


Photolithography mask

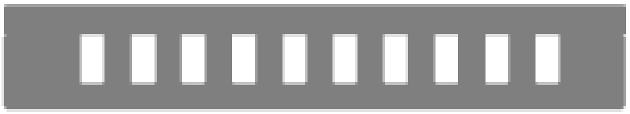
Photolithography process



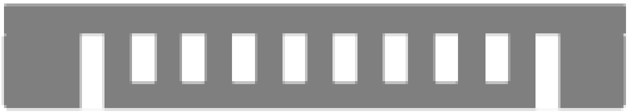
DRIE etching of channels



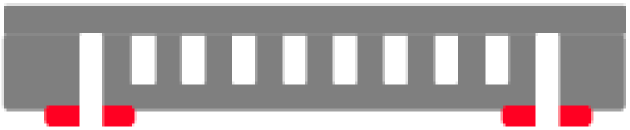
Si - Si direct bonding



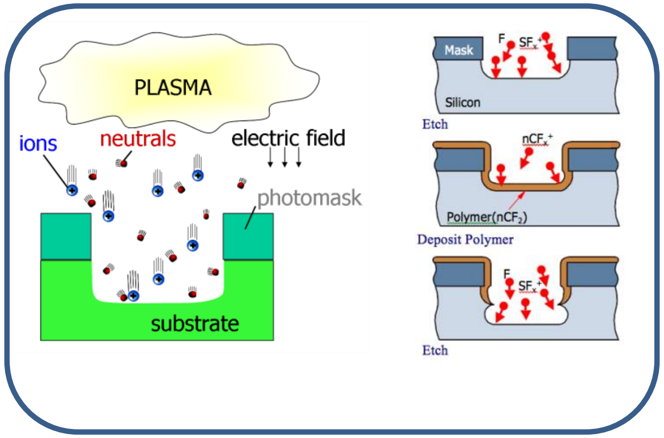
Thinning



Plasma etching of fluidic inlets



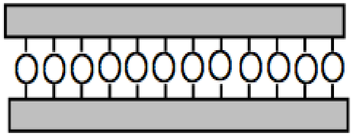
Metalization for soldering connectors

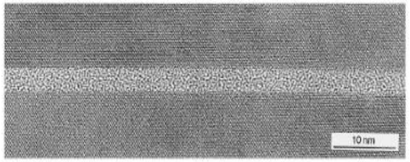


Pressure resistance

for two types of direct (fusion) bonding

Hydrophilic bonding

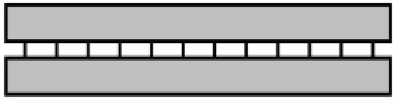


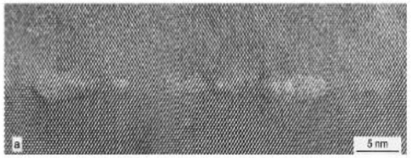


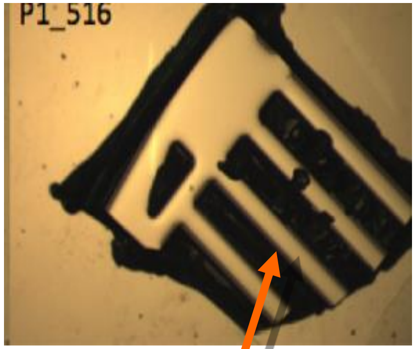
The bound was not strong enough!

The hydrophilic samples exploded with a pressure around 400 bars.

Hydrophobic bonding







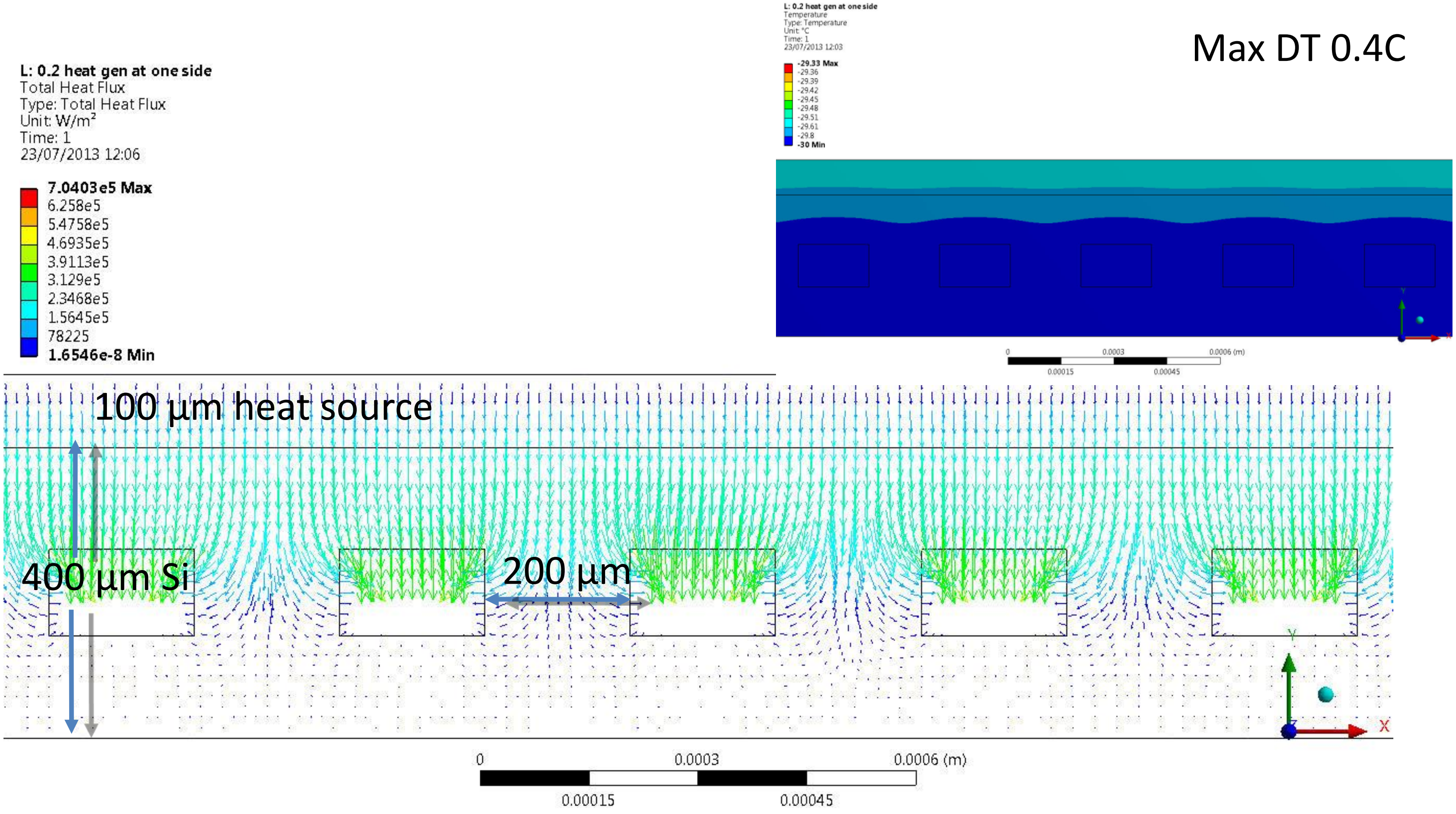
No delamination on the bounding areas!

The hydrophilic samples resisted up to 700 bars (pump limit).

Thermal simulation

- Optimize the spacing distance between the channels for the new layout
  - balance cooling efficiency against pressure resistance
- Simulation with a 3D model is done using ANSYS
  - Spacings of 500 µm, 600 µm, 700 µm and 1000 µm

Spacing simulation (0.2mm edge-to-edge – current design)



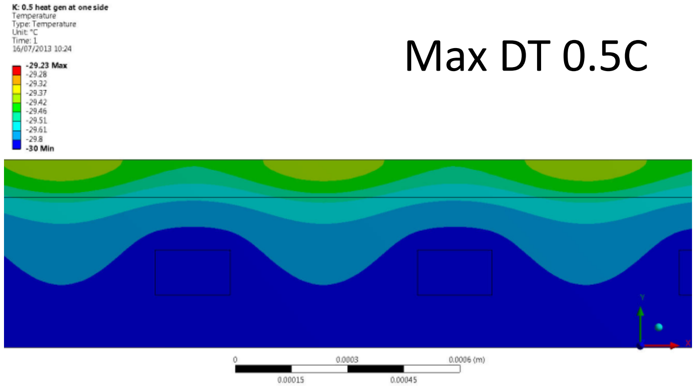
Max DT 0.4C

100 µm heat source

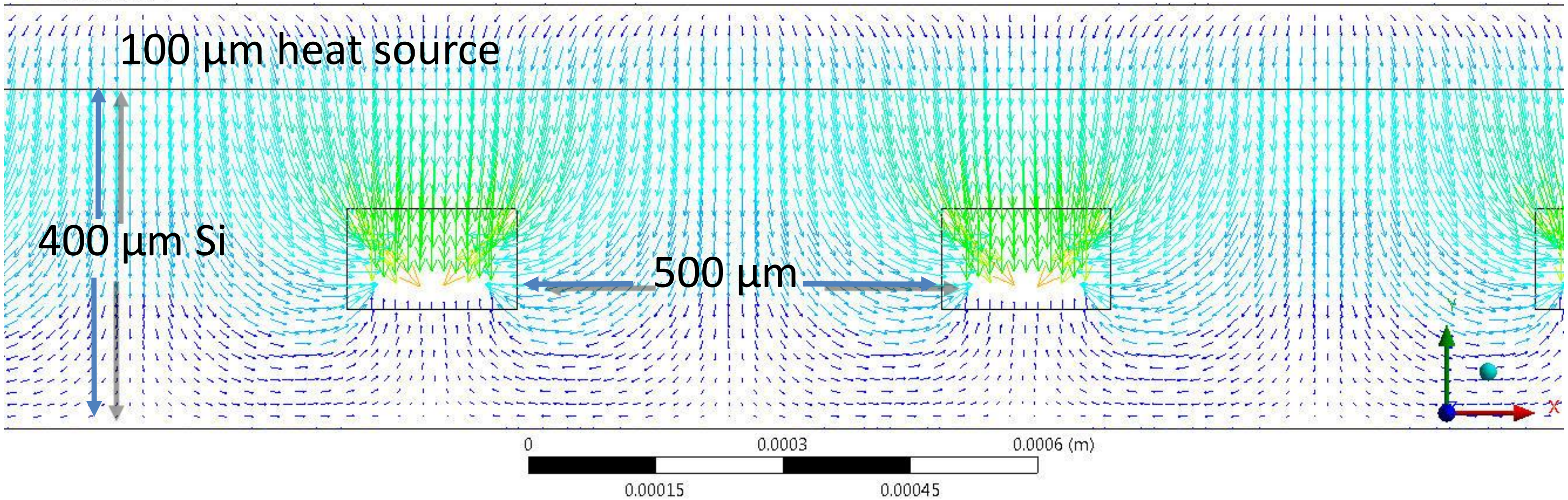
400 µm Si

200 µm

Spacing simulation (0.5mm edge-to-edge)



Max DT 0.5C



100 µm heat source

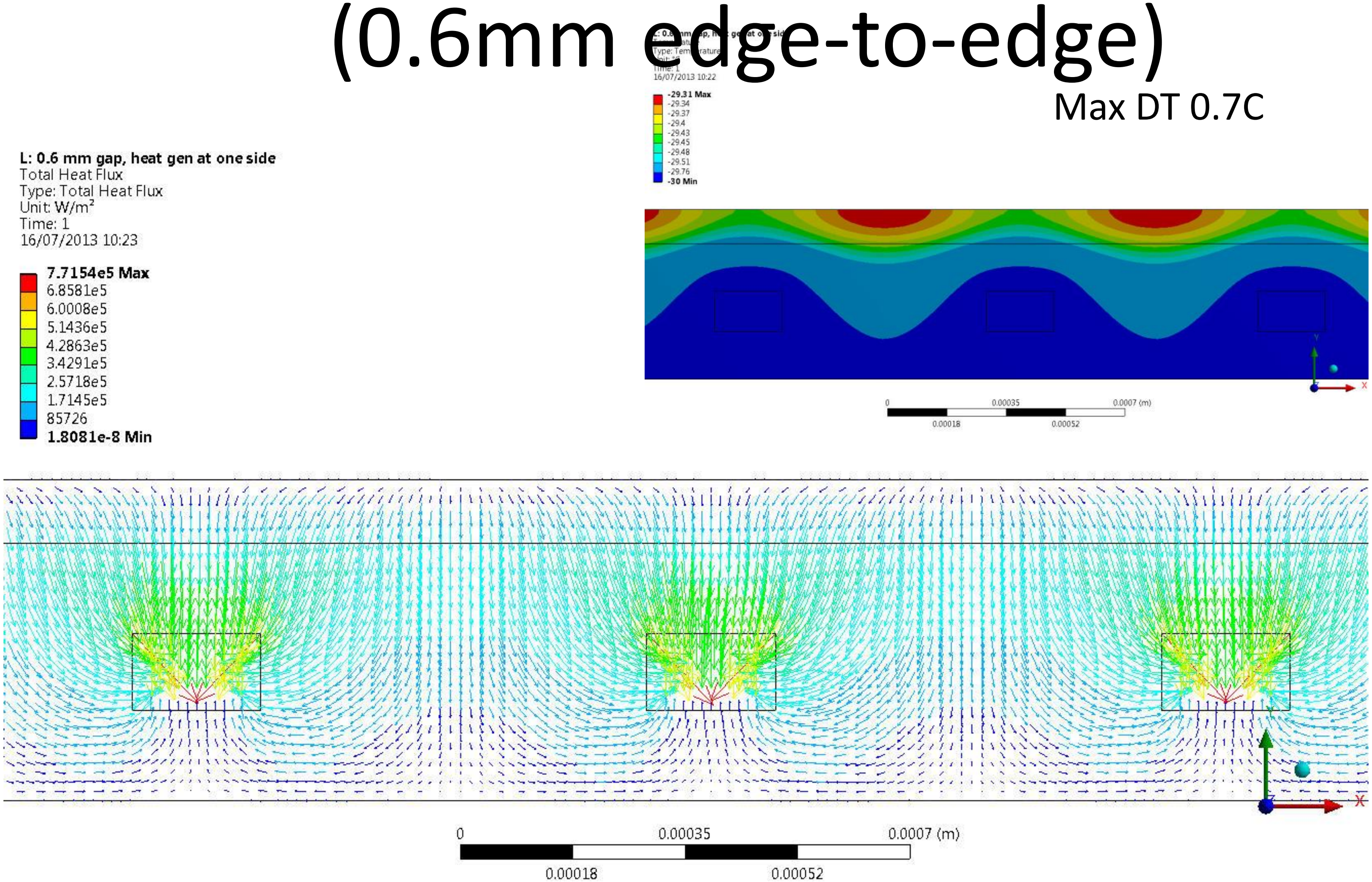
400 µm Si

500 µm

This is taken for the new layout

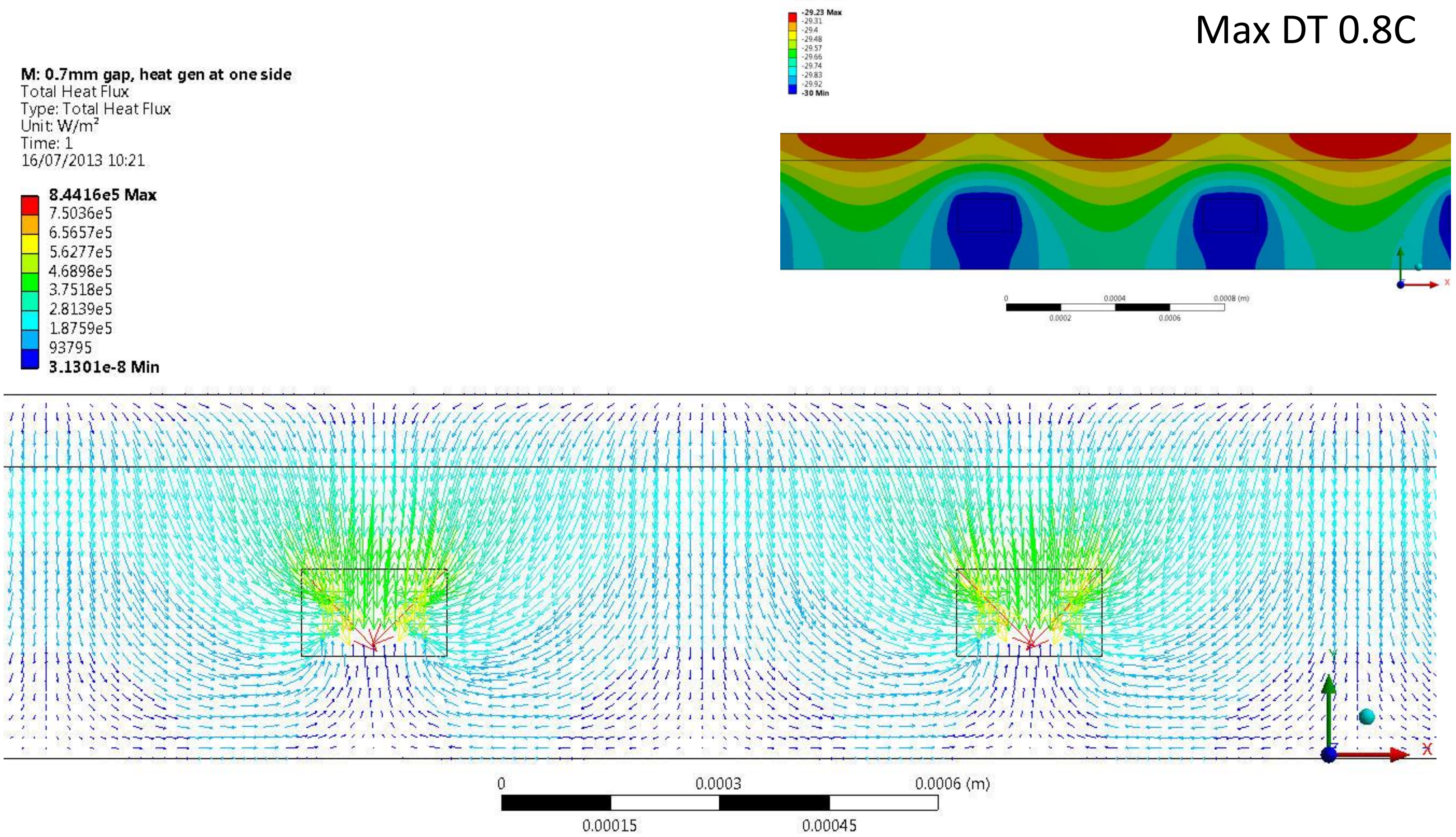
Spacing simulation (0.6mm edge-to-edge)

Max DT 0.7C



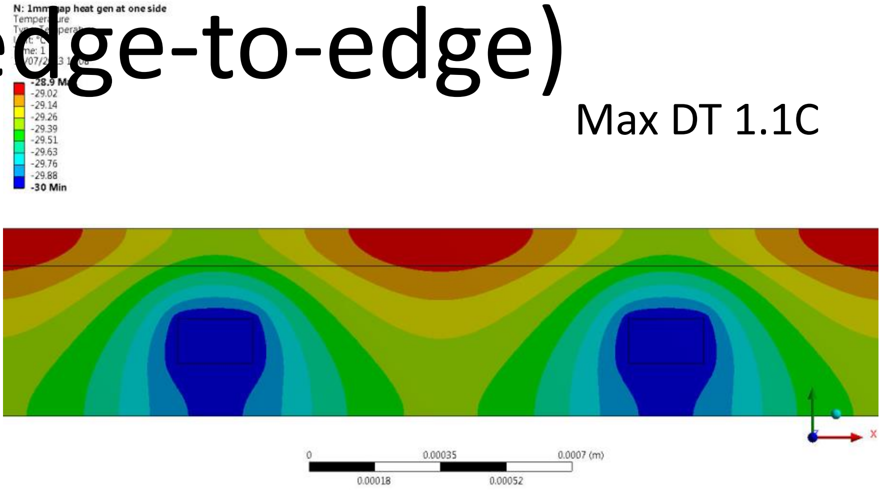
Spacing simulation (0.7mm edge-to-edge)

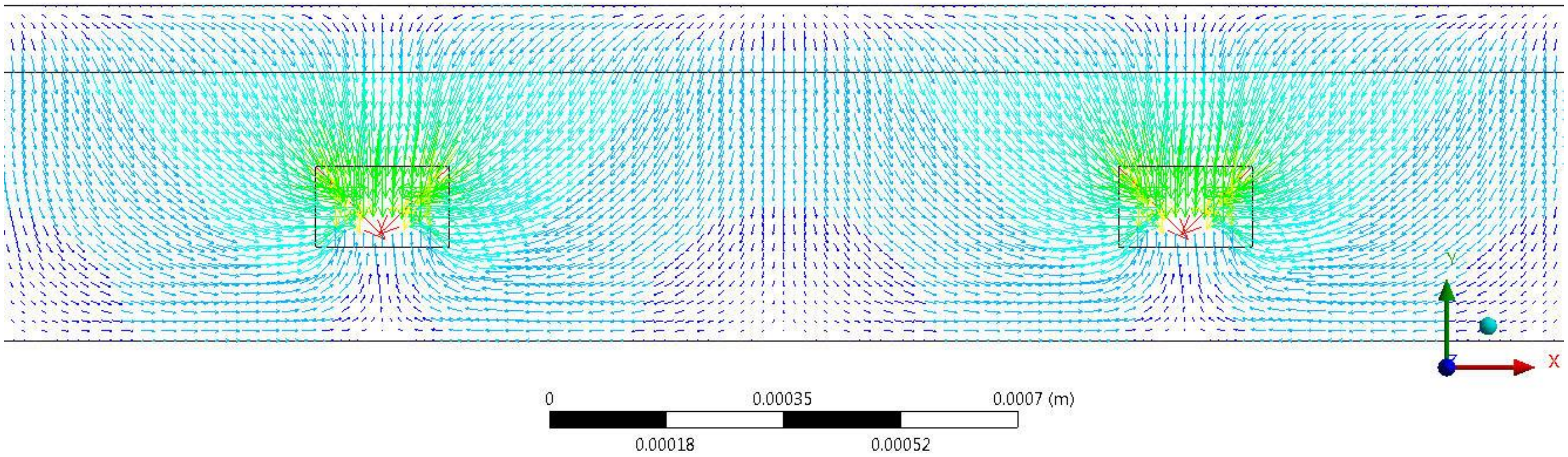
Max DT 0.8C



Spacing simulation (1mm edge-to-edge)

Max DT 1.1C

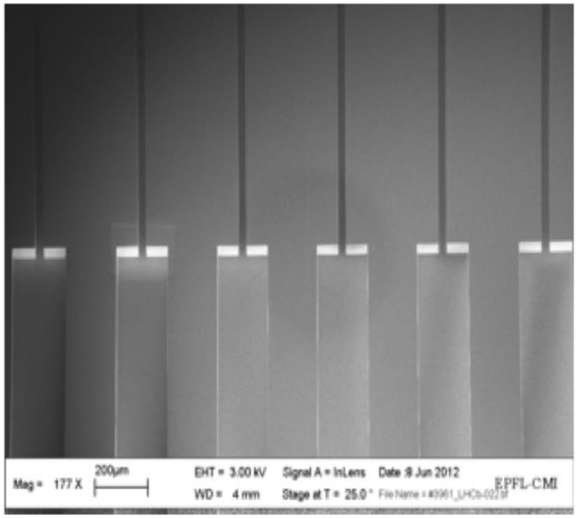


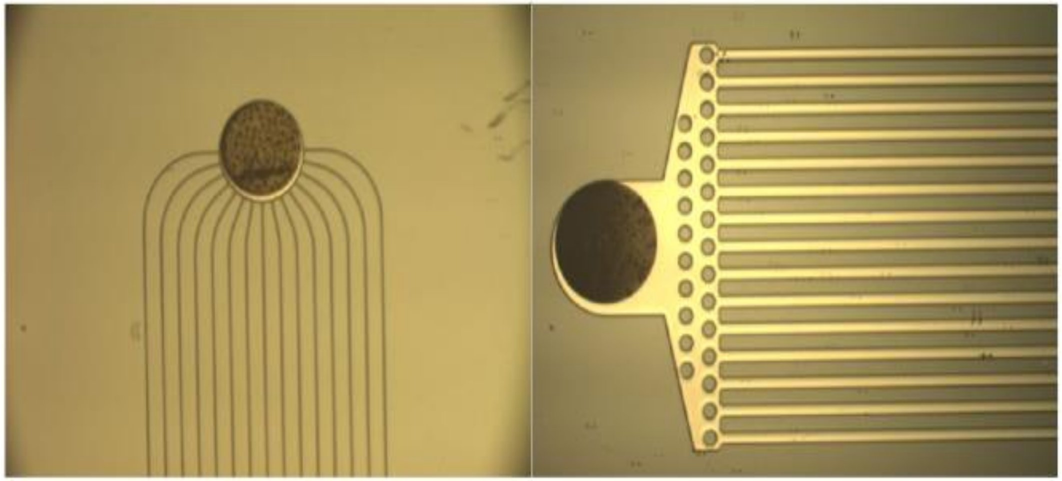


Micro-channels prototype: Snake I

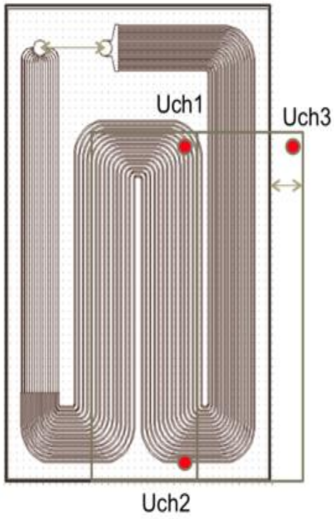
- “Snake I” prototype: 4 x 6 cm^2
- 380µm silicon bounded to 2 mm Pyrex
- Dimensions*
  - Restrictions: 70µm x 30µm
  - Micro-channels: 70µm x 200 µm
- The restrictions are designed to trigger the boiling
- It is critical to control the area on the output manifold

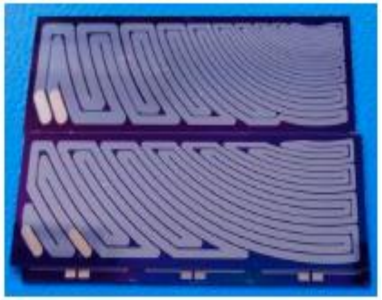
*The diameter of the human hair is between 17µm and 181µm.

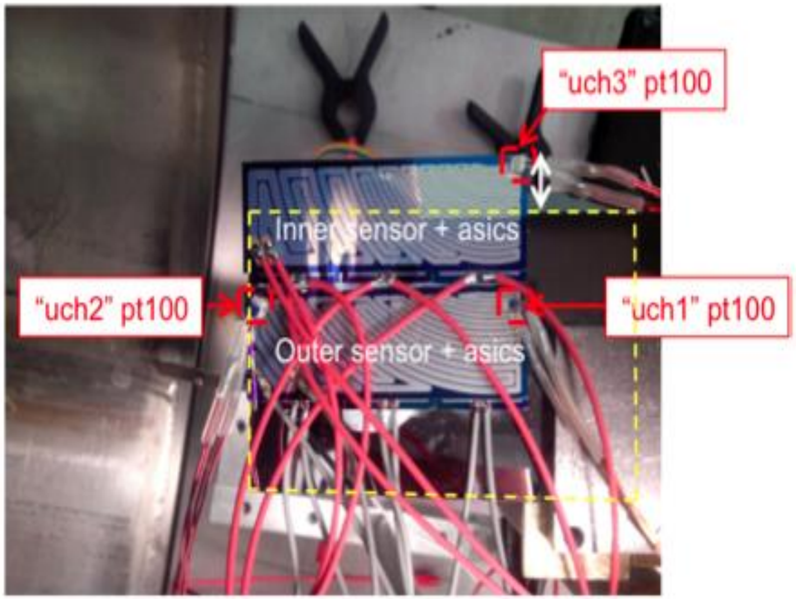




Cooling performance

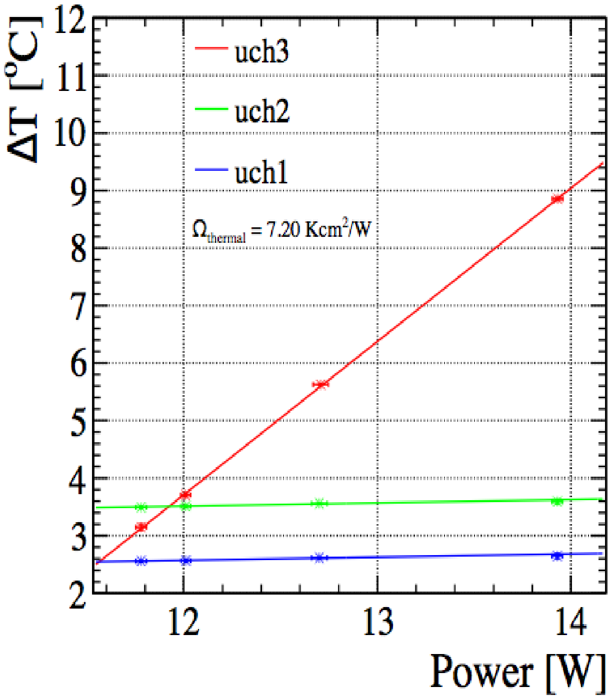






Glued surface: 11,34 cm2

CO2 connector



The end of lifetime expectations corresponds to ~13W and on this conditions the maximum ΔT across the module is less than 7˚C (apart from the sensor tip the difference is only 1˚C)

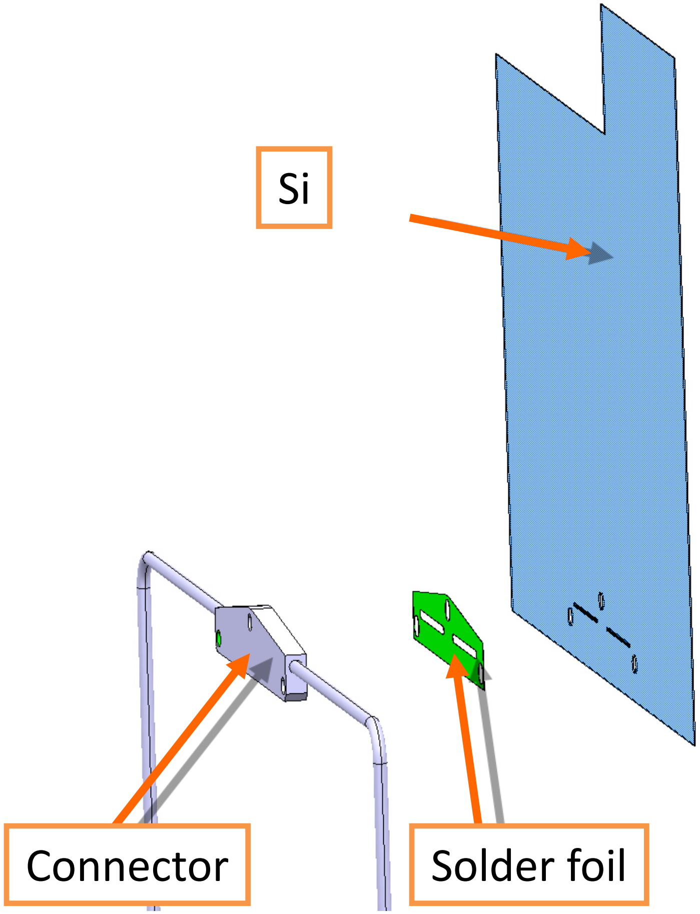
Supplying the micro-channel wafer with CO_2

- How to reliably join metal cooling pipes to a silicon wafer ?
- Metallize the silicon surface and solder
- Need to resist the pressure > 200 Bar
- Must not degrade with time (creep, corrosion)
- Must withstand numerous thermal cycles

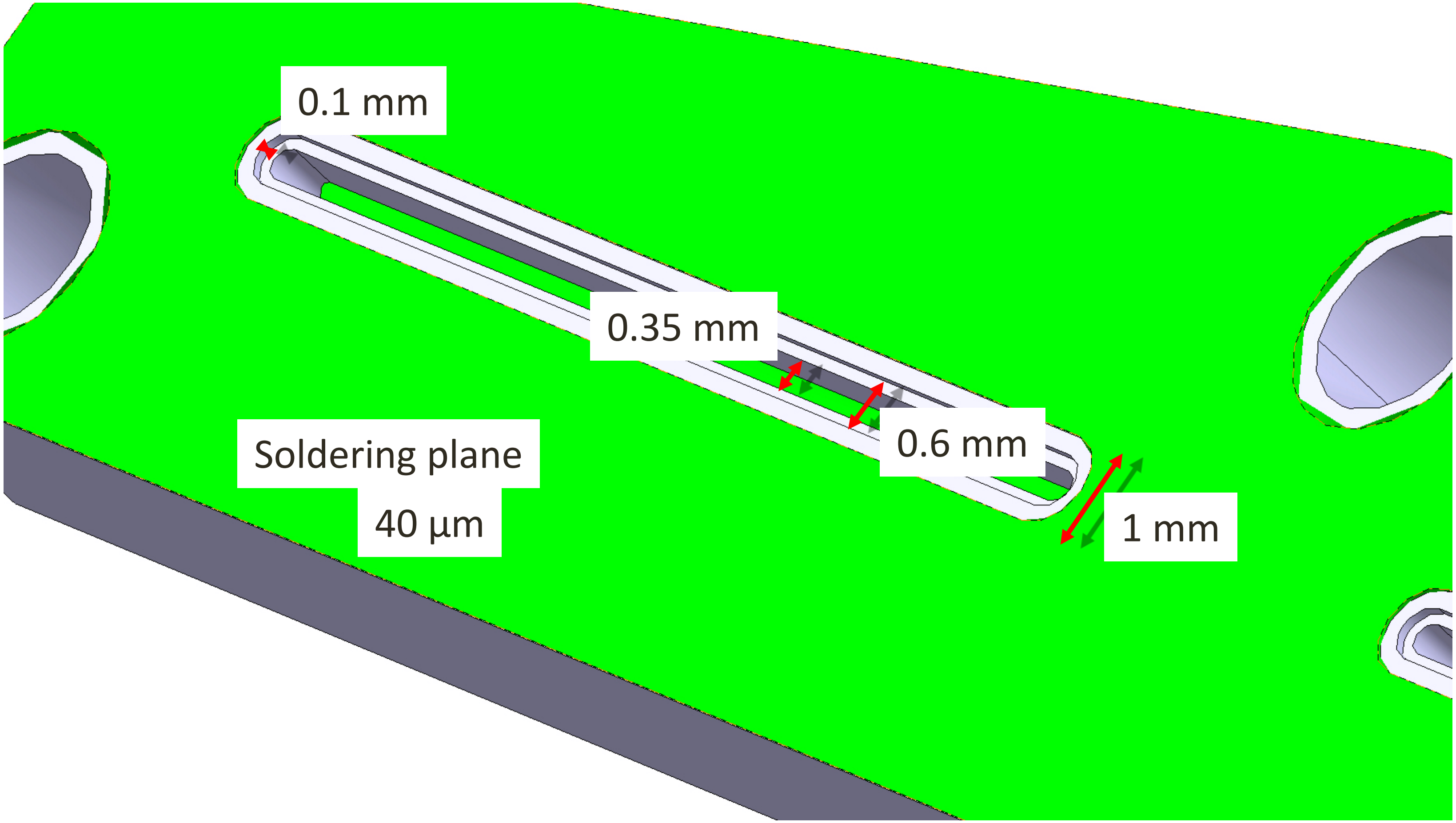
Connector soldering

- Attachment of the fluidic connector on the silicon substrate
- Requirements:
  - No interconnections between the voids
  - Maximum dimensions of the void should not be bigger than 1 mm
  - It should corresponds to less than 5 % of the total soldering area
  - No flux (prevent corrosive effects on long term)

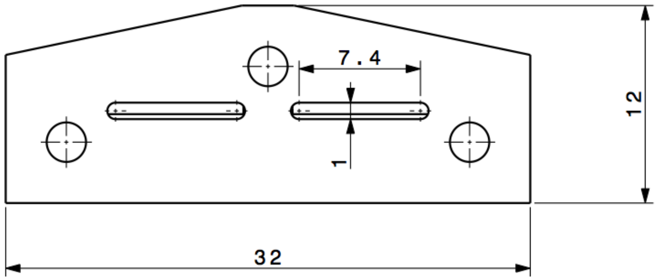
- Preform foil soldering technique with frame on vacuum

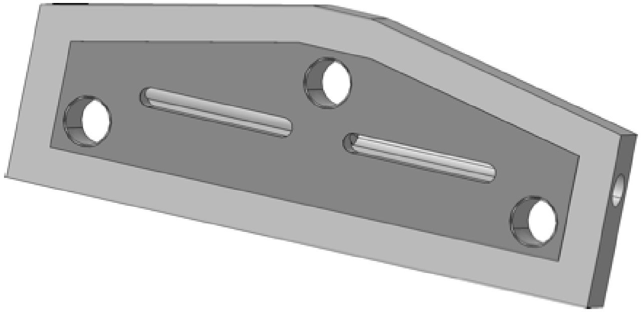


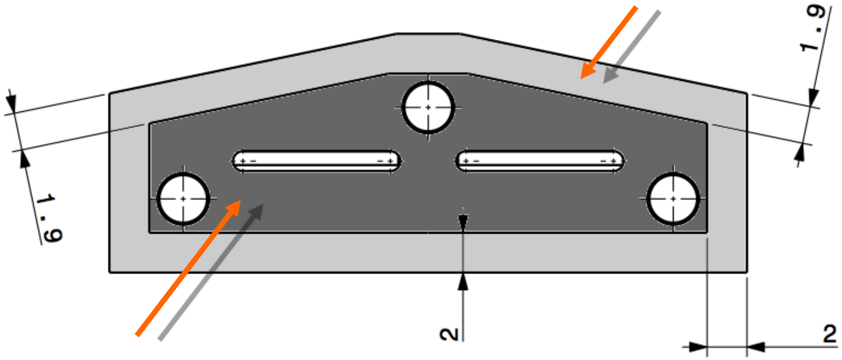
Connector soldering



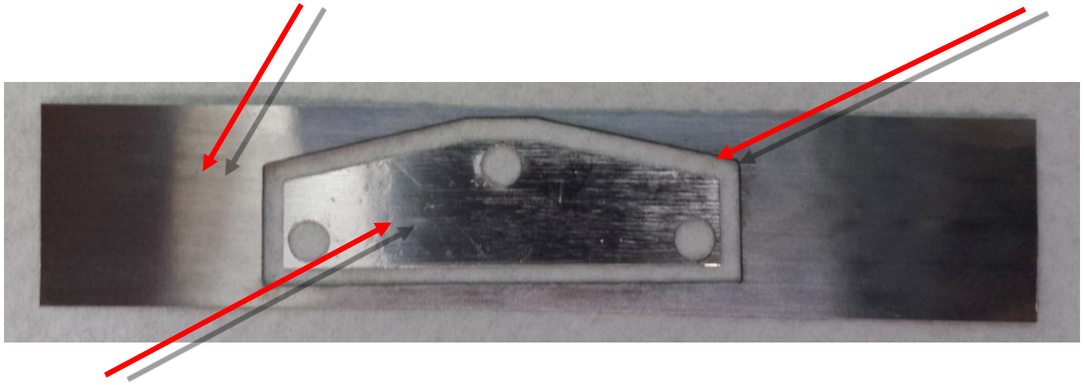
Preform foil soldering technique with frame (with slids)







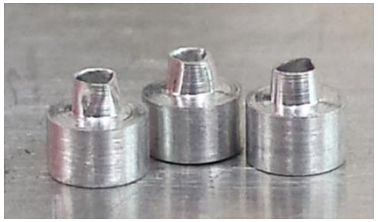
Preform foil soldering technique with frame: components



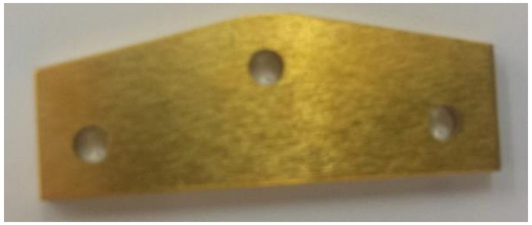
Frame in Stainless Steel 50 µm (laser cut @ CERN)

1mm gap

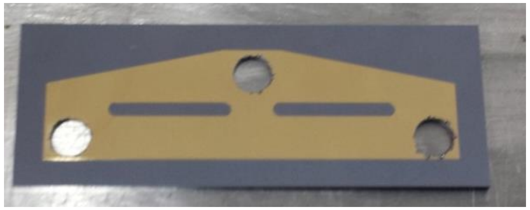
Solder foil 50µm (made in our lab)



Small aluminium “washers” (D=2.46 mm)

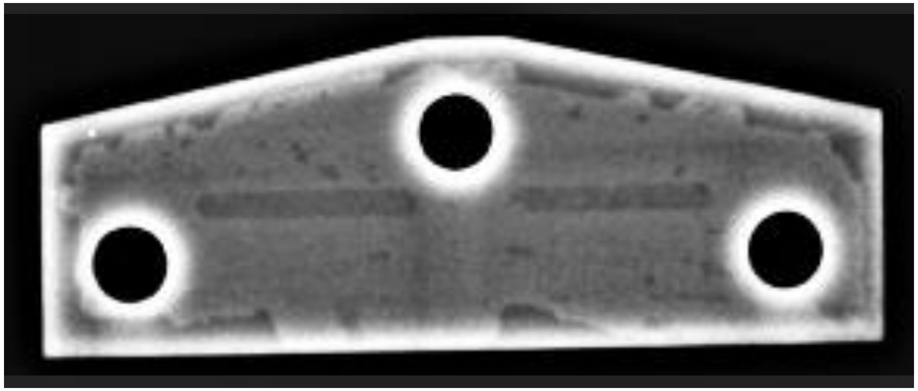


Connector without the slits

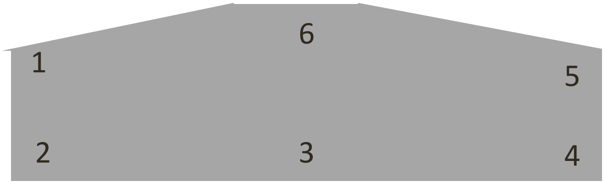


Silicon with the slits pattern on the metallization

Sample 66



Total thickness measurement



1 – 3104 µm
2 – 3105 µm
3 – 3099 µm
4 – 3109 µm
5 – 3108 µm
6 – 3111 µm

Δh = 12 µm

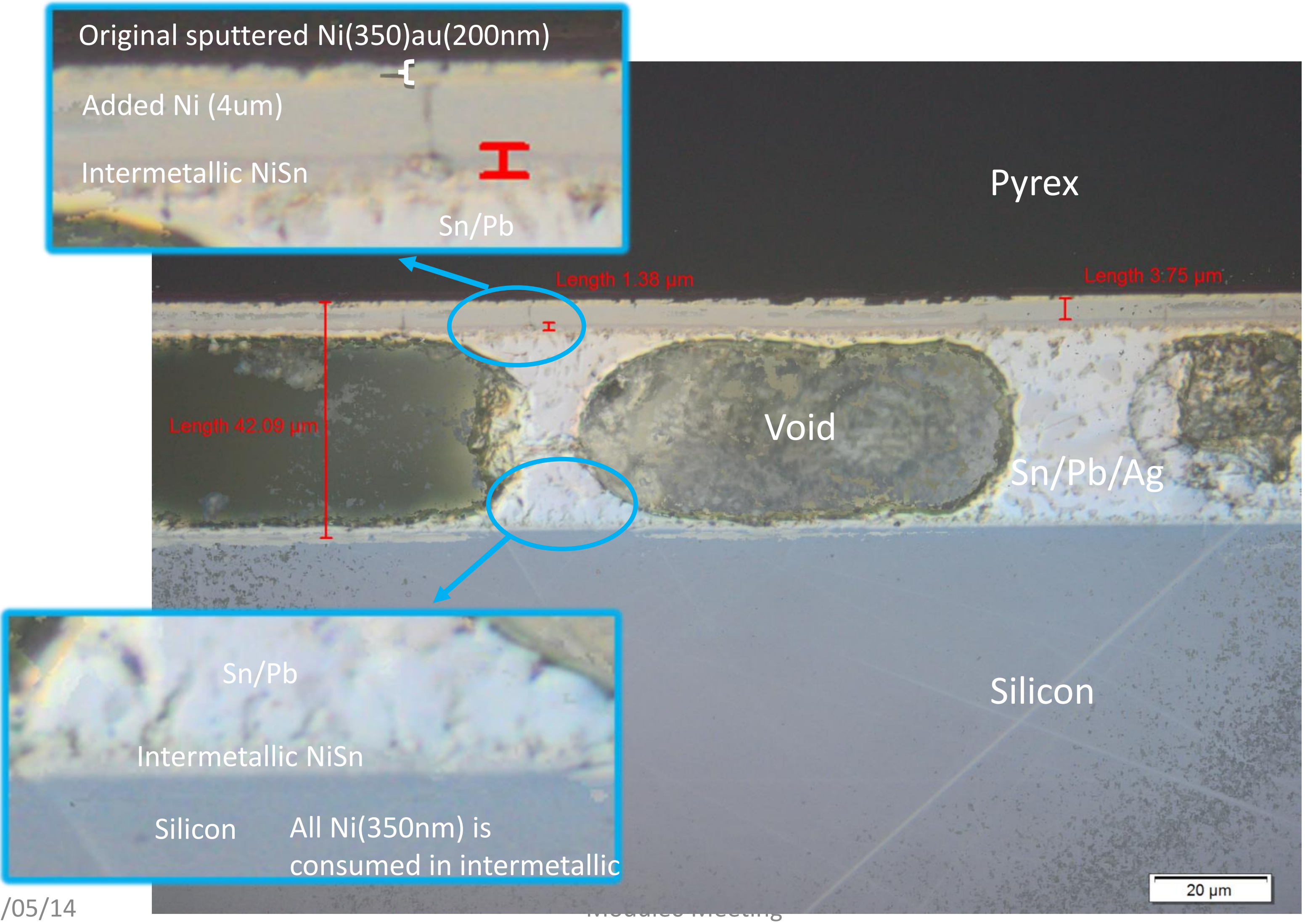
+5µm of Ni on the Si metallization

T_{MAX}=195˚C
TAL = 46.5 s
P = 1.8×10^{-3} mbar

•Solder
  - The solder moved out of the non metallized area (slits).
  - The excess is constrained inside the frame
  - No escape through the holes ("washers")

•Voids
  - Few voids
  - Small (≤ 1 mm)
  - Not interconnected

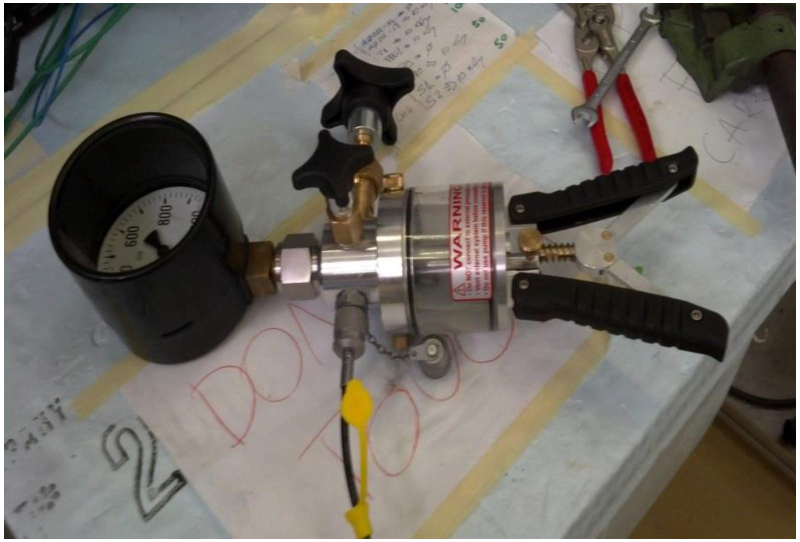
Optical zoom 1000x on void in solder layer



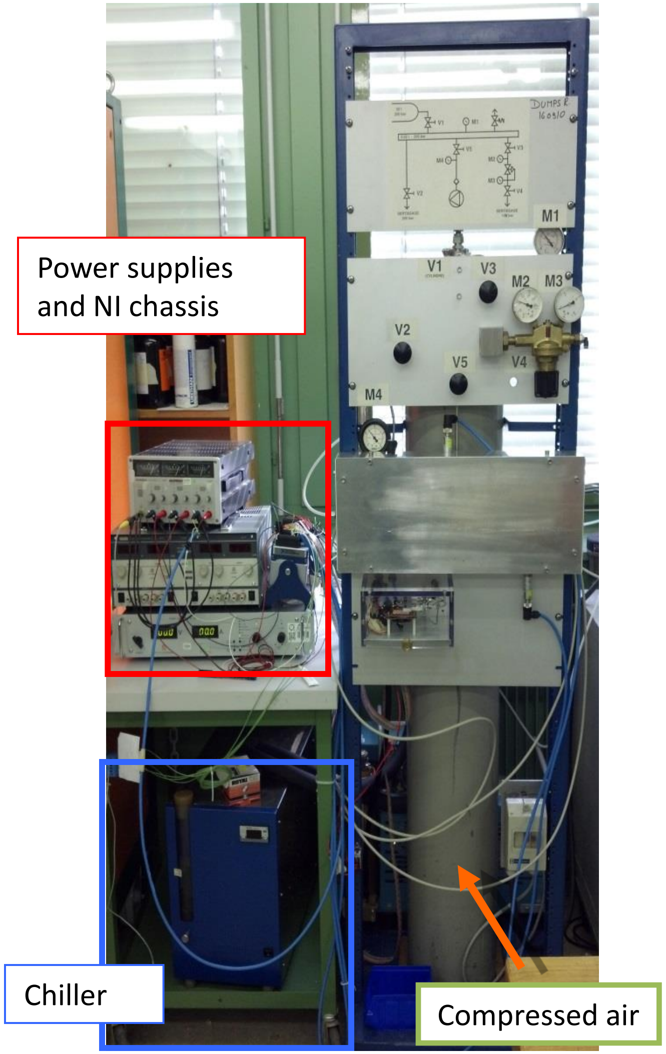
All Ni(350nm) is consumed in intermetallic

Solder leak test

- Leak test performed using water
  - All samples resisted more than 70 bars
  - Exploded with pressures around 80-145 (2 samples)
  - The explosions happened exactly on the slits
  - Is it too wide? New design for the slits?



Stress tests

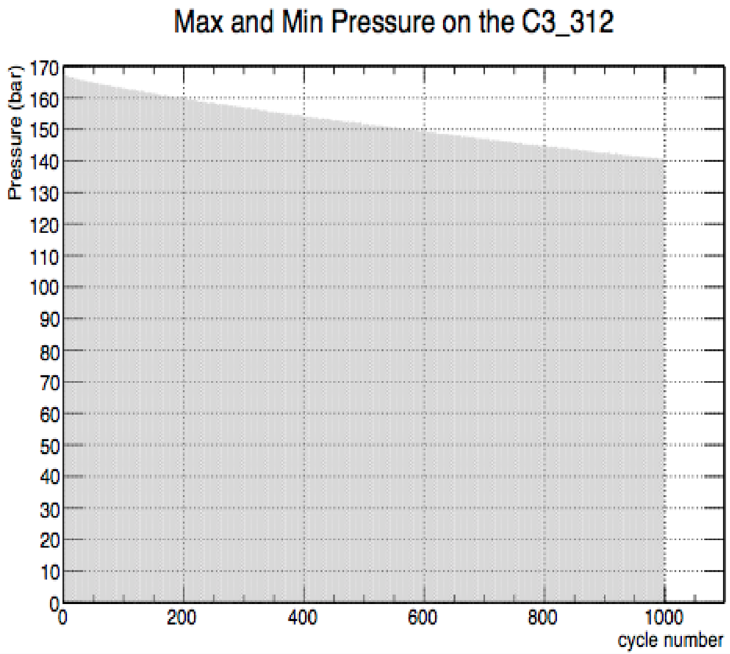

Power supplies and NI chassis

Chiller

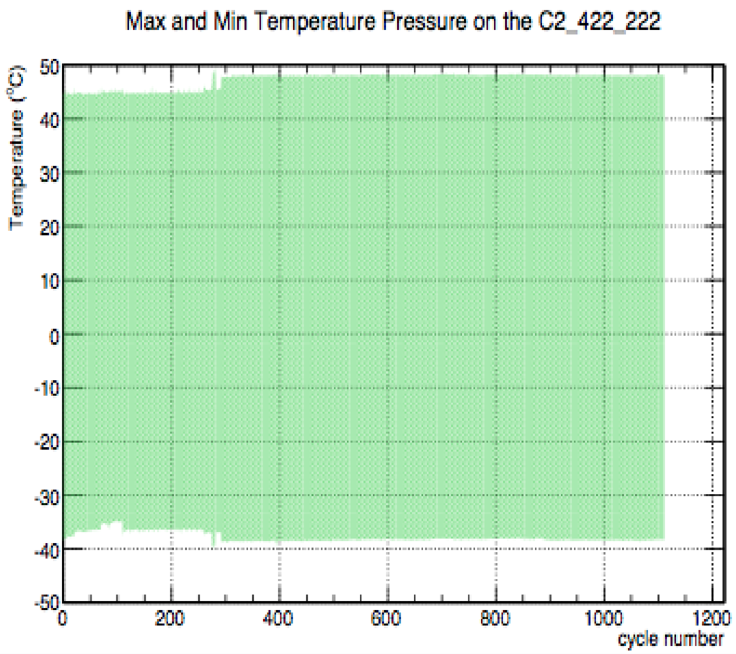
Compressed air

- Perform temperature and pressure cycles:
  - Pressure: 1-200 bars
  - Temperature: -40˚C up to + 40˚C
- Ensure long system life

Stress tests



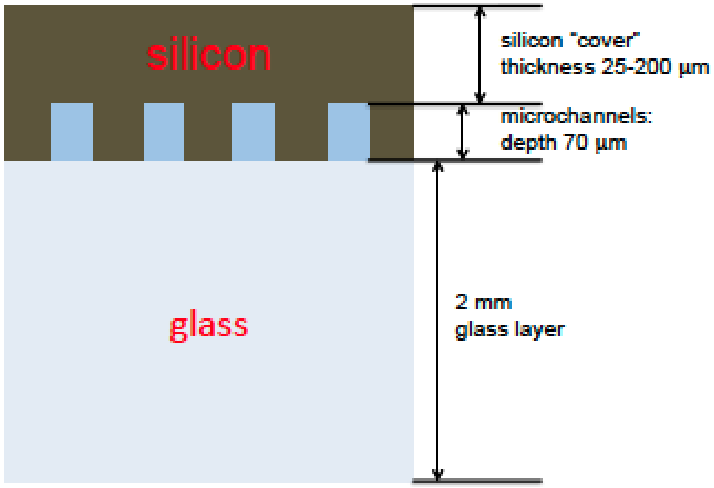
1000 pressure cycles starting at 166 bars.

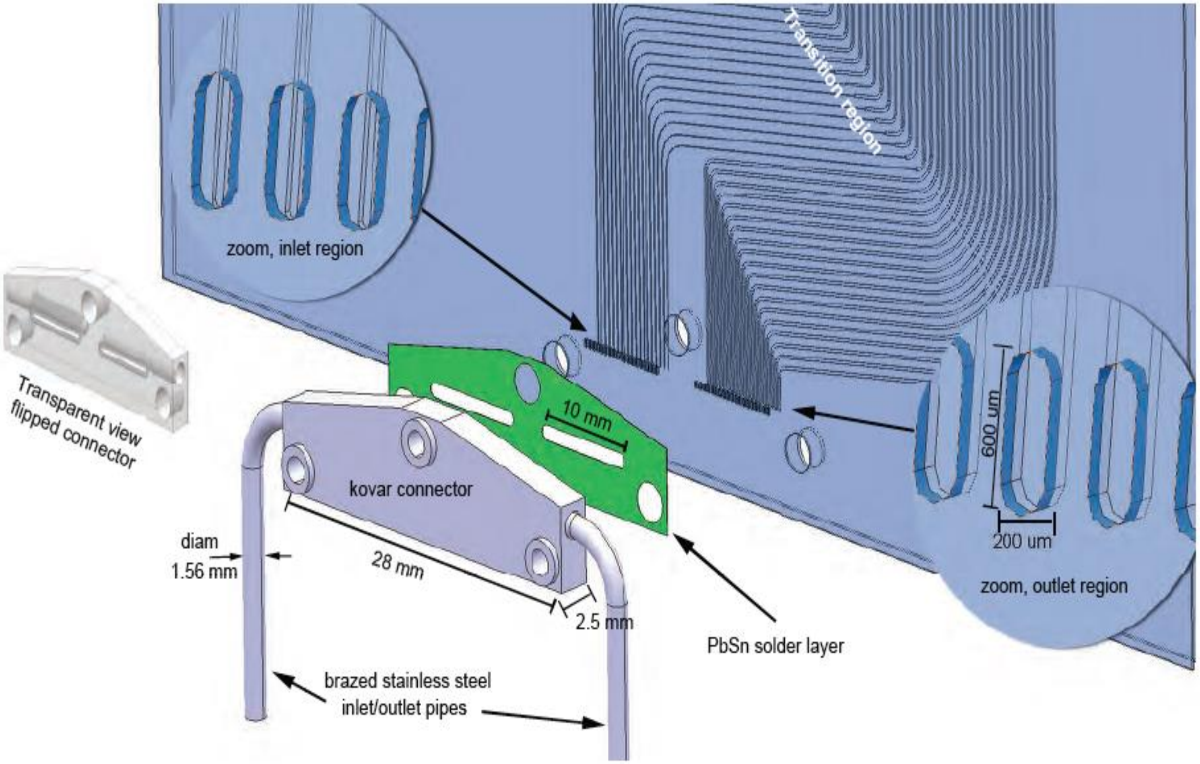


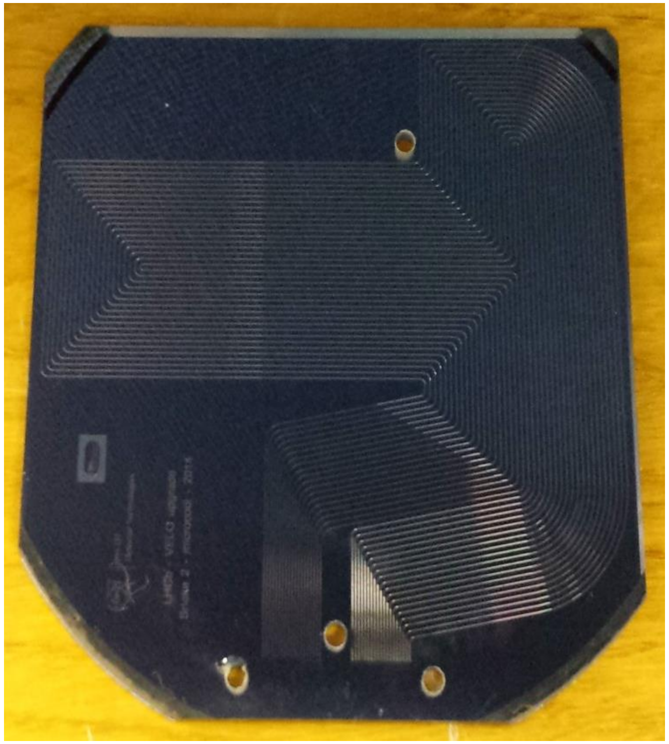
~1100 temperature cycles at low pressure (12 bars)

Thousands temperature and pressure cycles were performed on micro-channels samples without any sign of long term effect

Snake II prototype





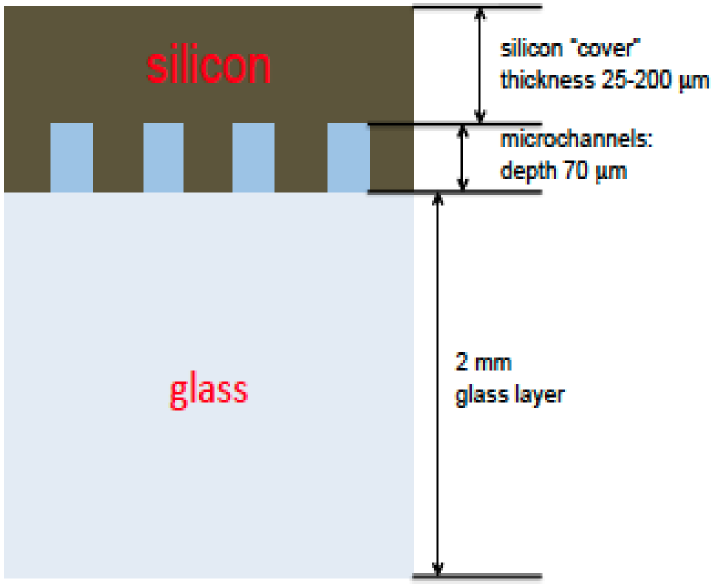


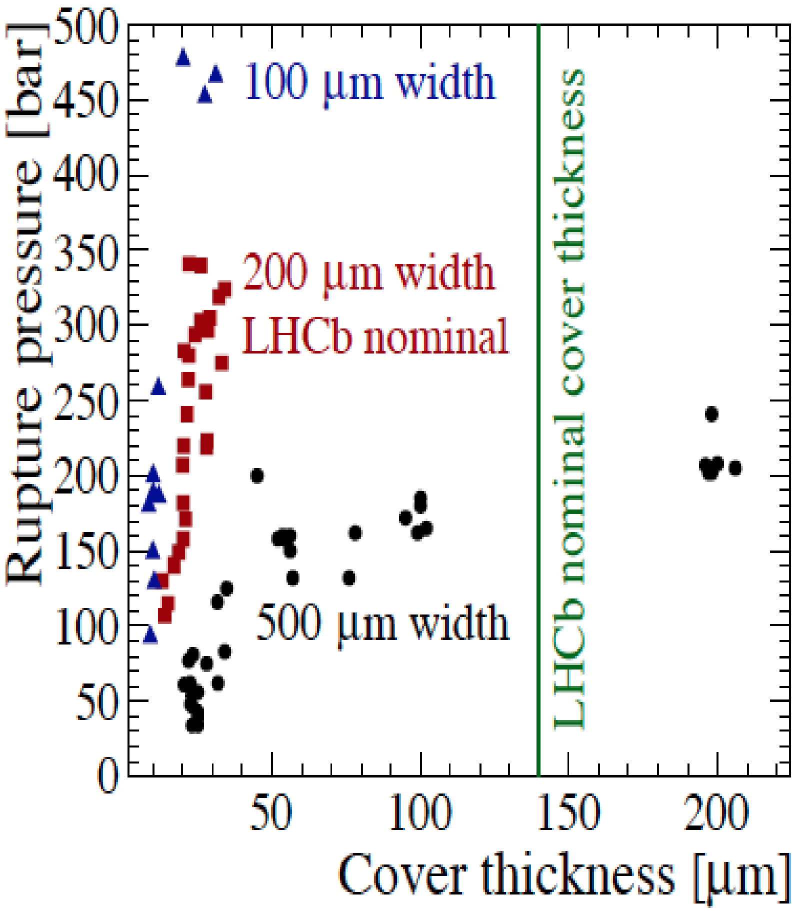
Summary

- LHCb VELO Detector will be built with microchannel cooled pixel modules
- Requirements for VELO are satisfied: material, power density, sensor tip temperature
- Reliability under pressure and temperature cycles
- Current intensive research around the soldering technique to join metal to silicon.
- New Snake II prototype from Lausanne
- More test samples from Southampton around September to be tested in Oxford

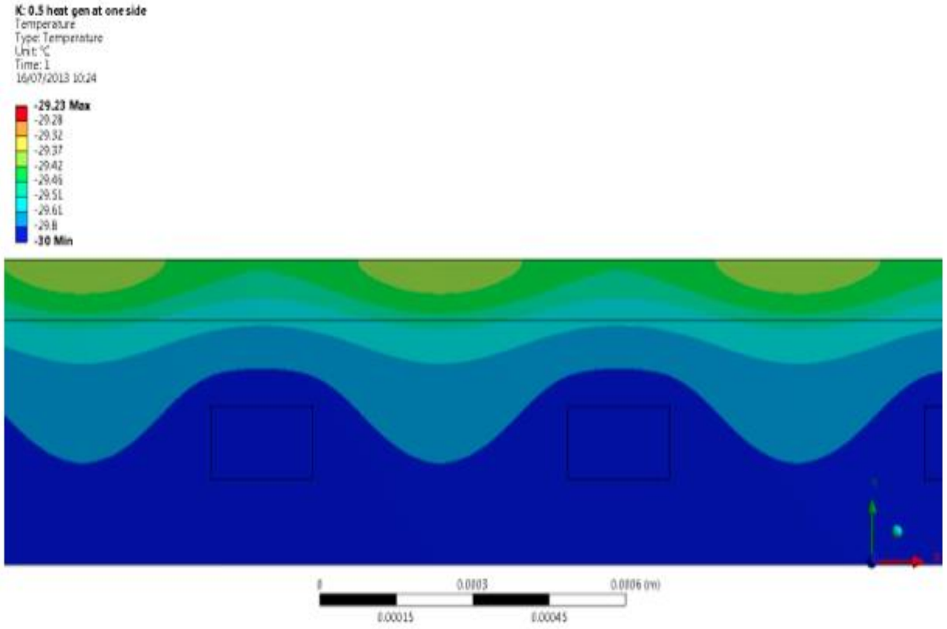
Backup slides

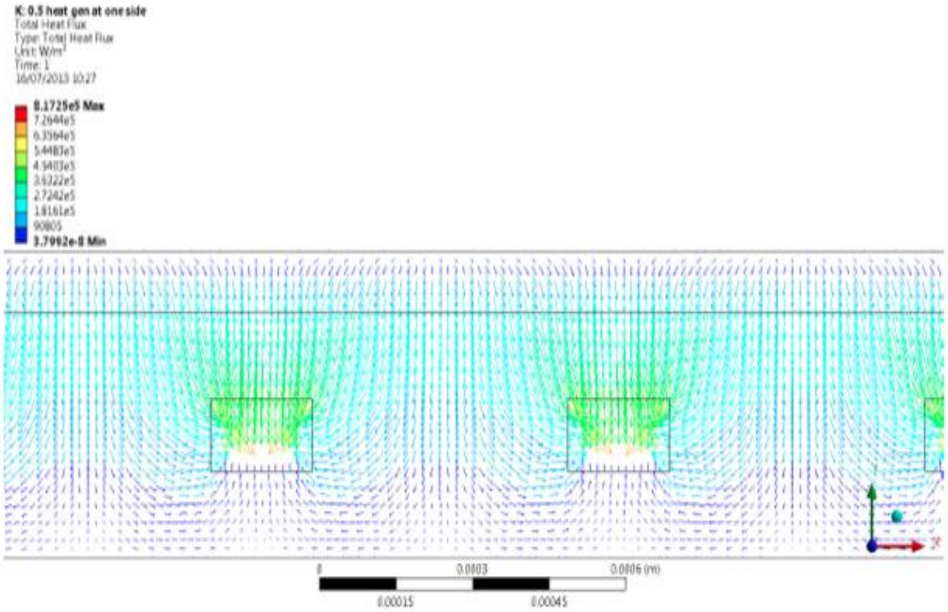
Snake II – Si Thickness





Snake II – channel spacing





Criteria: Maximum ΔT < 1˚C

The heat flow should use most of the silicon substrate

The spacing of 0.5 mm was chosen.

Upgraded VELO (VErtex LOcator)

Function of VELO: provide precise tracking and trigger on displaced vertices

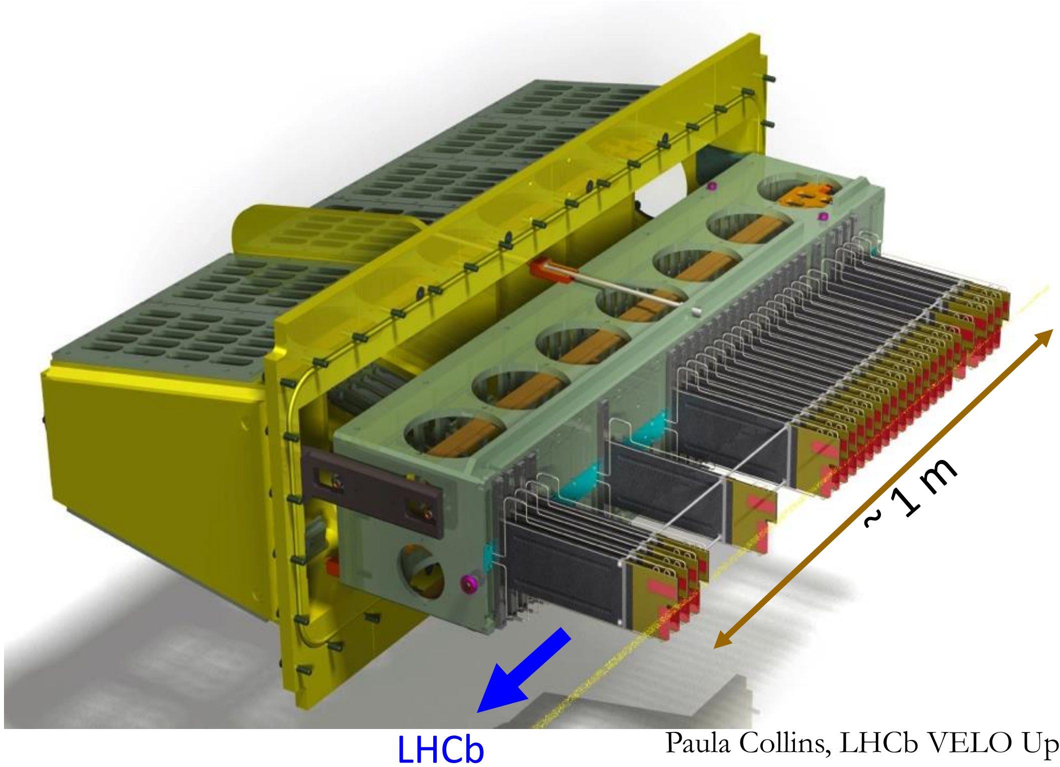
New Pixel detector approved by collaboration on 17th July 2013

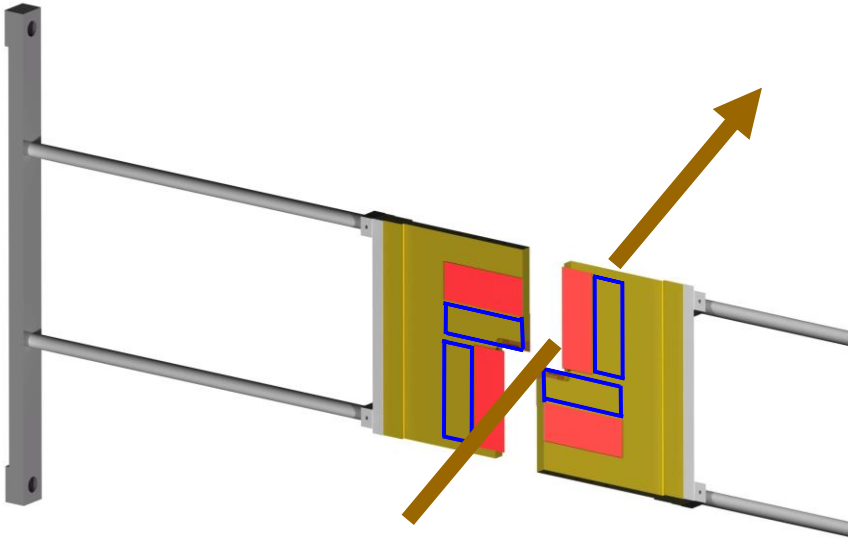
26 stations arranged perpendicularly along the direction of the beam

- varying spacing in beam direction, min. 24 mm between stations
- total active area 1237 cm2 (= size of A3 sheet of paper)

Geometrical efficiency > 99 % for R < 10 mm

- 99 % of tracks from interaction region have 4 or more hits



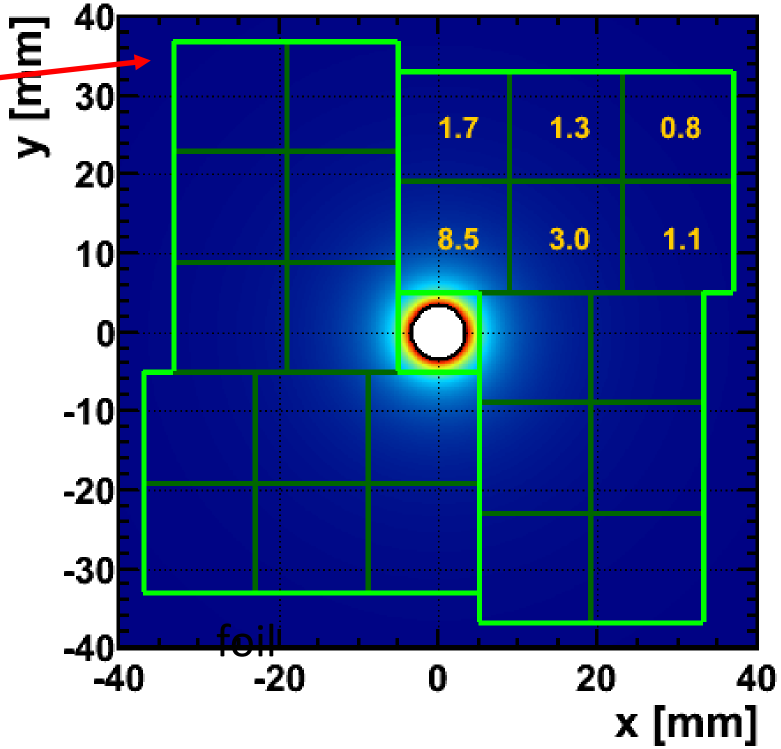


Paula Collins, LHCb VELO Upgrade,
IEEE/MIC 2013

Challenges for upgraded VELO

Radiation Damage

- Highly non-uniform radiation damage of up to 8×10^{15} n_{eq}/cm^2 for 50 fb-1 (= full lifetime super LHC)
- Factor 40 less at sensor outer corner
- Expect ~7nA per pixel and 130 mW per tile
- ASICS must tolerate 400 MRad



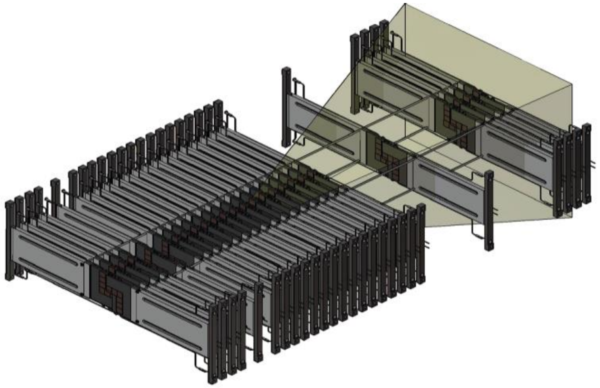
pixel layouts superposed above anticipated flux (arbitary scale)

Enormous Data Rates

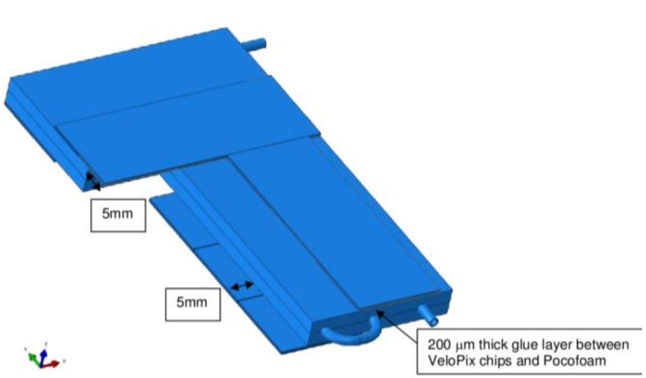
- ~8.5 tracks/collision for hottest ASIC
- Hottest chip 230-320 Mtrack/s
- 600-900 Mhits/s/ chip

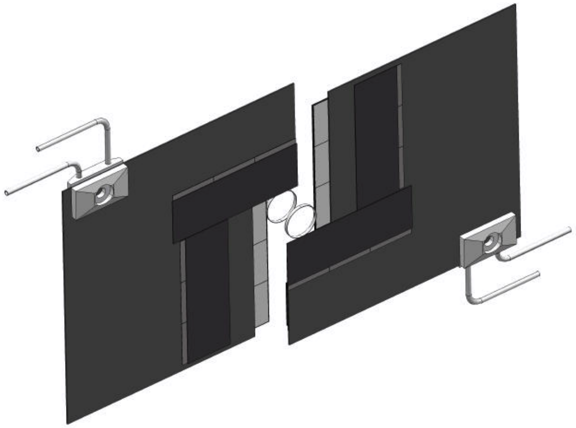
Material Budget (thinning and cooling)

  - Modules are partially in acceptance



Two solutions proposed: Poco-foam and micro-channels





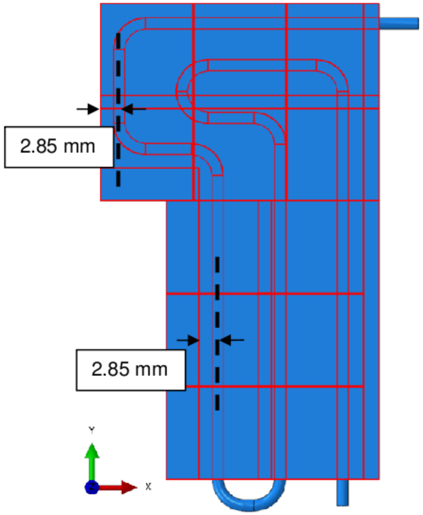
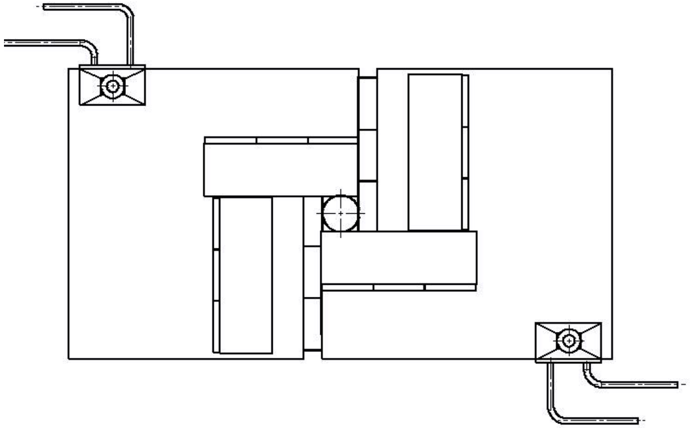


Figure 6. Structure 3, position of the cool pipes



Micro-channel cooling

High speed pixel readout chips produce a lot of heat (~ 1.5 W/cm^{2})

Keep the sensors at < -20 °C to minimize the effects of radiation damage, and to avoid thermal runaway

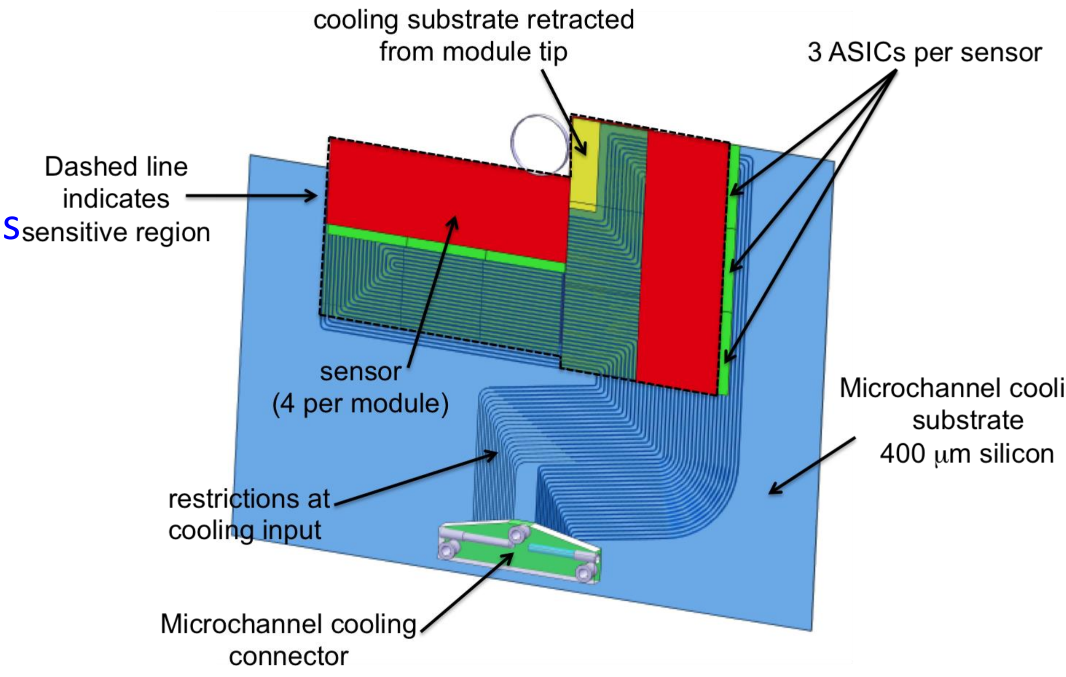
Bring the cooling power where you need it, using least material

Novel method: evaporate CO_2 via micro-channels etched in Si substrate

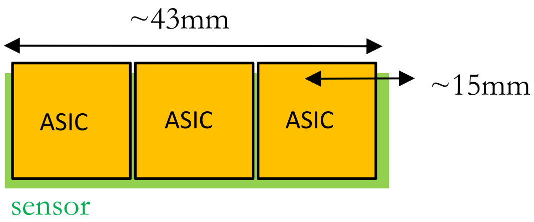
Additional advantages:

no CTE difference (Si on Si)

very good uniformity of material in sensitive region



VELO module



Sensor tiles: 3 readout VeloPix ASICs on a sensor:

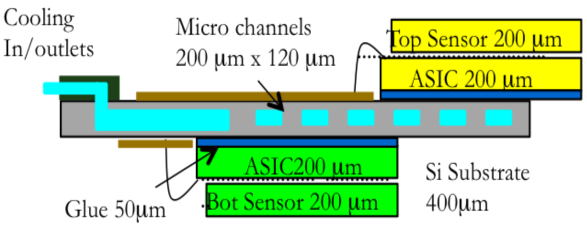
  - 55 x 55 μm^2 pixels
  - elongated pixels between ASICs
  - ~450 μm guard ring

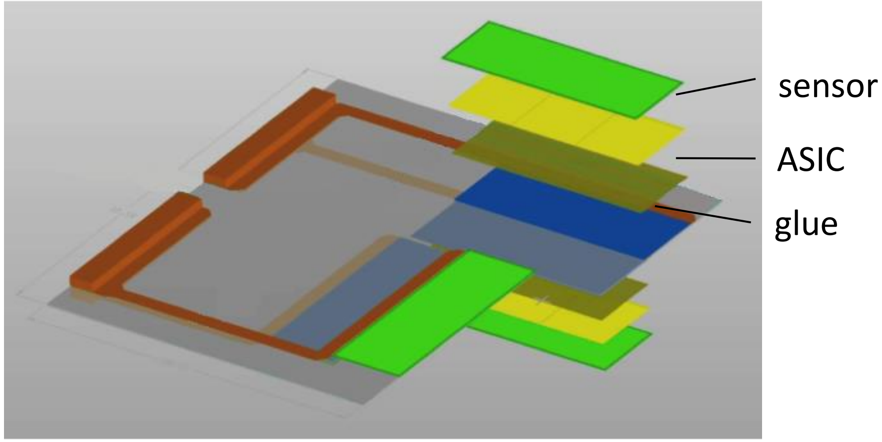
4 sensor tiles, 2 on each side of substrate

  - power and readout traces on kapton circuit board

Whole VELO ~41 Mpixels

- Silicon substrate with integrated micro-channels for cooling
- Material in active region ~ 0.8 % X_0





Why CO_2 evaporative cooling in silicon micro-channels?

- Silicon micro-channels
  - Cooling is under the heat source
  - Low mass – The substrate is also the cooling
  - No mismatch of expansion coefficients

- CO_2
  - High latent heat
  - Low viscosity
  - Not toxic
  - Inert gas
  - Cheap
  - Radiation hard

Micro channel cooling II

Channel dimensions 200 x 120 μm^2

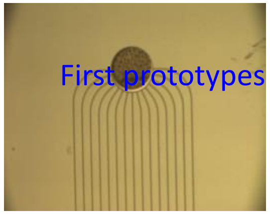
Operational Pressure ~15 Bar at -30 °C, and ~60 Bar at room temp.

Including safety limits it has to withstand > 150 Bar

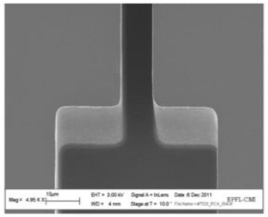
Samples with hydrophobic bonding withstand > 700 Bar

Thermal and pressure cycling tests (-40 .. +40 °C, 0 .. 200 Bar) ongoing

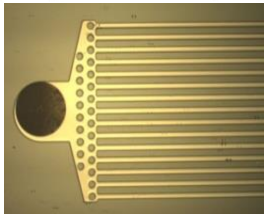
Inlet hole
(Ø 2mm)



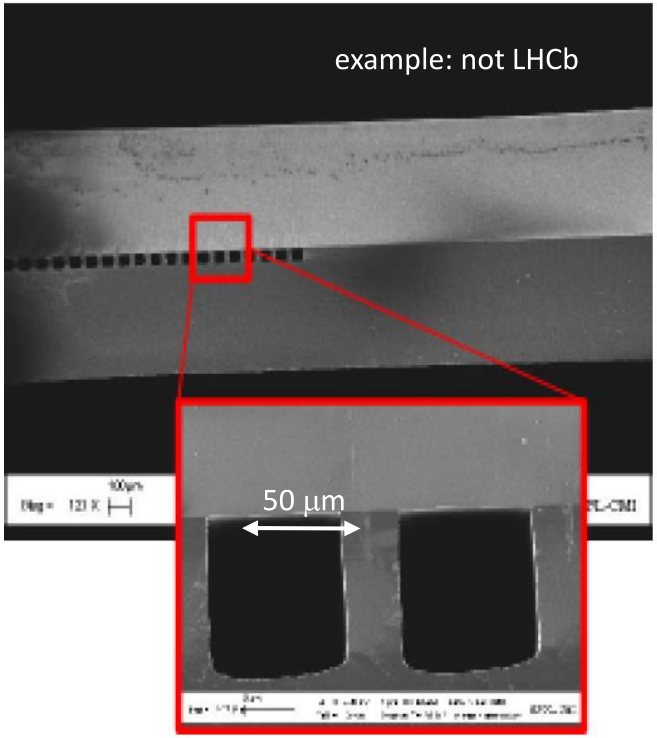
Transition from input restrictions
(60 um width) to cooling channel
(200µm).



Output manifold
with "pillars"



First prototypes (early2012)



example: not LHCb