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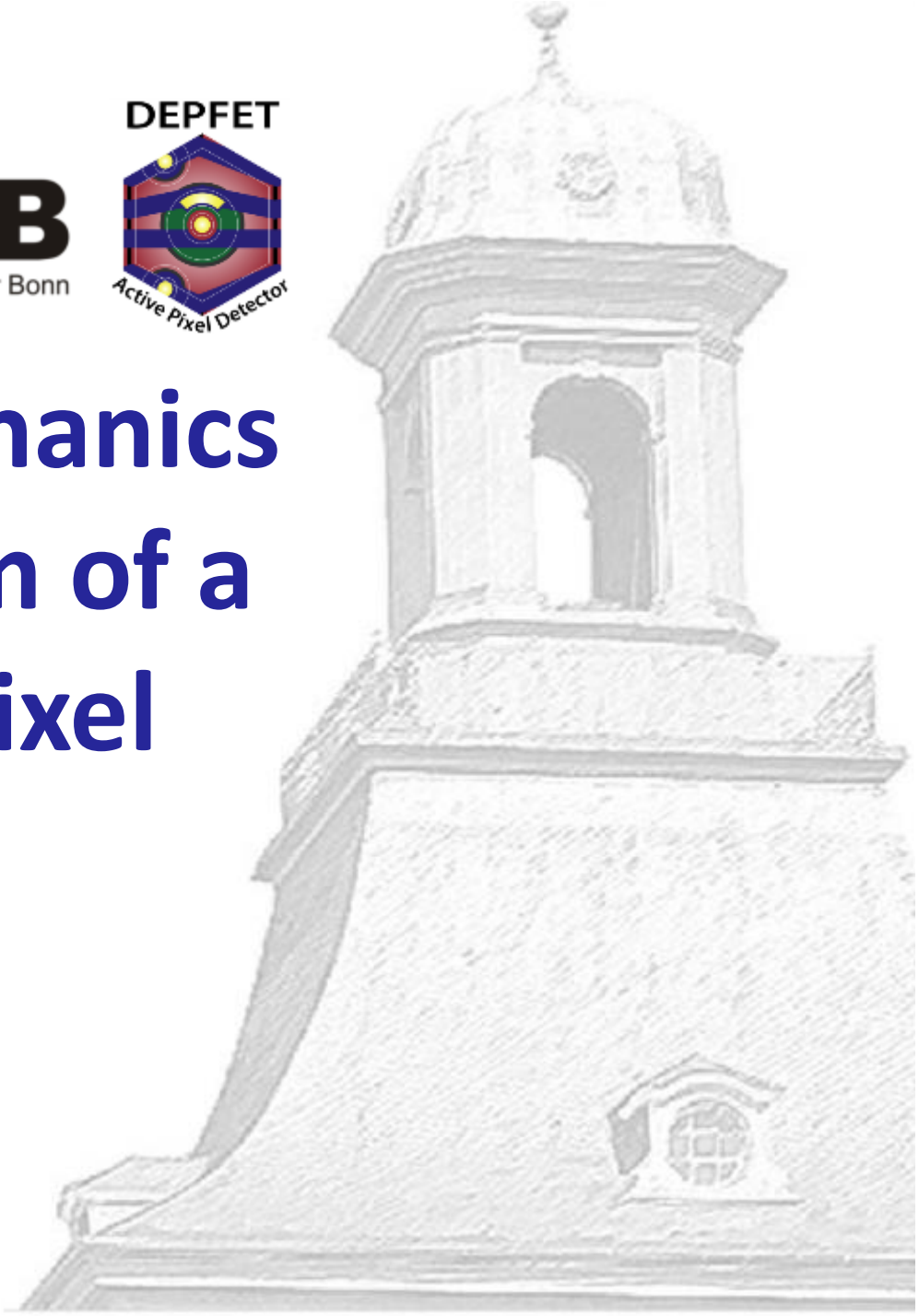
SI LAB Silizium Labor Bonn

DEPFET Active Pixel Detector

The ultralight mechanics and cooling system of a DEPFET-based pixel detector

C. Marinas
University of Bonn

DEPFET Collaboration



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Outline

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- Vertexing requirements in future colliders
  - SuperKEKB and ILC
- Belle II vertex detector
  - Mechanics and cooling
- ILC specific developments
  - Forward petals
  - Power pulsing
  - Micro-channel cooling

Future Vertex Detectors

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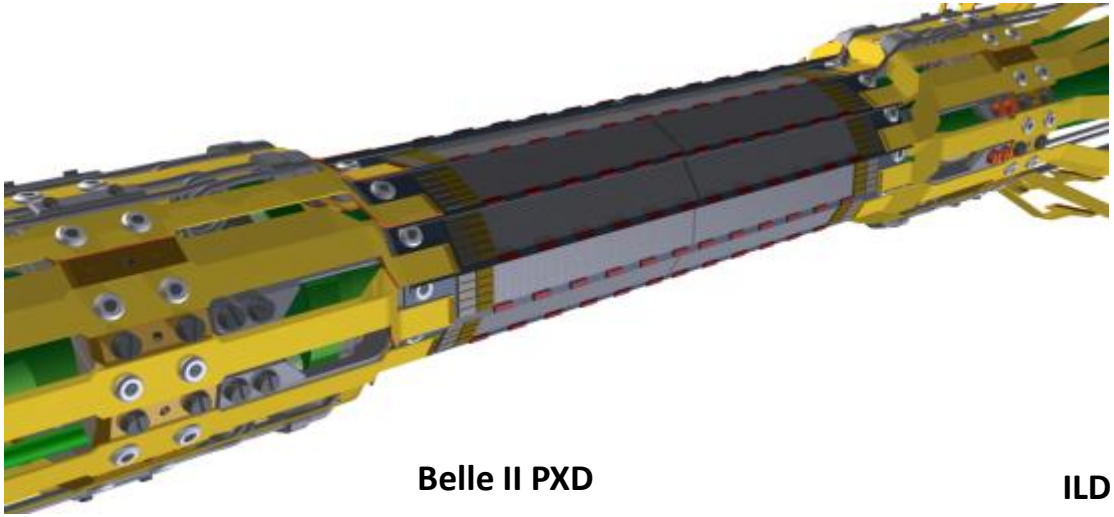
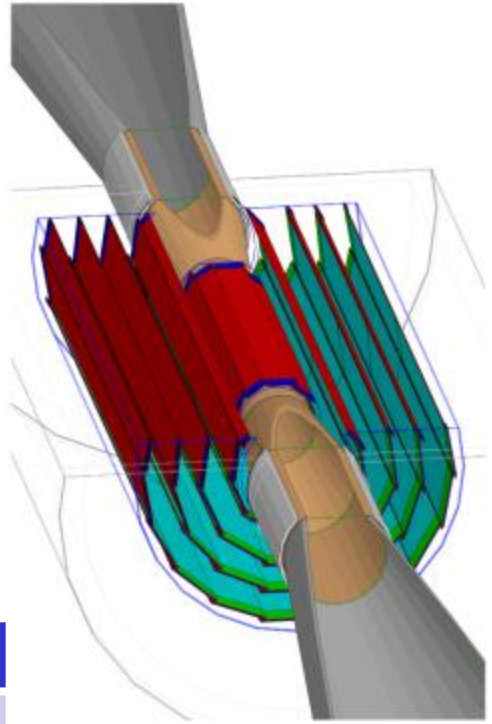
The Belle II Collaboration decided on DEPFET as baseline for the pixel detector



Belle II PXD



ILD 5-layer VXD

	Belle II	ILD LOI 5-layer layout	
Radii	14, 22	15, 26, 38, 49, 60	mm
Ladder length	90 (L1), 122 (L2)	123 (L1), 250 (L2-L5)	mm
Sensitive width	12.5 (L1-L2)	13 (L1), 22 (L2-L5)	mm
Number of ladders	8, 12	8, 8, 12, 16, 20	
Pixel size	50x50 (L1), 50x75 (L2)	25x25 (L1-L5)	μm^2

The Belle II PXD DEPFET ladders: *almost* prototypes for L1 and L2 of ILD

ILC Detector Concepts and Belle II

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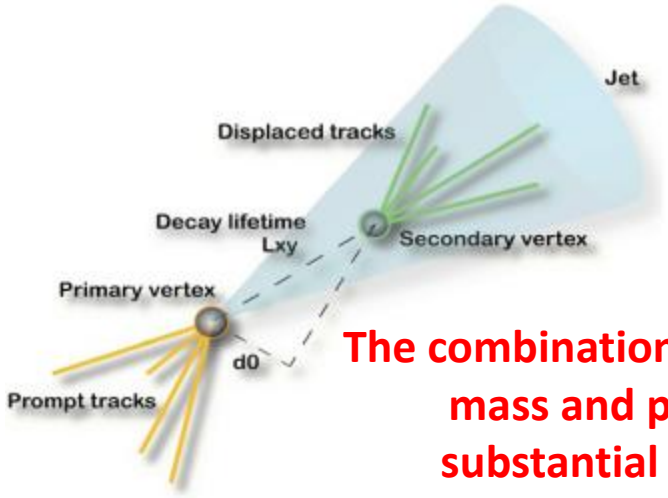
	Belle II	ILC
Occupancy	0.4 hits/μm^2/s	0.13 hits/μm^2/s
Radiation	2 Mrad/year	< 100 krad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year	10^{11} 1 MeV n_{eq} per year
Duty cycle	**1**	**1/200**
Frame time	20 μs	25-100 μs
Momentum range	Low momentum (< 1 GeV)	All momenta
Acceptance	**17°-155°**	**6°-174°**
Material budget	**0.21% X_0 per layer**	**0.12% X_0 per layer**
Resolution	15 μm (50x75 μm^2)	5 μm (20x20 μm^2)

- Lowest possible material budget
  - Ultra-transparent detectors
  - Low power dissipation
  - Lightweight mechanics and minimal services

Vertexing Requirements HEP



$$\sigma_{d0} \approx \sqrt{\frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}} \oplus \frac{r}{p \sin^{\frac{3}{2}} \theta} 13.6MeV \sqrt{\frac{x}{X_0}}$$

$$\sigma_{d0} \approx a \oplus \frac{b}{p \sin^{\frac{3}{2}} \theta}$$

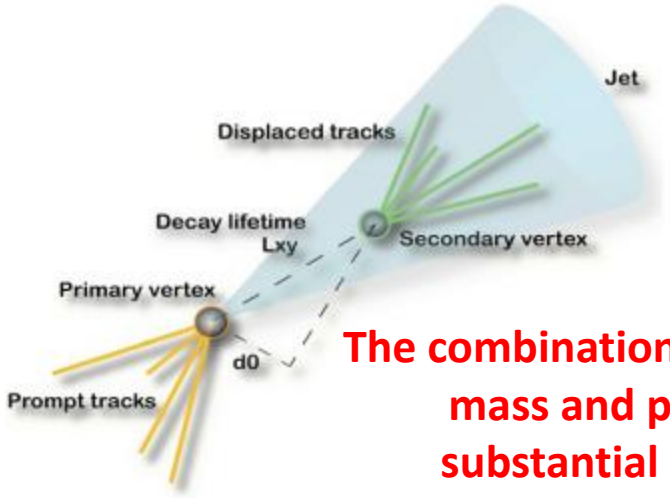
The combination of resolution, mass and power is a substantial challenge

	a (μm)	b (μm GeV)
LHC	12	70
STAR	12	19
Belle II	8.5	10
ILC	5	10

a: Governs high momentum
b: Dominates at low momentum

- Common vertex detector requirements
  - First layer close to the IP
  - Low material budget
    - Reduced services
    - Low power dissipation
  - High granularity
    - Good spatial resolution
  - Fast readout
  - Radiation hardness

Vertexing Requirements HEP



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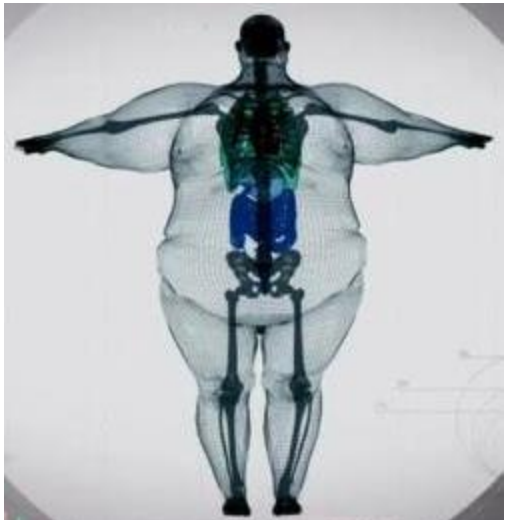

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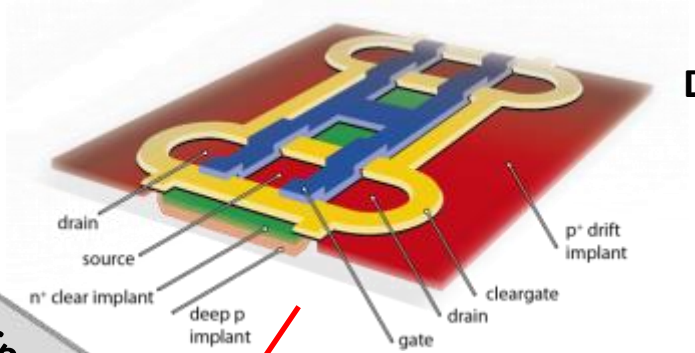
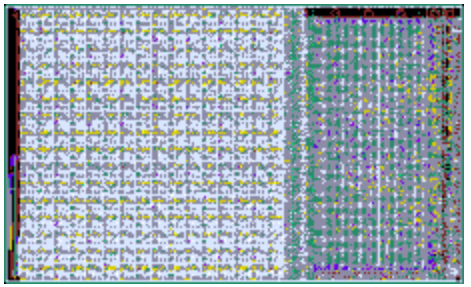
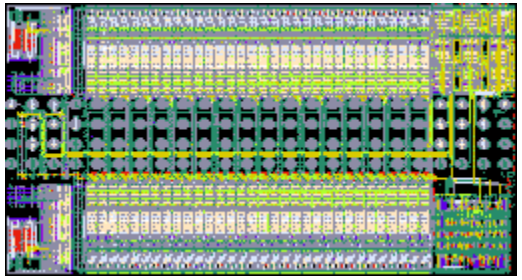
The DEPFET Ladder



DCDB (Drain Current Digitizer)
Analog frontend



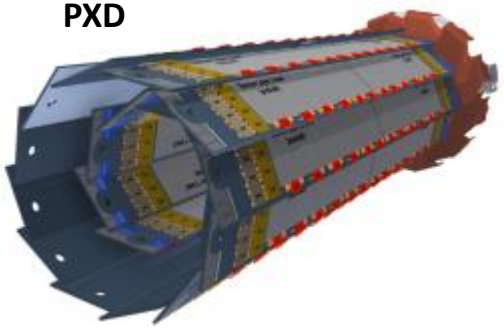
SwitcherB
Row control



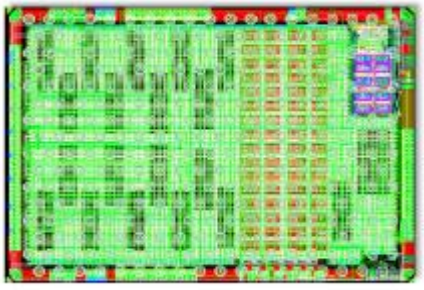
AMS/IBM HVCMOS 180 nm
Size 3.6 × 1.5 mm²
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

UMC 180 nm
Size 5.0 × 3.2 mm²
TIA and ADC
Pedestal compensation
Rad. Hard proved (20 Mrad)

PXD



DHP (Data Handling Processor)
First data compression



TSMC 65 nm
Size 4.0 × 3.2 mm²
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

Thin DEPFET Sensors

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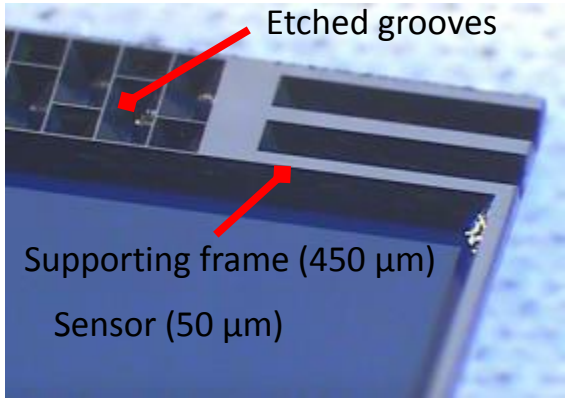
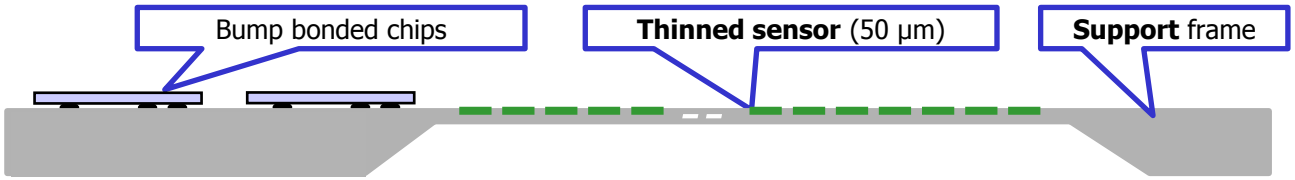
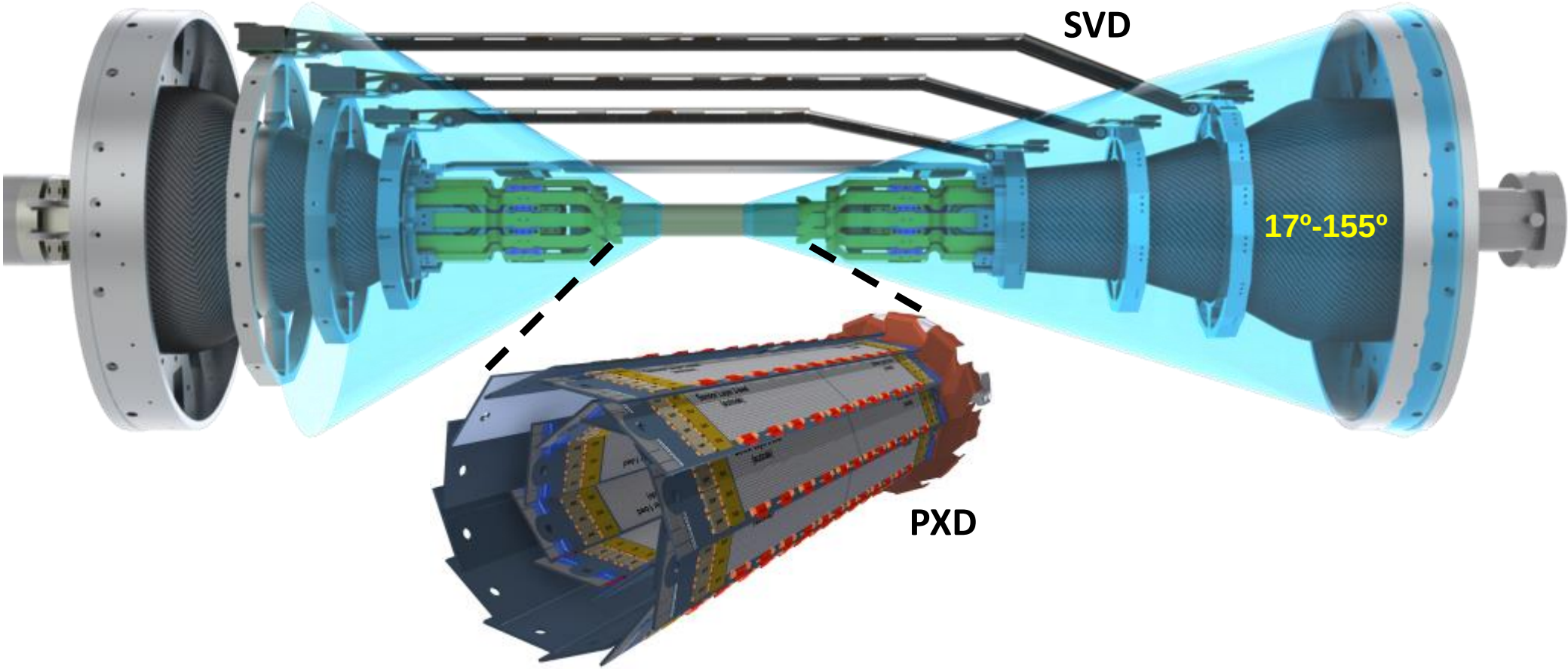
Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor

- One material: uniform and small thermal expansion
- The DEPFET thickness is a free adjustable parameter



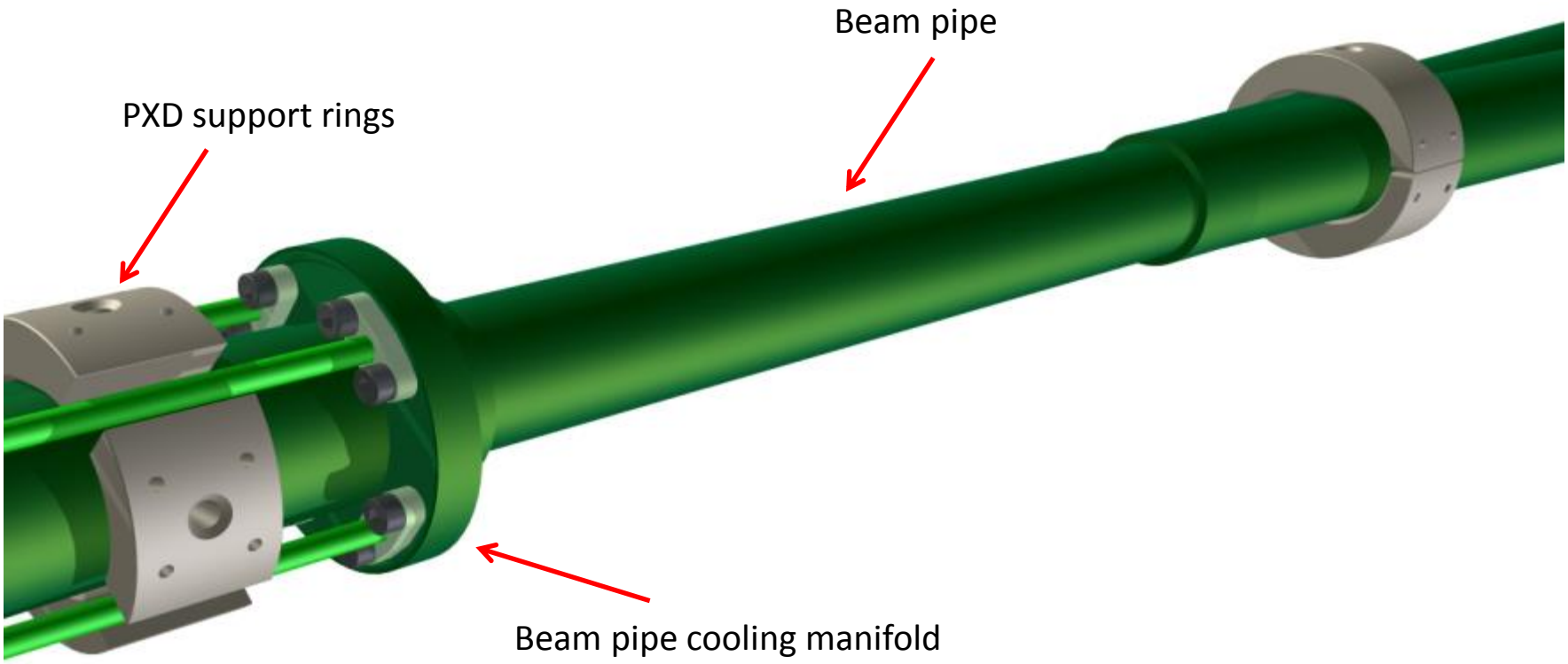


Belle II Cooling Strategy



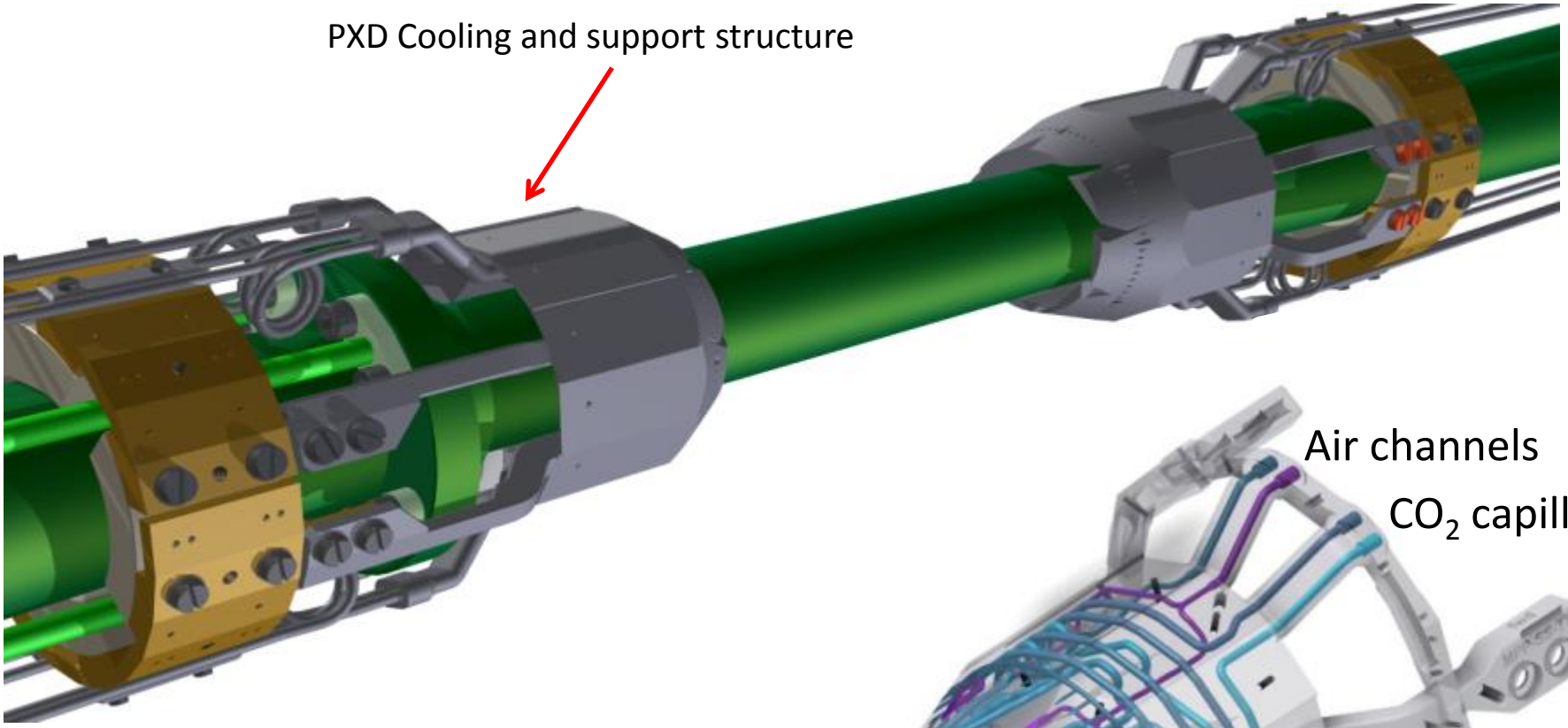
- The material budget must be minimal, no active cooling is allowed inside the acceptance
- The most straightforward solution:
  - Massive structures outside the acceptance to cool down the readout chips
  - The center of the ladder must be cooled using cold air

Building the Belle II PXD



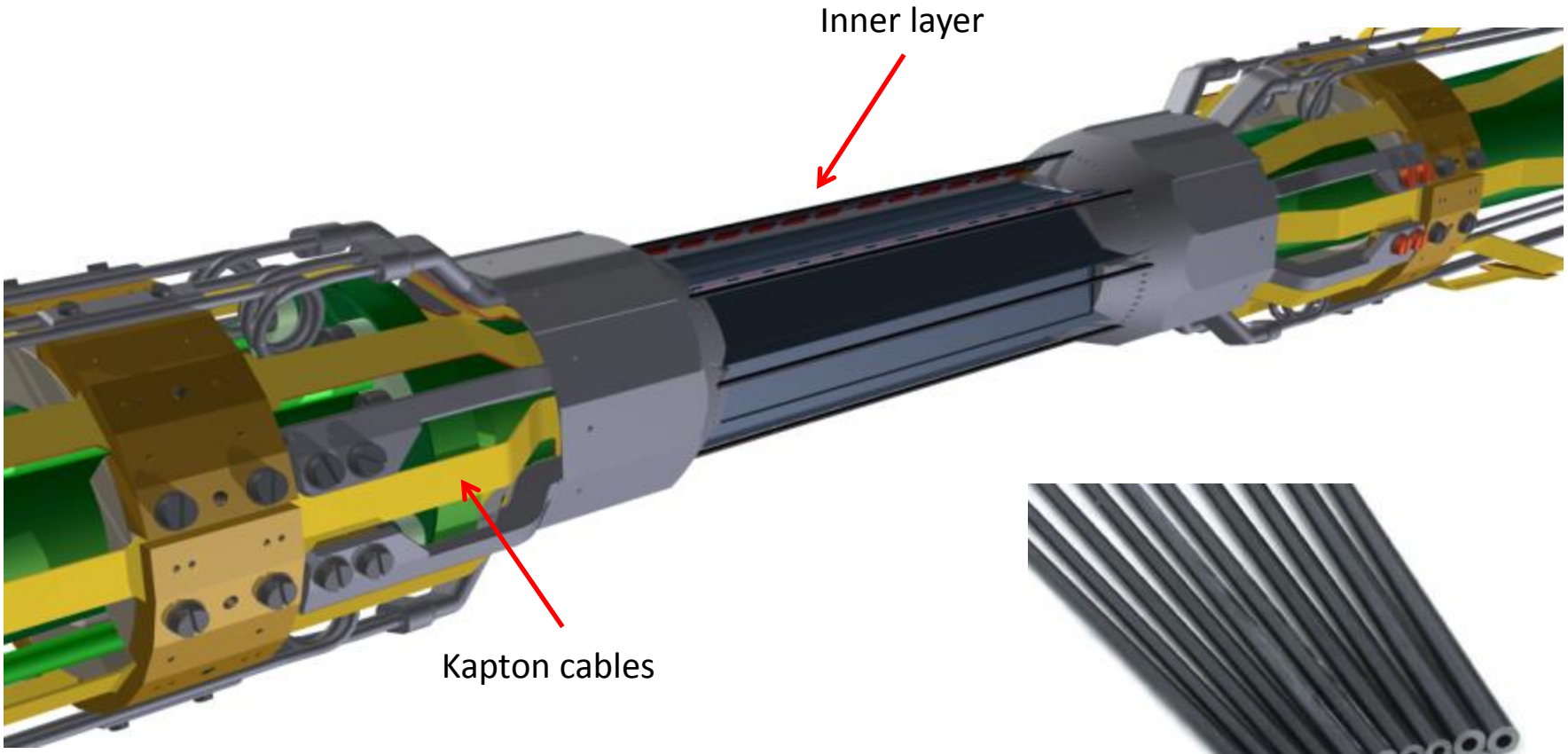
- Thinner pipe
- Smaller radius
- Lighter materials

Building the Belle II PXD



- Stainless steel
- Fast sintering
- Coolant: CO_2

Building the Belle II PXD



Inner layer close to the IP (14 mm)

Additional carbon fibers capillaries to cool the Switchers

Building the Belle II PXD

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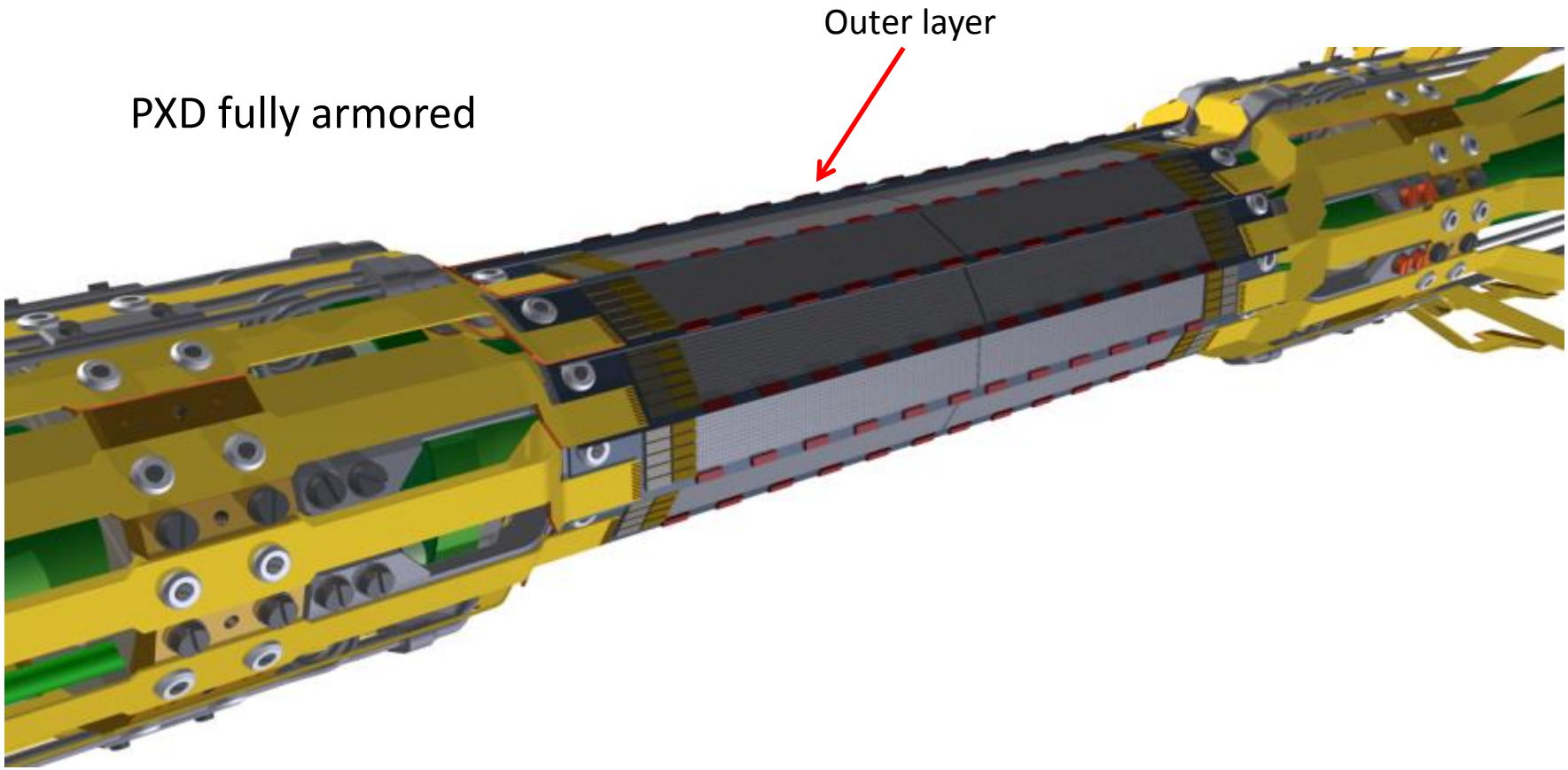
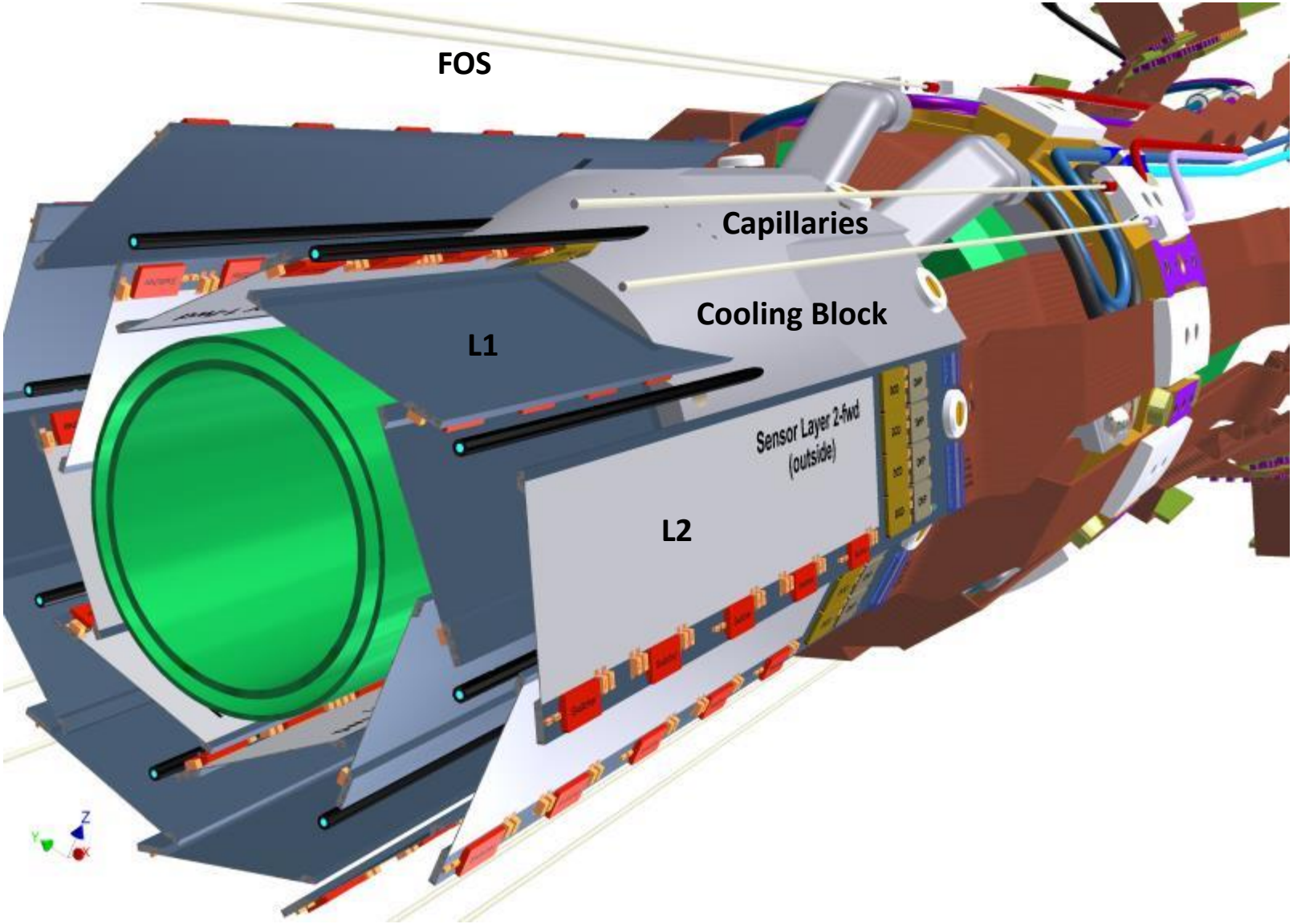
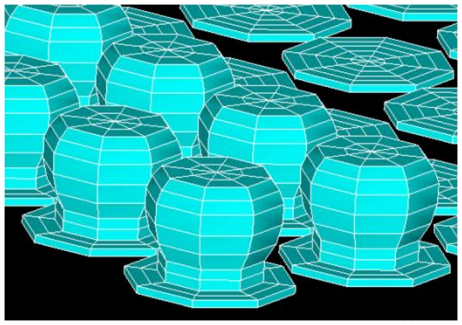


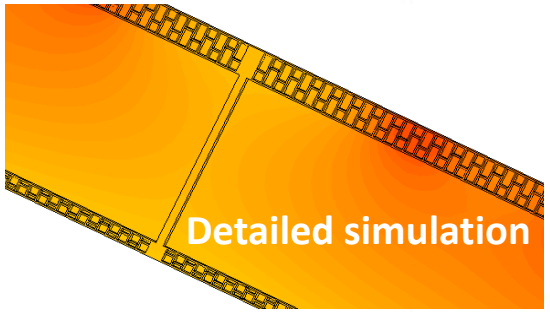
- Low material budget cooling
  - Massive structures outside the acceptance to cool down the readout chips
  - The center of the ladder rely on cold air

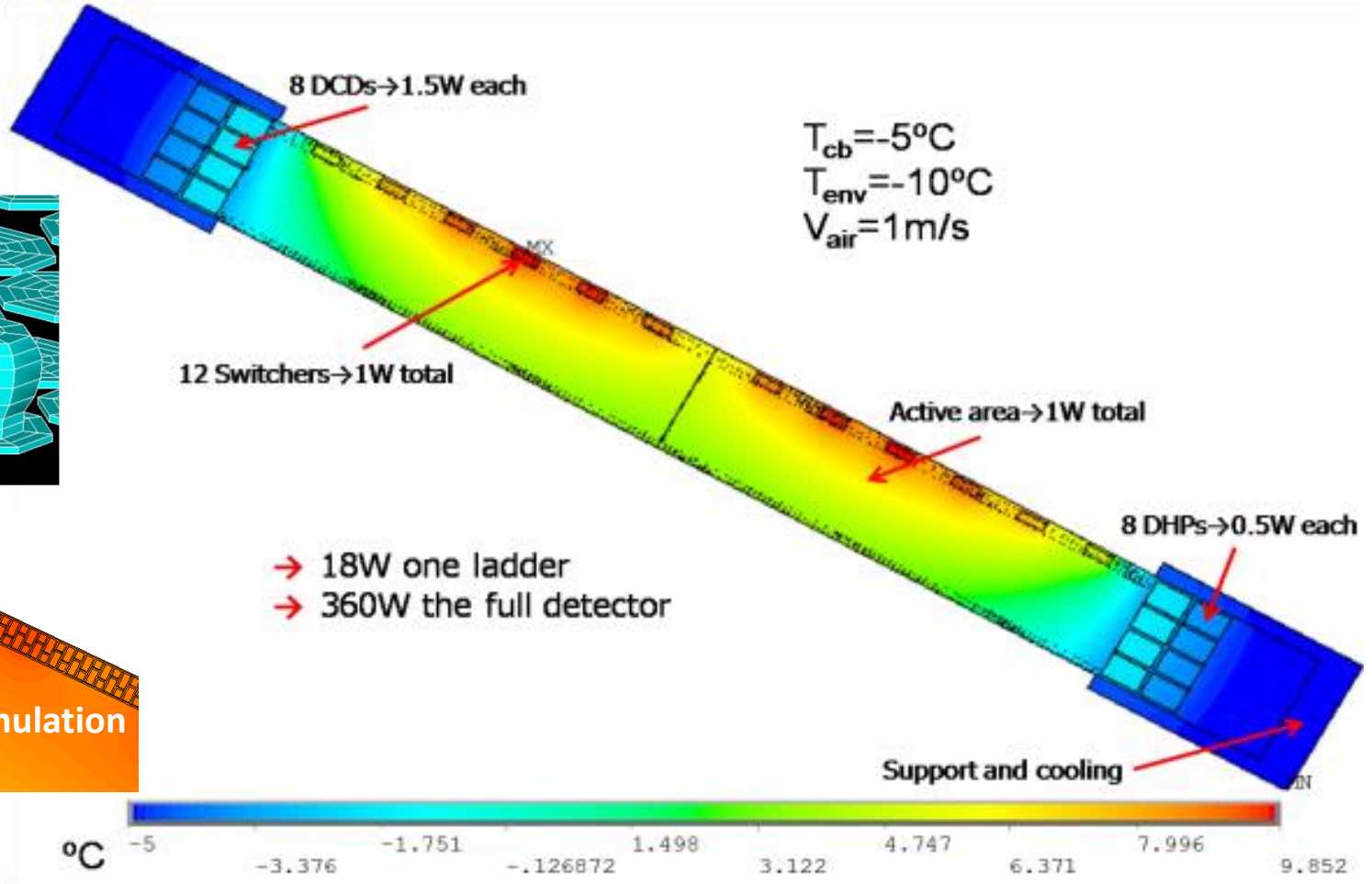
Exploded View



Thermal Simulations





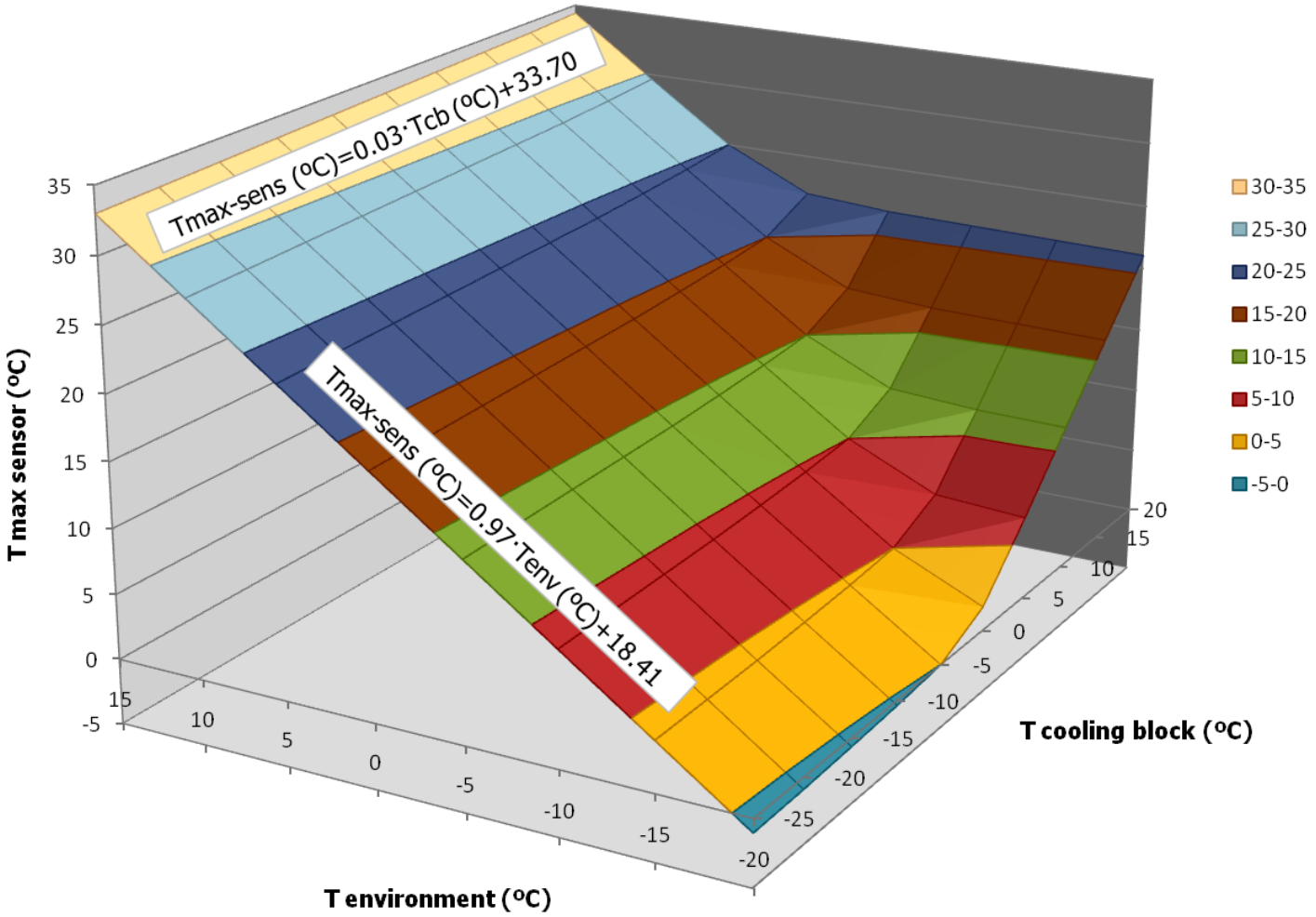


- Find an optimal cooling solution (T_{env} and T_{cb}) such that:

T_{max} (Sensor)<30ºC

T_{max} (Chips)<60ºC

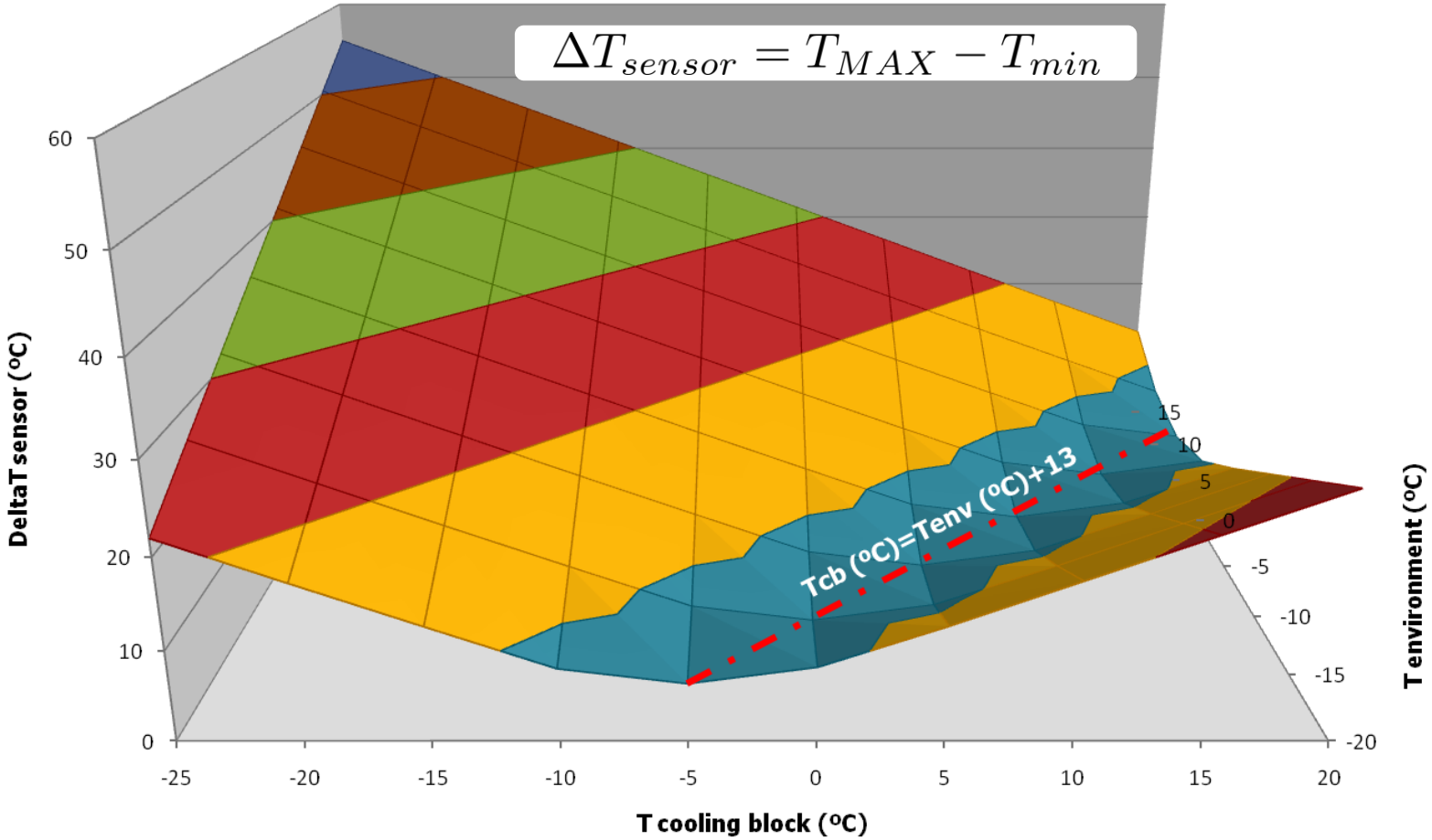
Working Point



• According to these simulations, one can choose whichever combinations for the environment and cooling block temperatures within these ranges

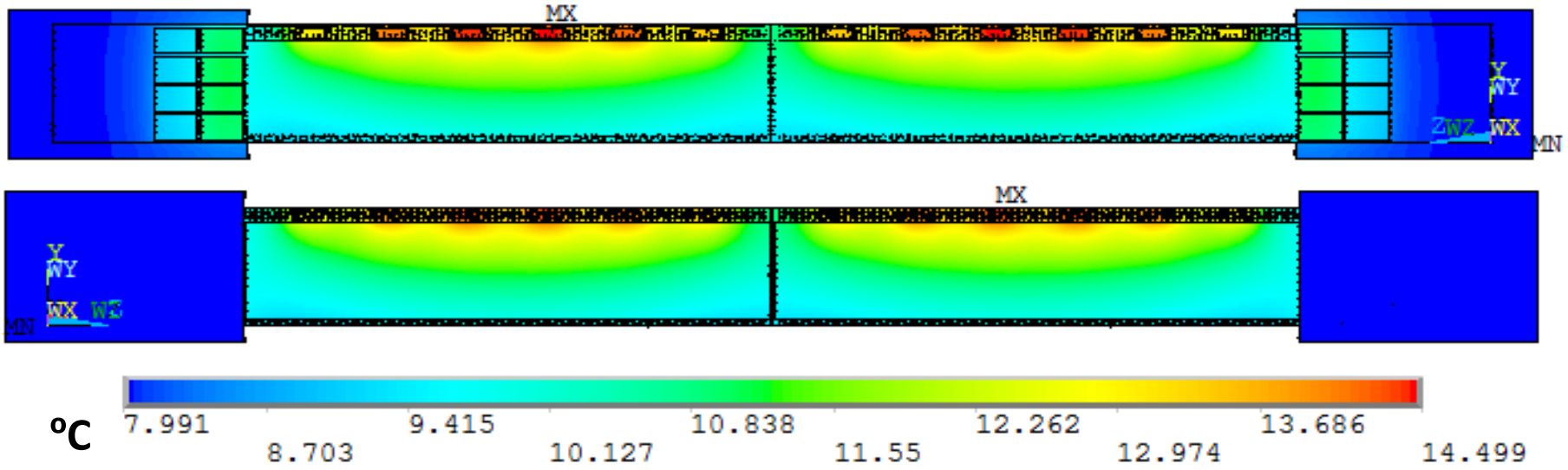
Additional Constraint

- The new reference to decide the temperatures to be applied is:



- In order to keep the DeltaT$_{Sensor}$ minimal, T$_{env}$-T$_{cb}$ are not free parameters anymore
  - Uniform sensor response
  - Avoid thermal stress (CTE mismatch)

Temperature Distribution



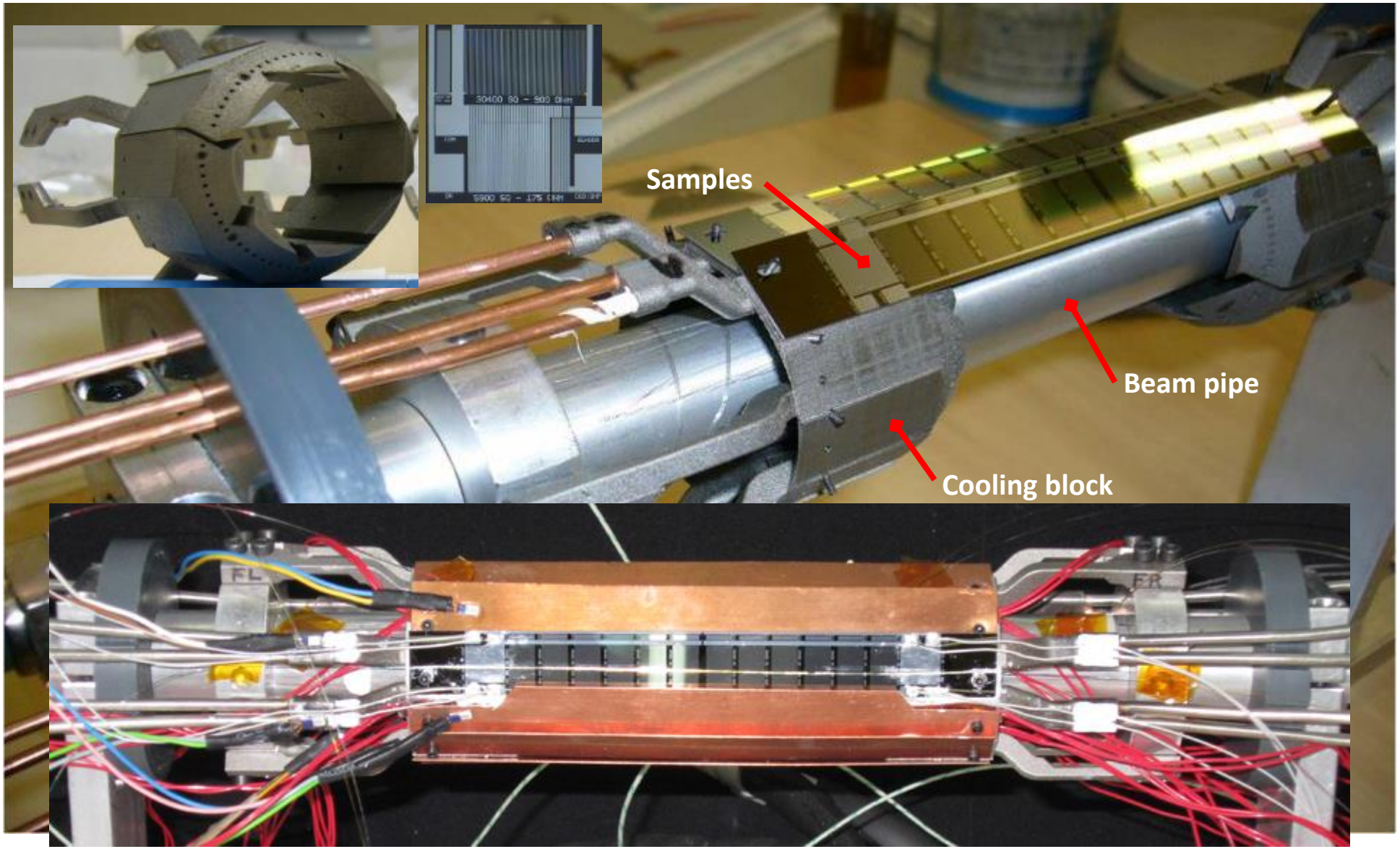
T_{env}=-5°C
T_{cb}=8°C

→

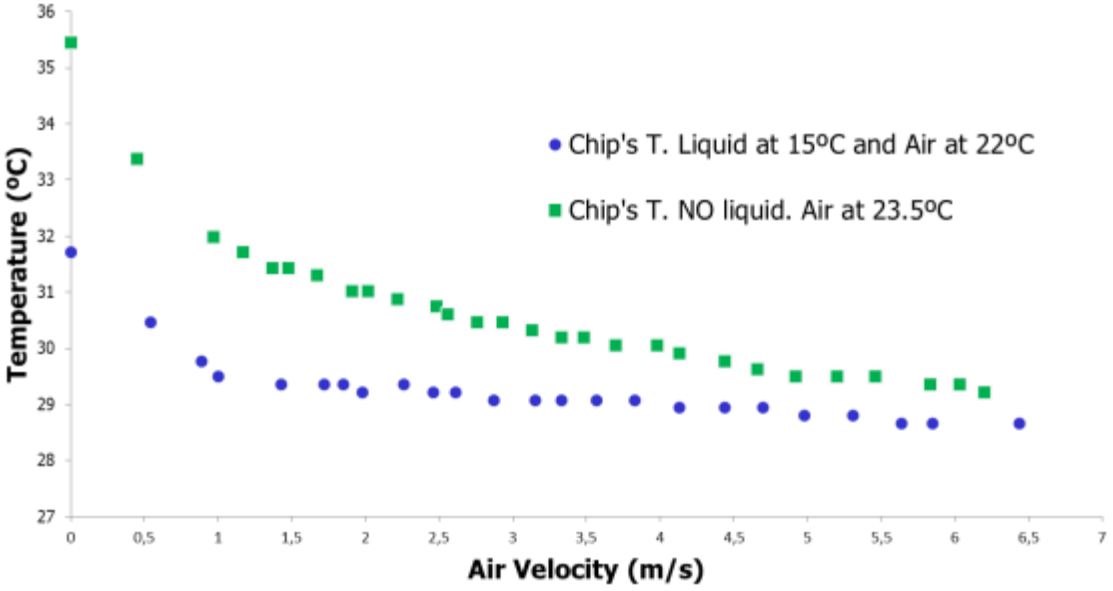
$T_{SENSORmax}$=14°C
DeltaT=4.7°C

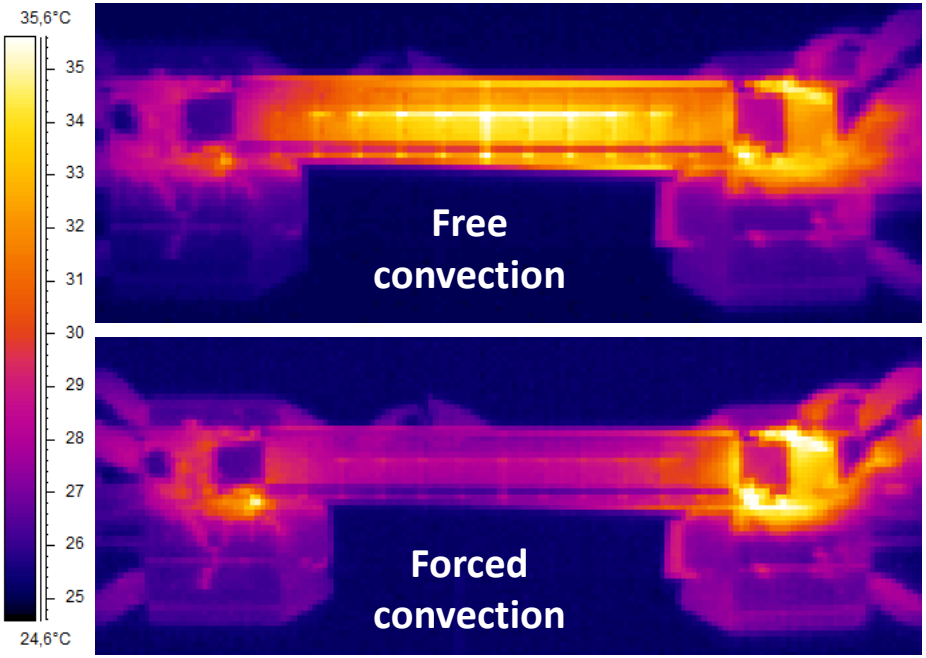
Just a gentle air flow (2 m/s) is enough to decrease and homogenize the temperature distribution

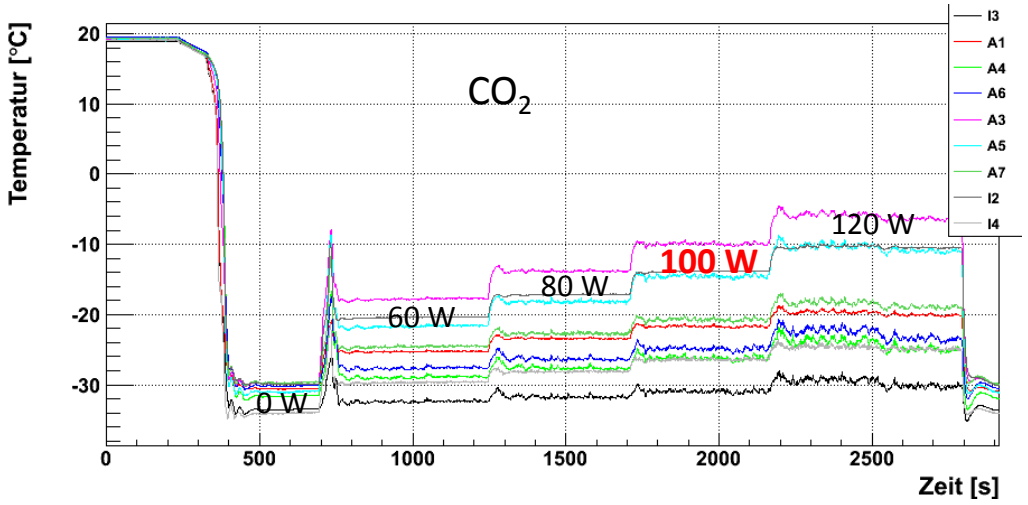
PXD Mockup



PXD Thermal Measurements

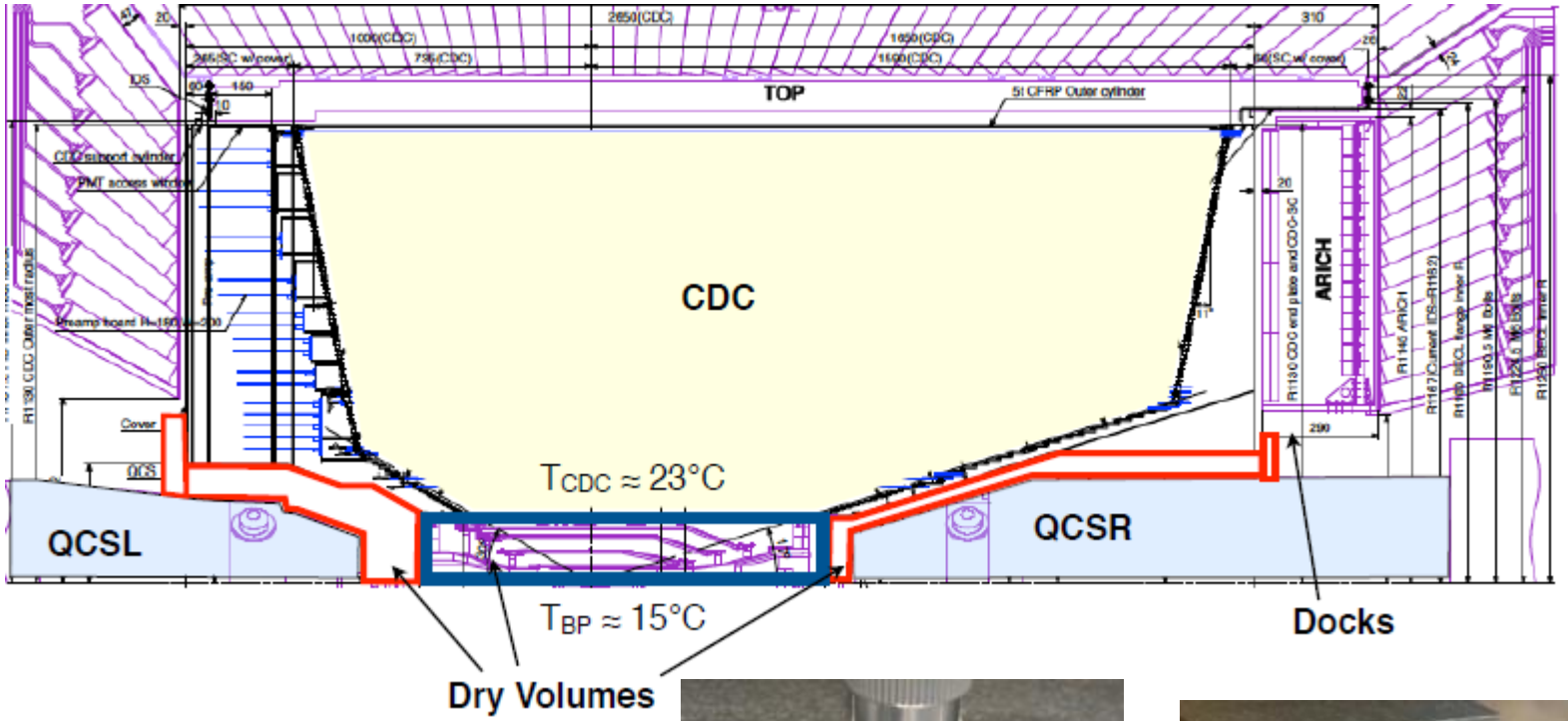


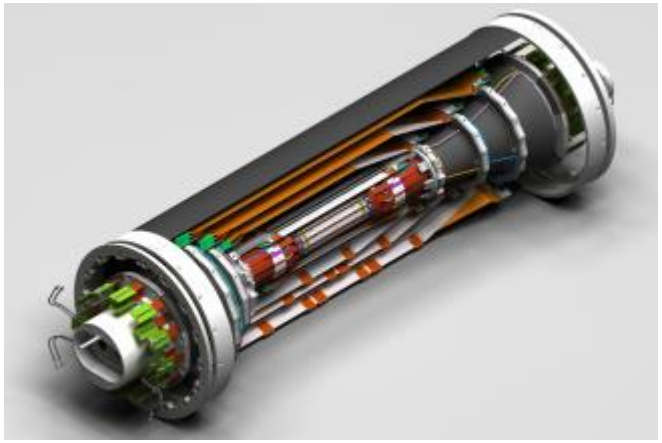


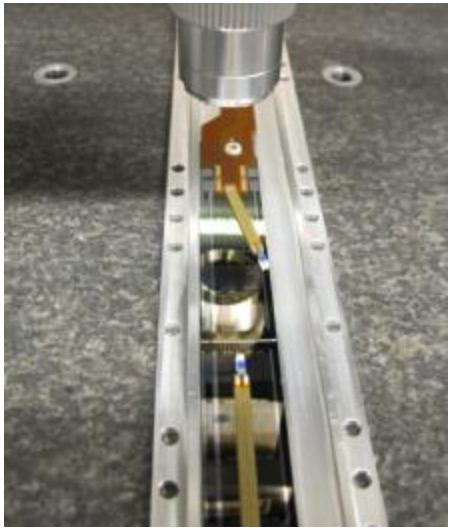


Cooling proof of principle

VXD Thermal Mockup







ILD Vertex Detector

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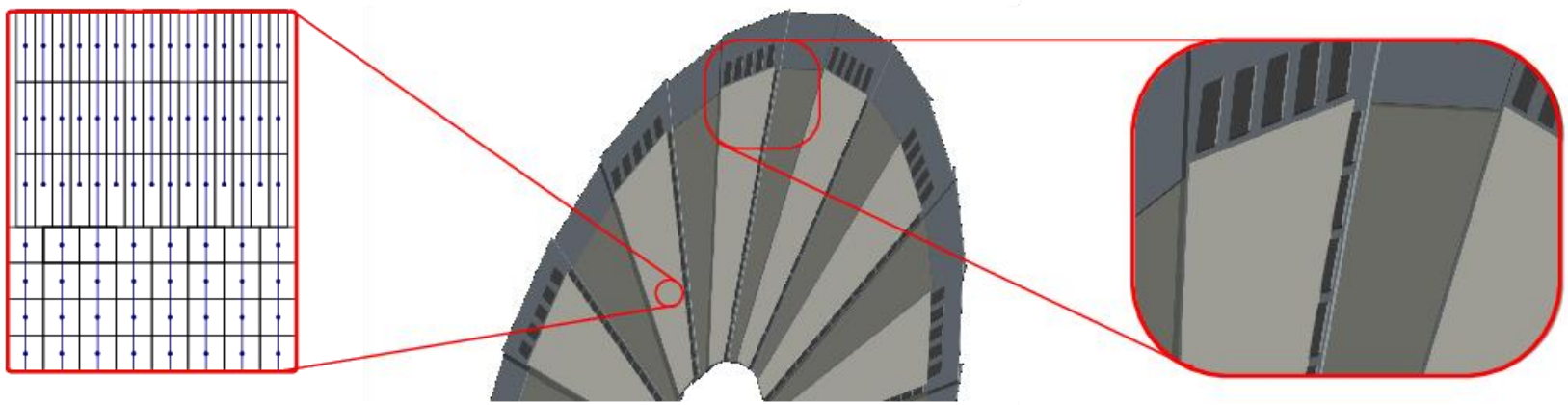

DEPFET Mechanical Petals

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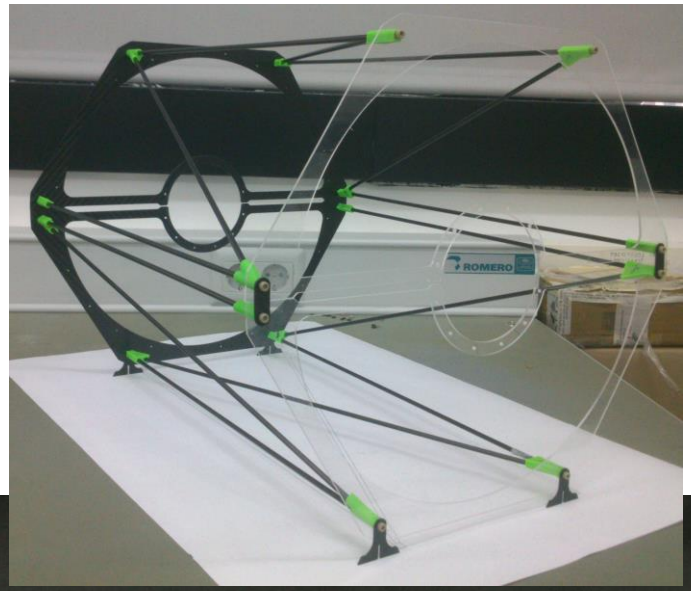

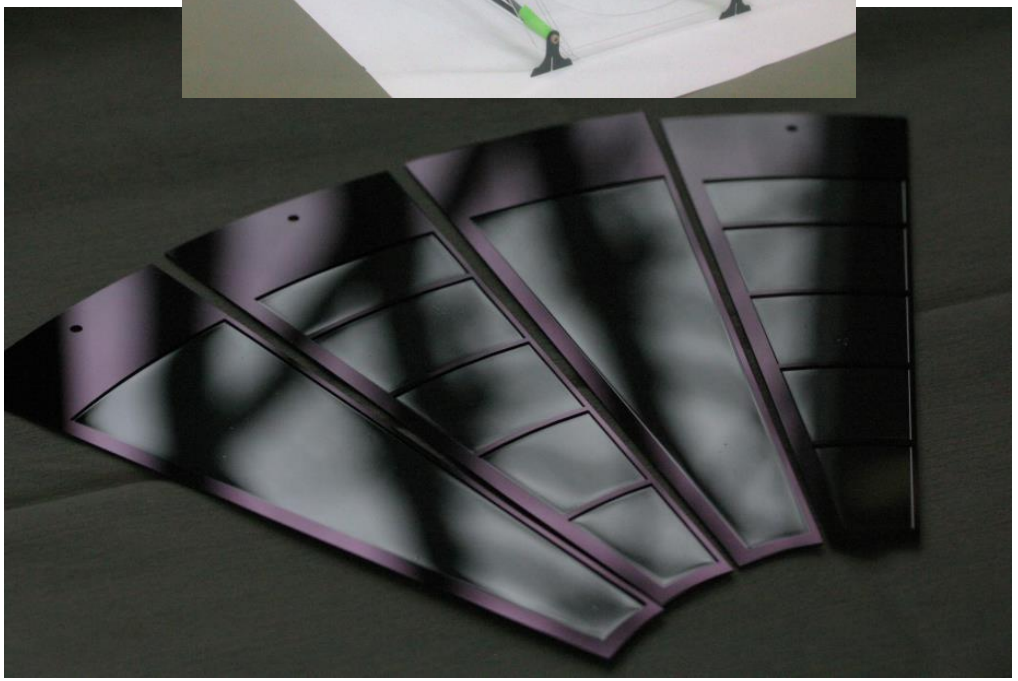

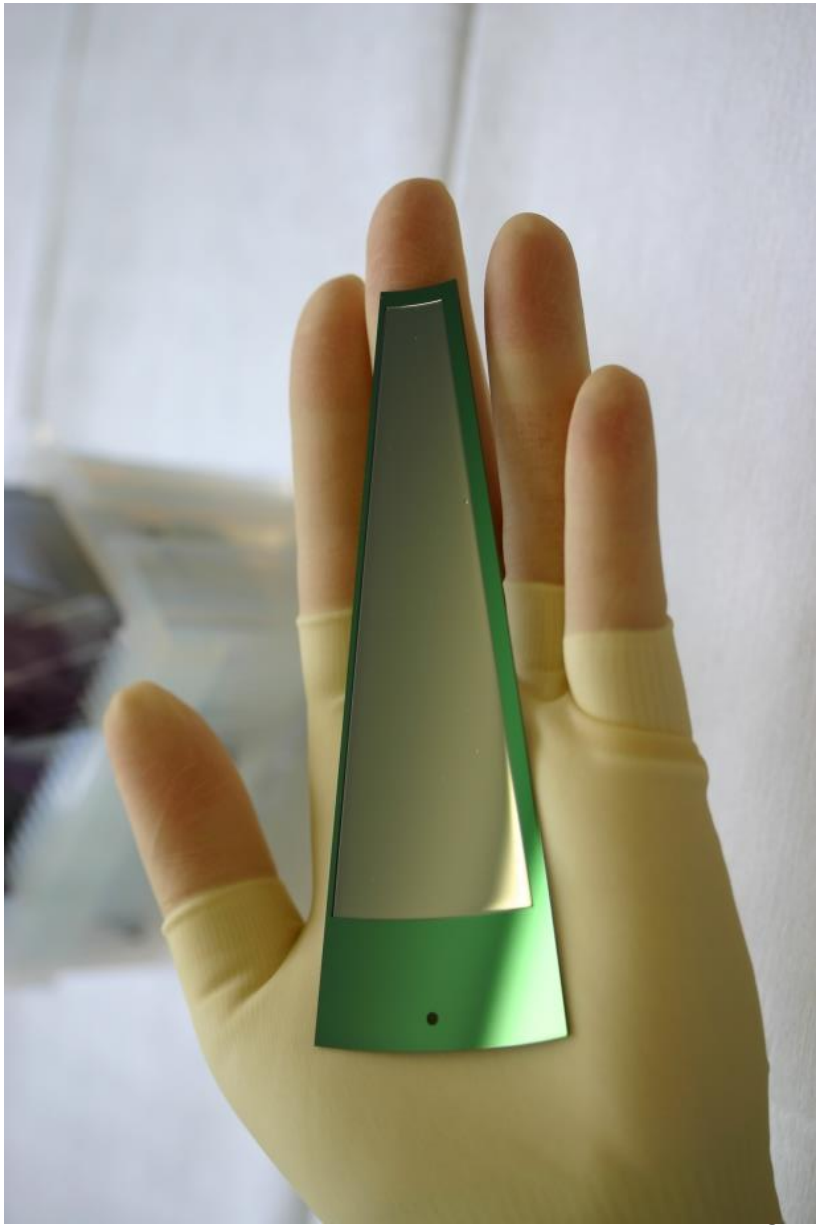

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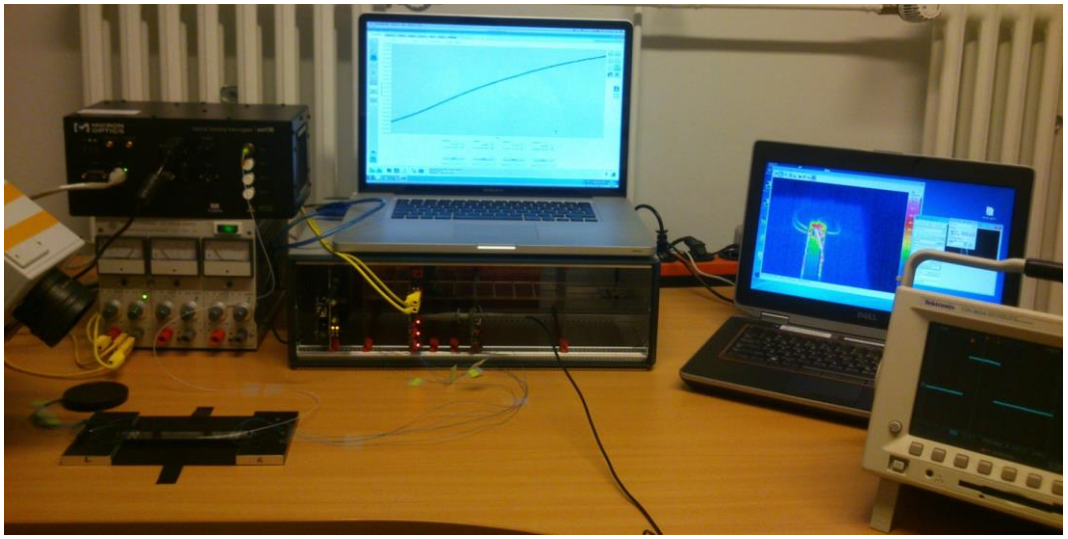
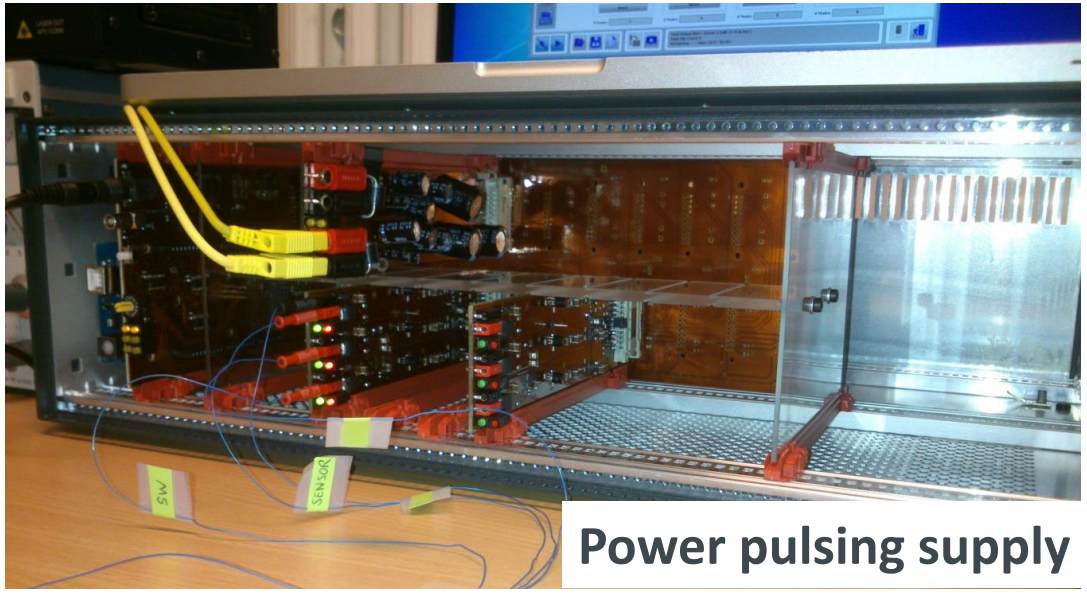
Power Pulsing

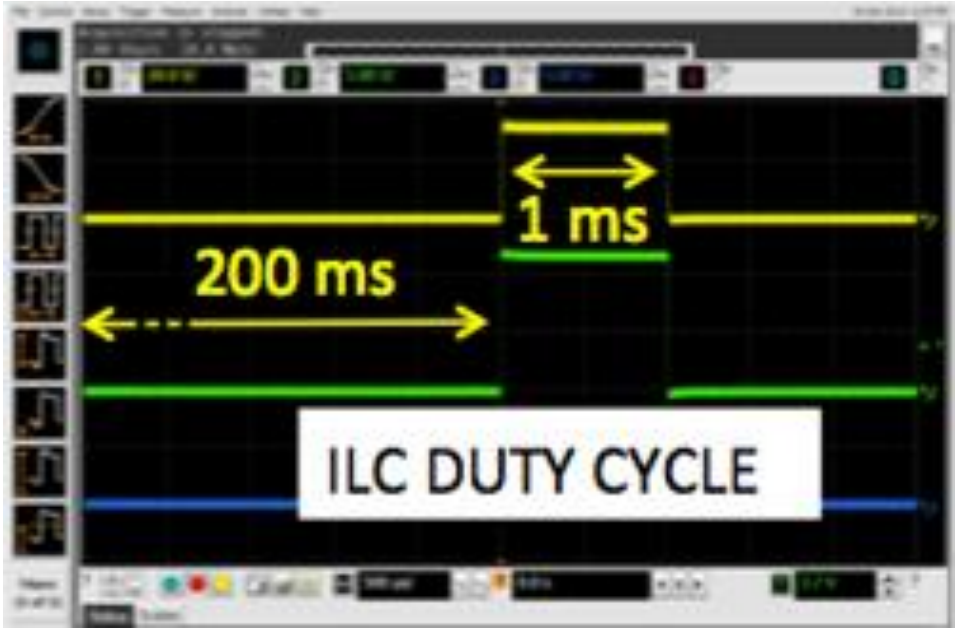


Mechanical DEPFET ladder sample

Study of the thermo-mechanical properties of thin sensors with a pulsed power supply



Power pulsing supply



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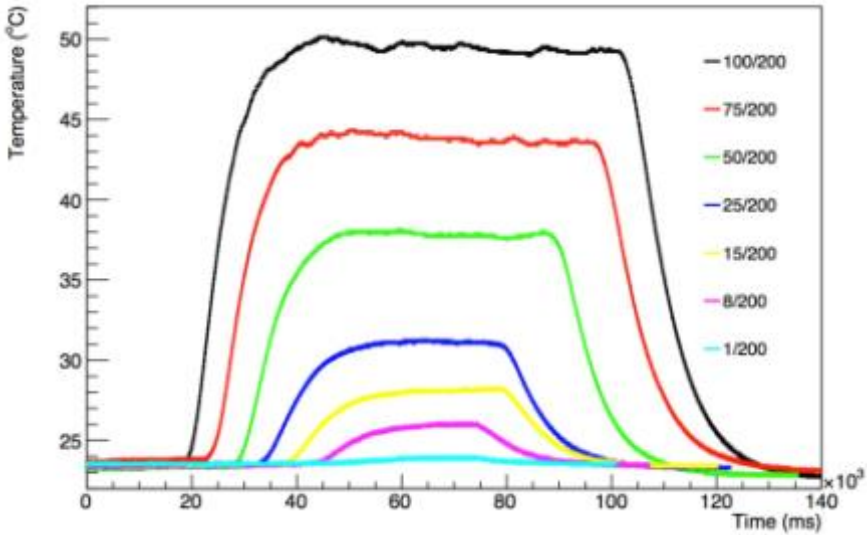
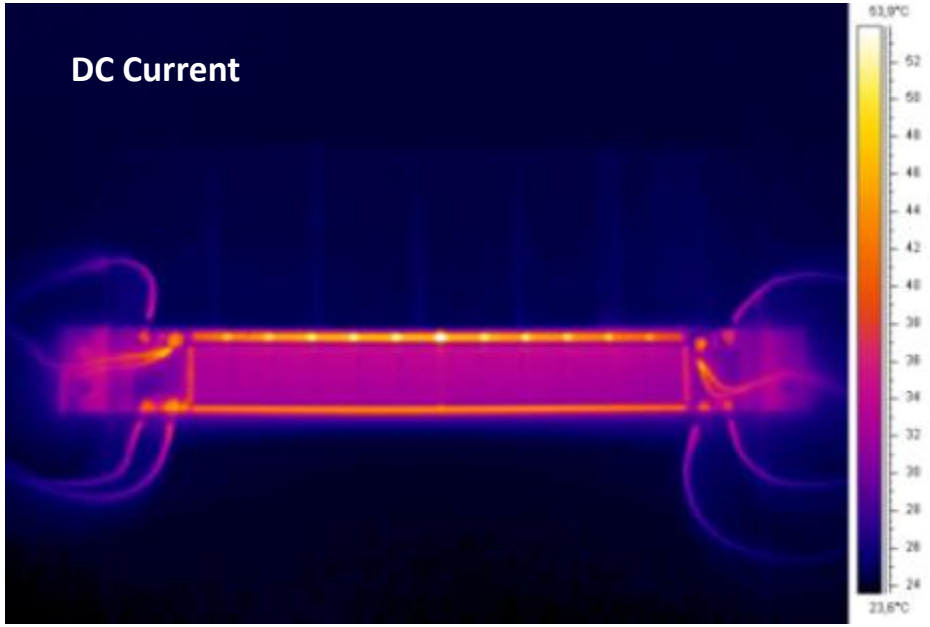
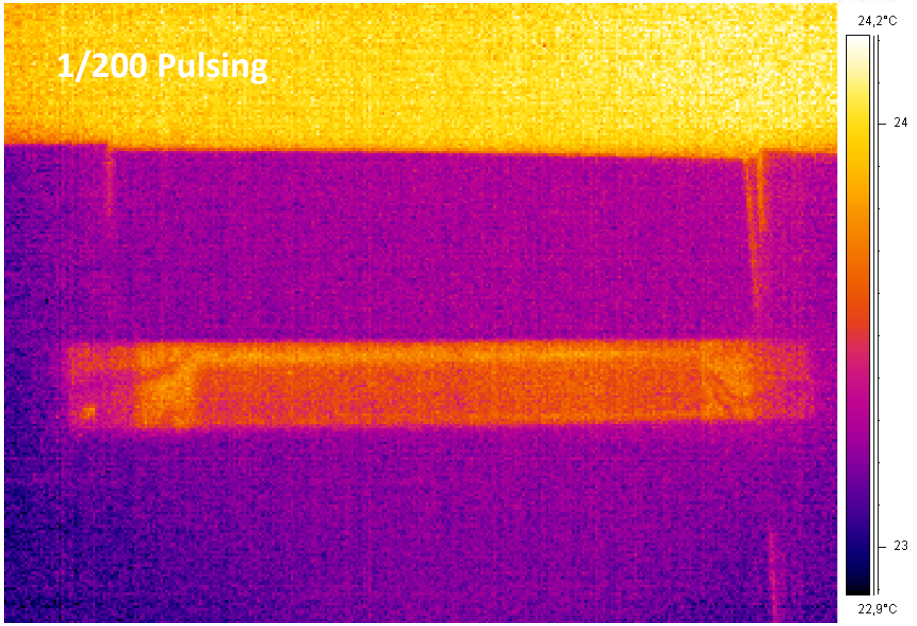
Power Pulsing

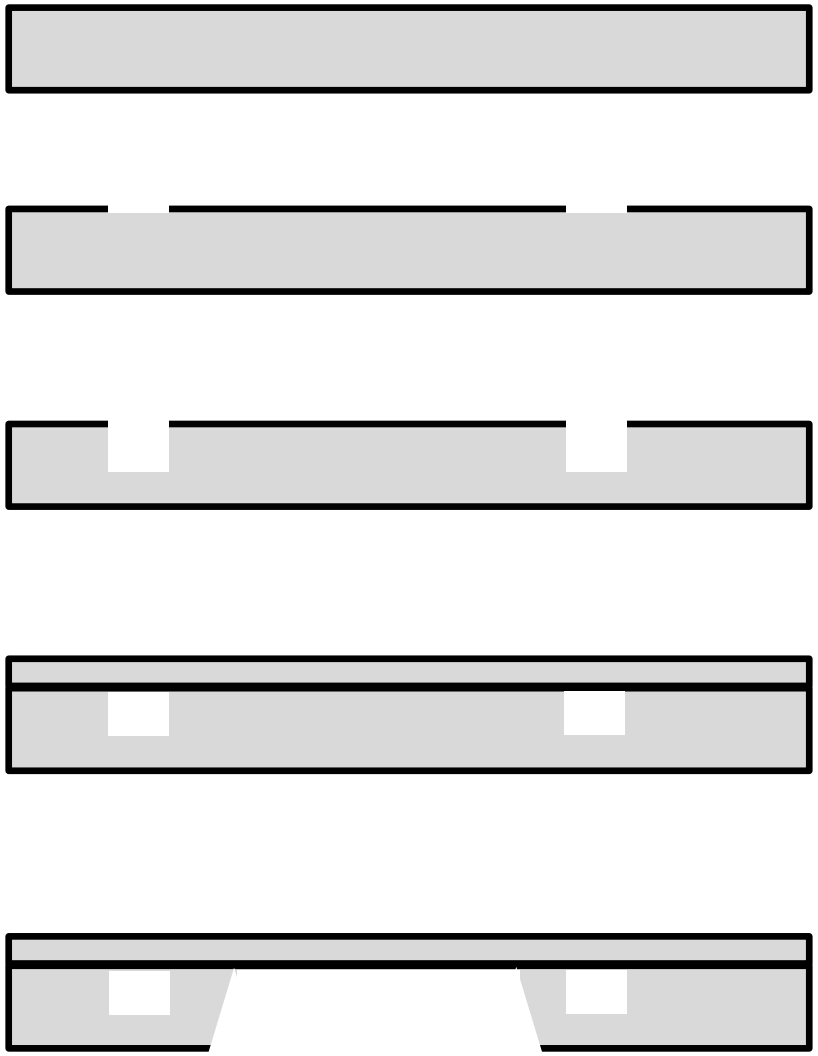
Supply pulsed power with ILC duty cycle and monitor temperature
- Ladder responds to sudden power-up with 2-4 s time constant
- Average temperature for nominal power and 1/25 duty cycle settles around +2 degrees (no active cooling)





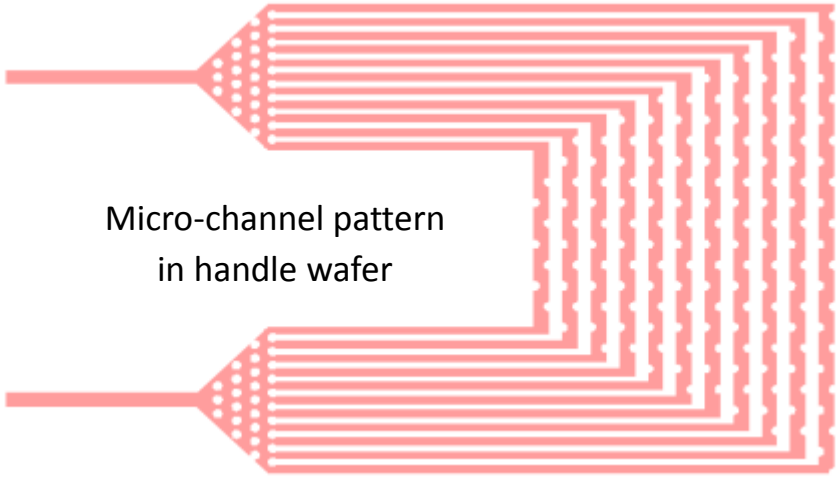


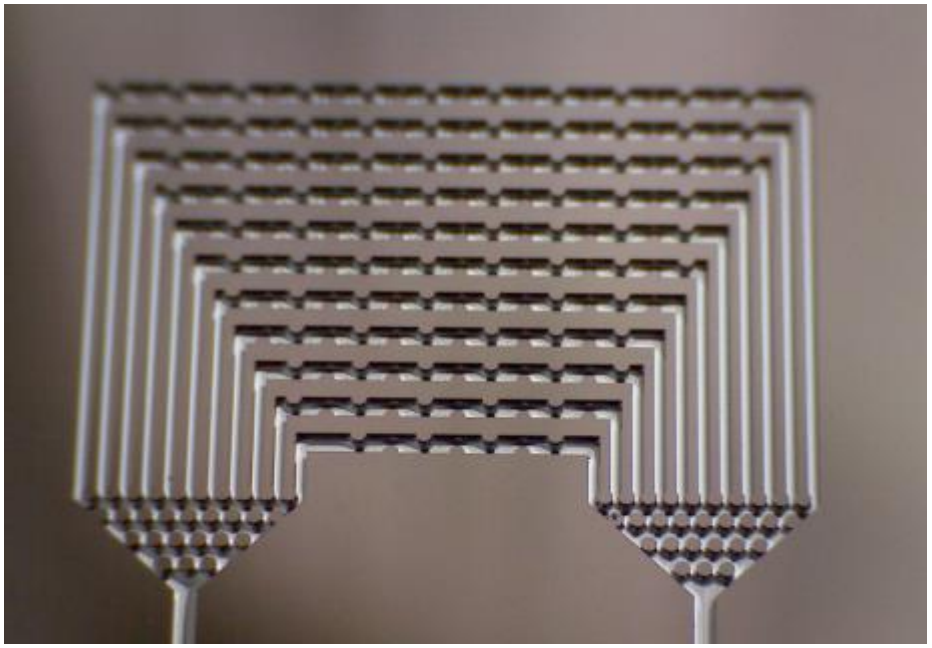
MCC: The Concept

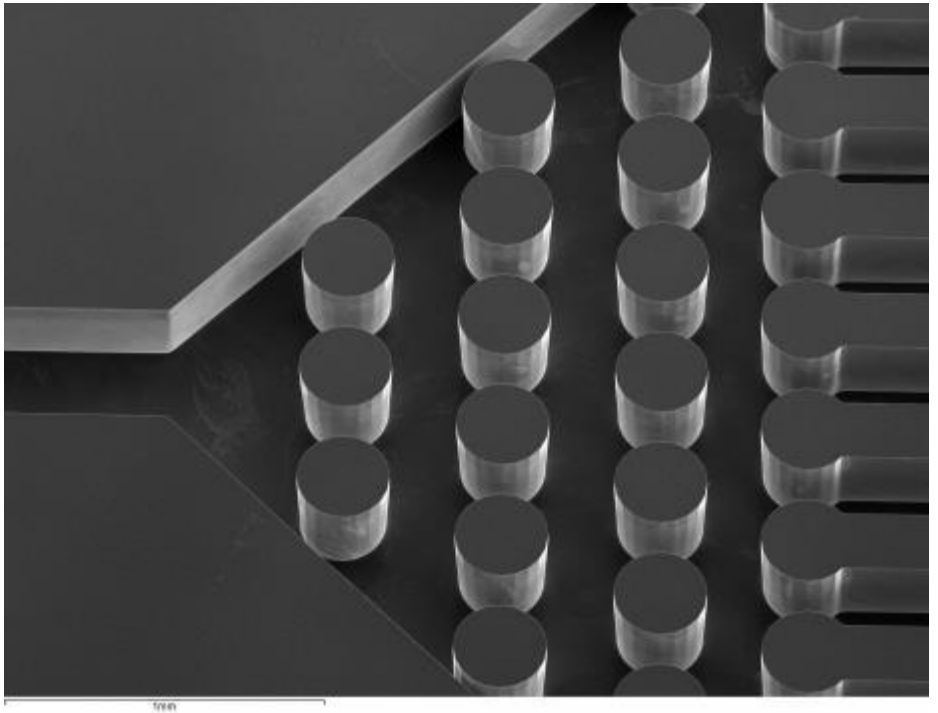


- Start with oxidized handle wafer
- Define lithographically µ-channels, etch oxide
- Etch micro-channels, blind via
- Bond prepared top wafer as usual
- Finish SOI wafer (“Cavity SOI”)
- top wafer for DEPFETs
- Handle wafer with µ-channels under ASICs
- Handle removed in sensitive area
- Channels exposed after cutting

MCC: The Realization

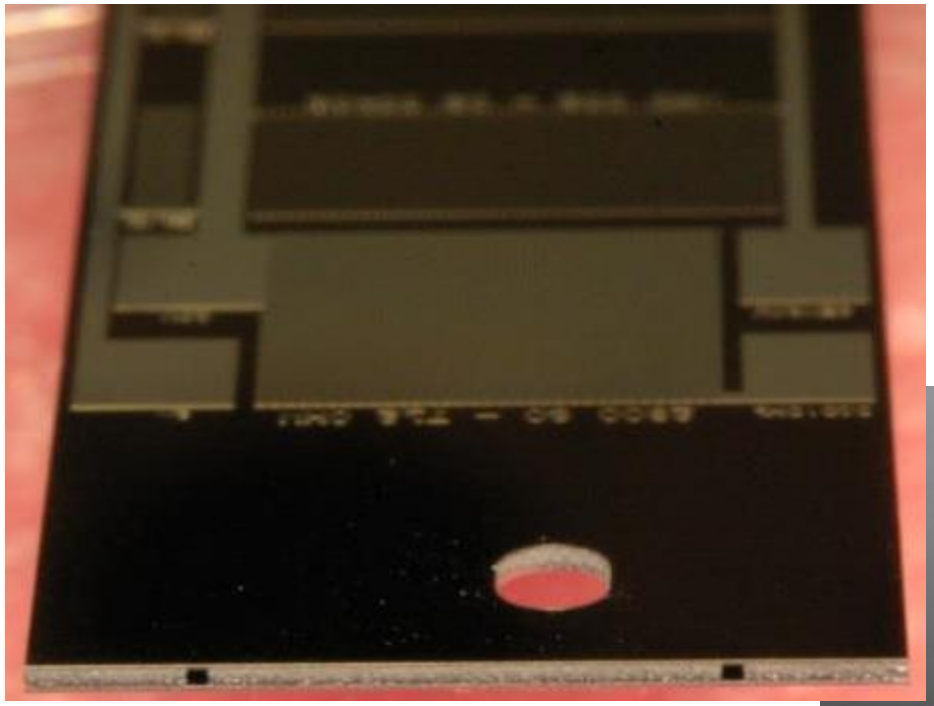


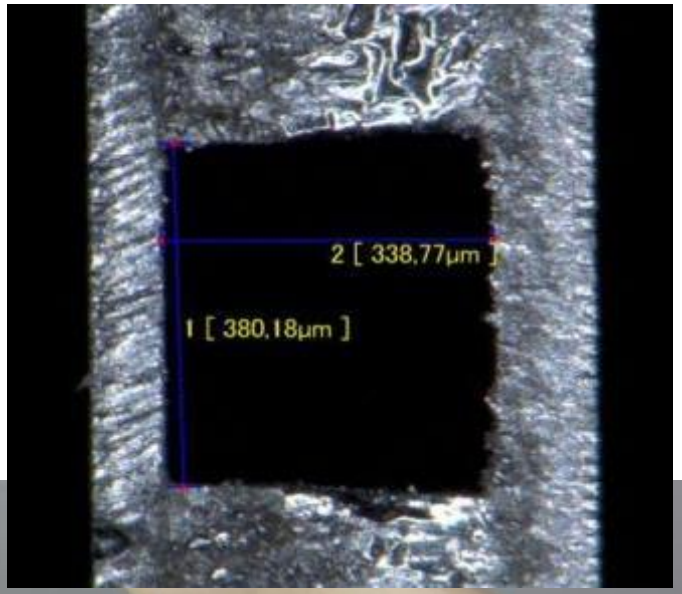


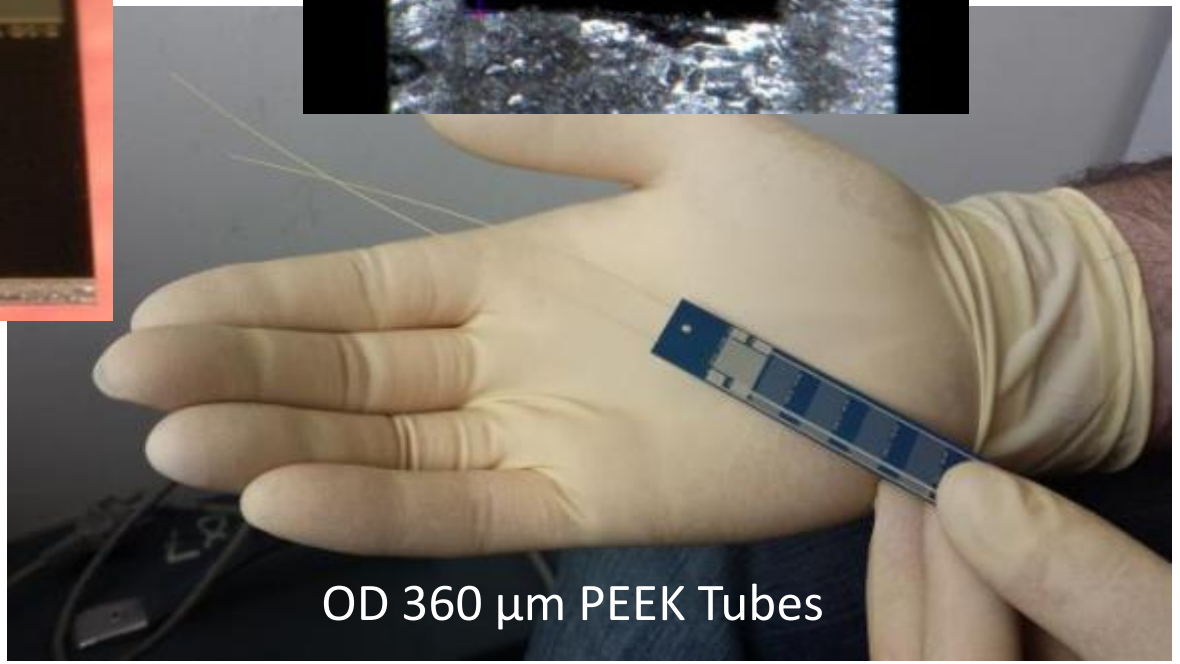


Inlet and outlet: ~350 µm deep, 400 µm wide

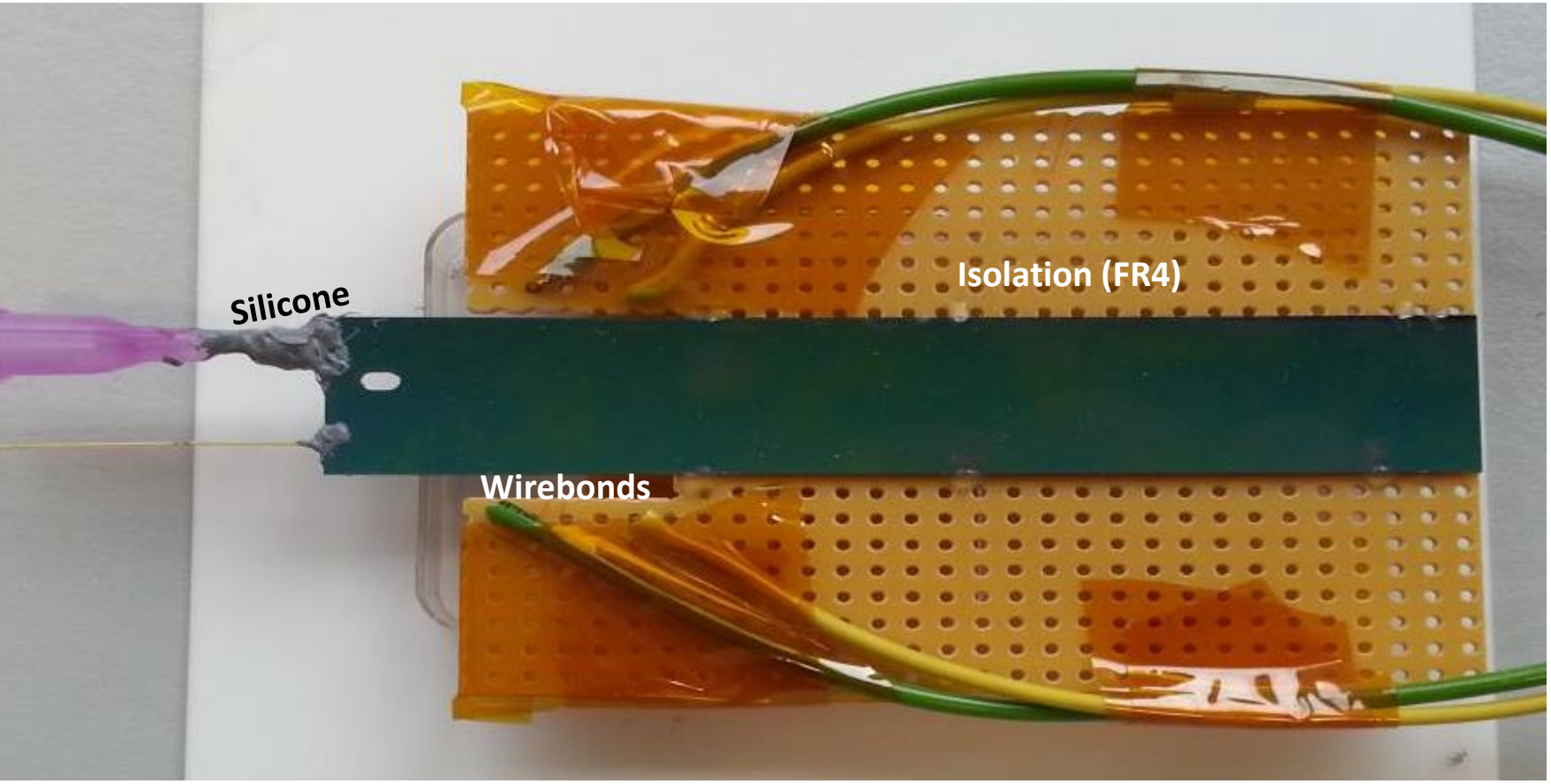
Connection





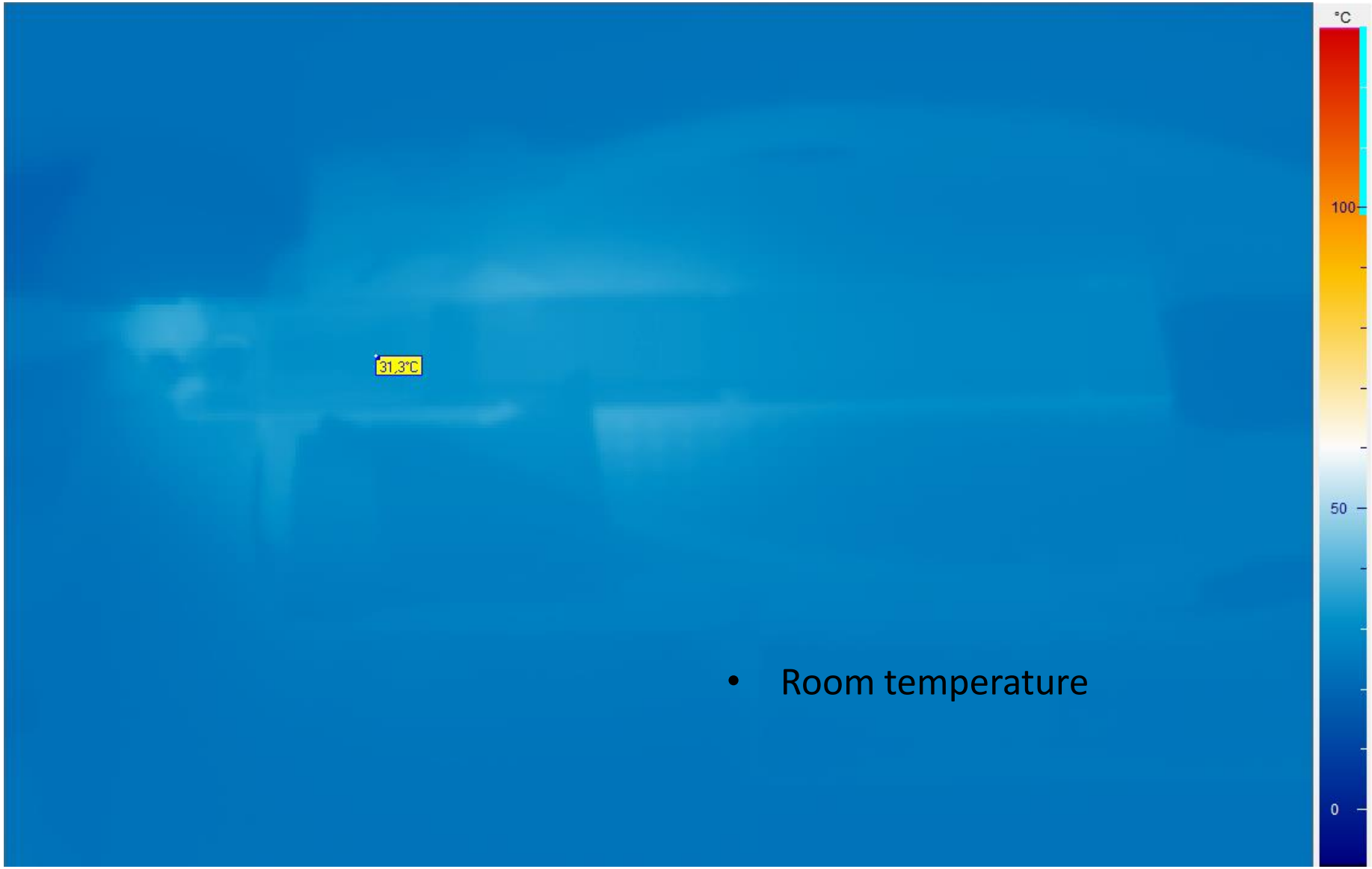


Experimental Setup



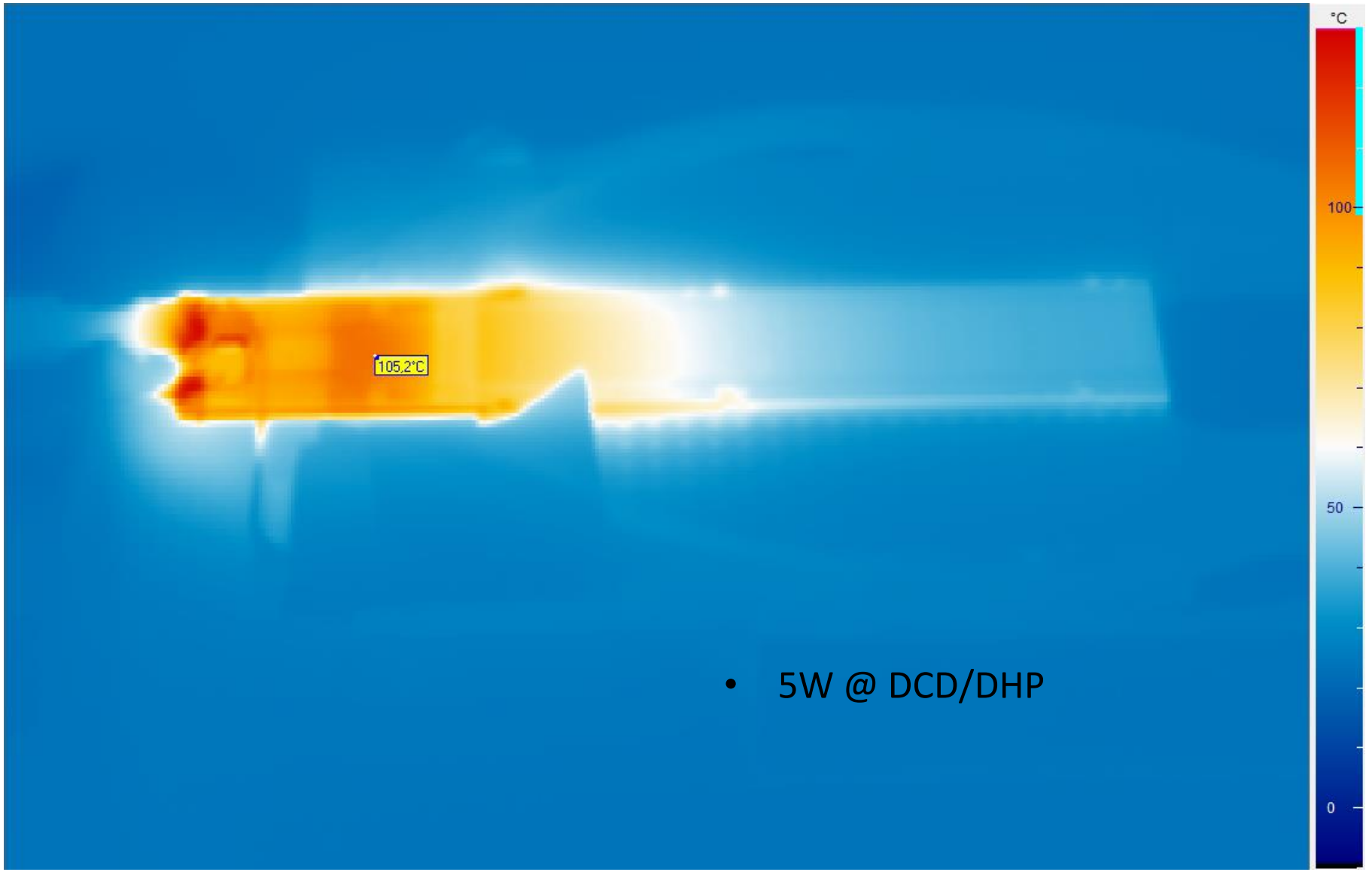
- Max mass flow= 0.1 l/h (2.5 bar)
- Water at room temperature
- DCD/DHP active only

Initial: Everything's cold



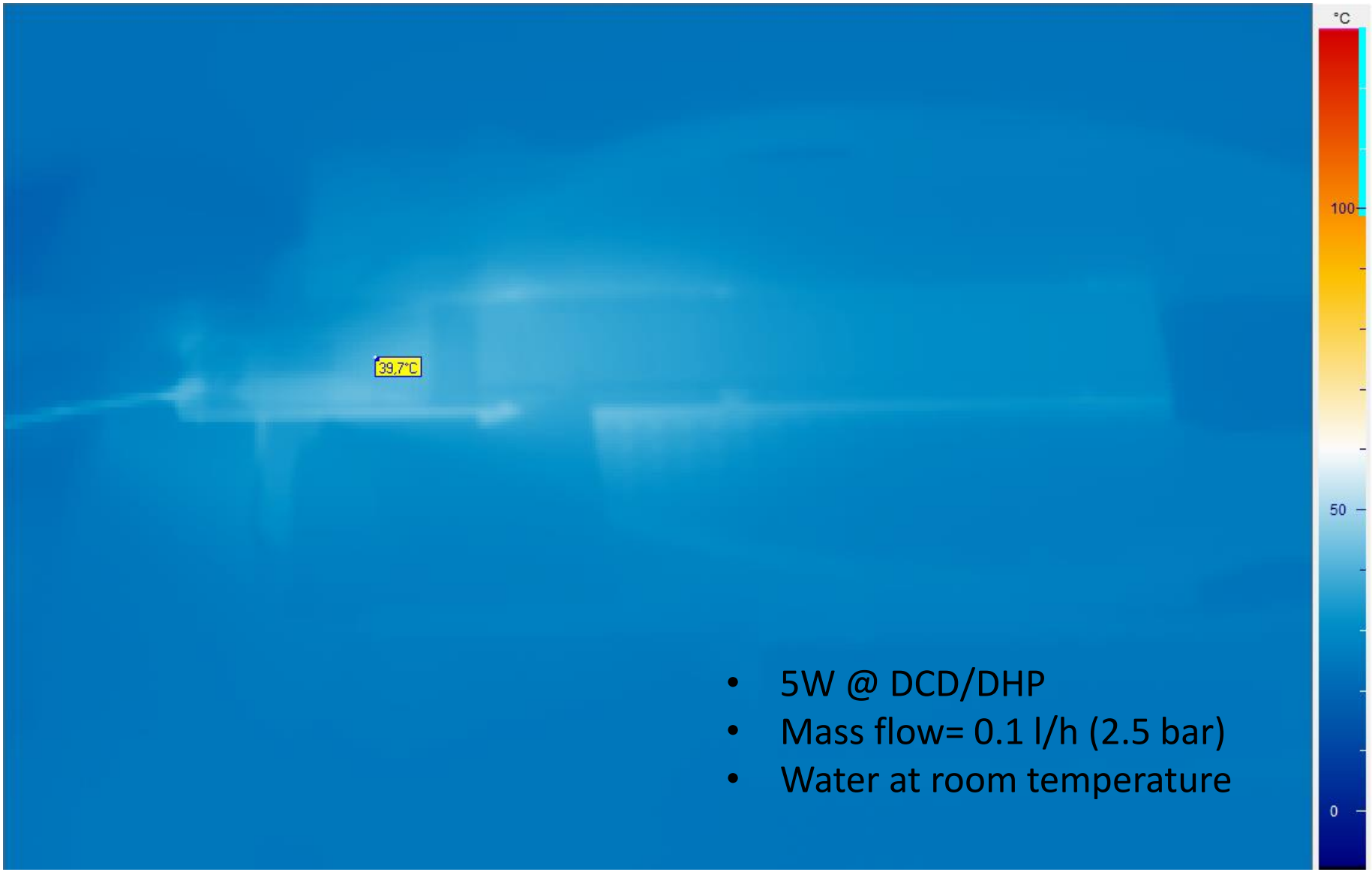
- Room temperature

Power On – Cooling Off



- 5W @ DCD/DHP

Power On – Cooling On



- 5W @ DCD/DHP
- Mass flow= 0.1 l/h (2.5 bar)
- Water at room temperature

Power On – Cooling On

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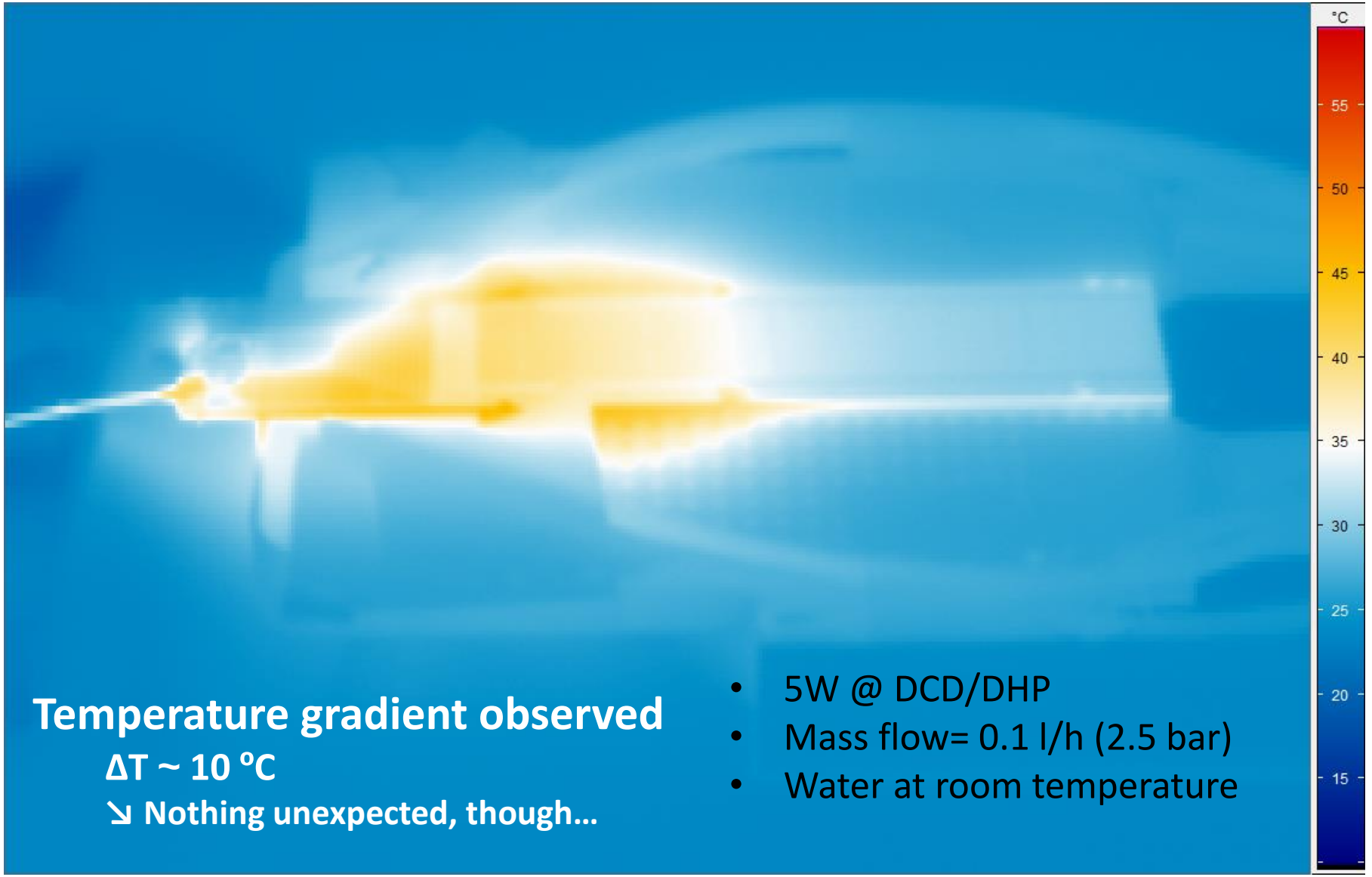


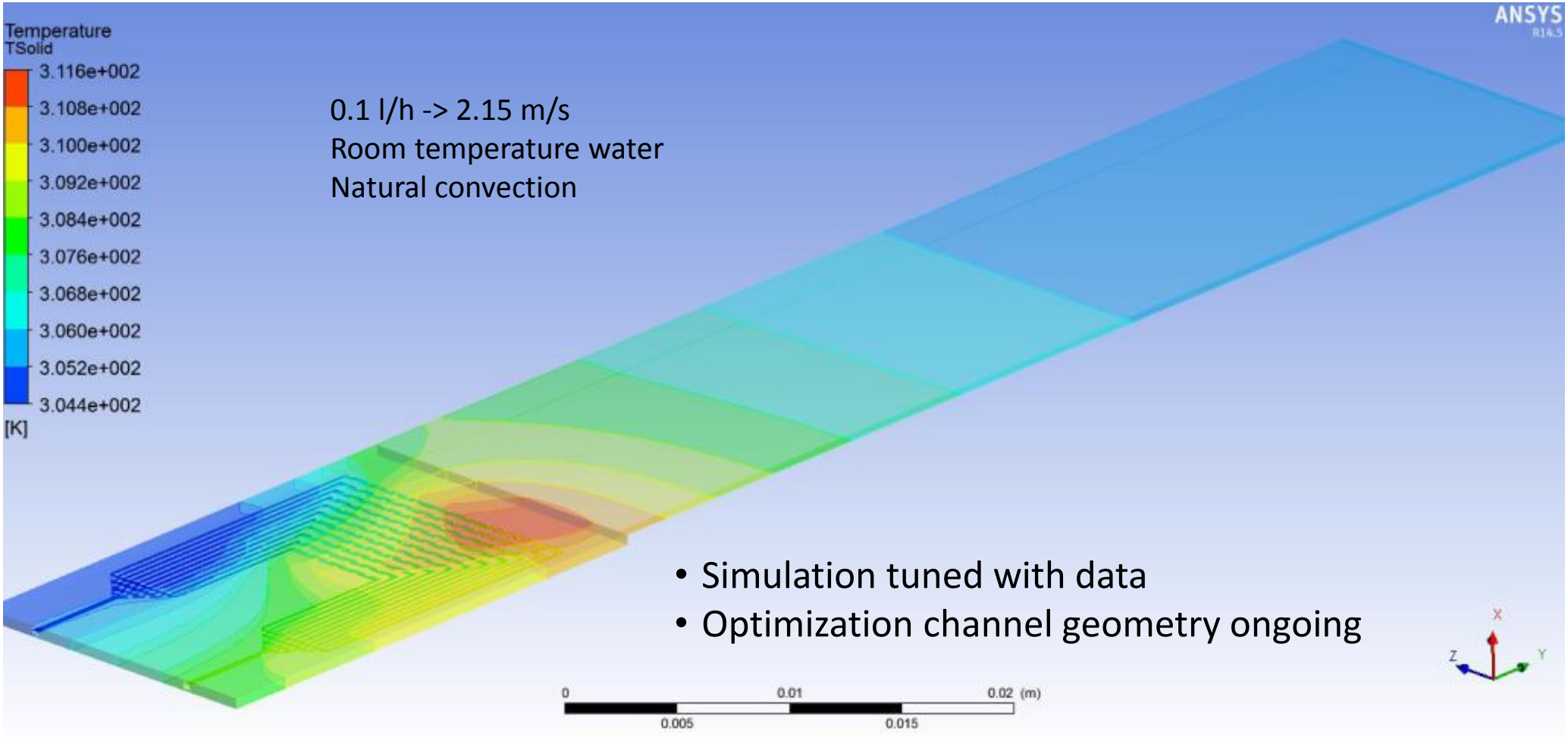
Temperature gradient observed

ΔT ~ 10 °C

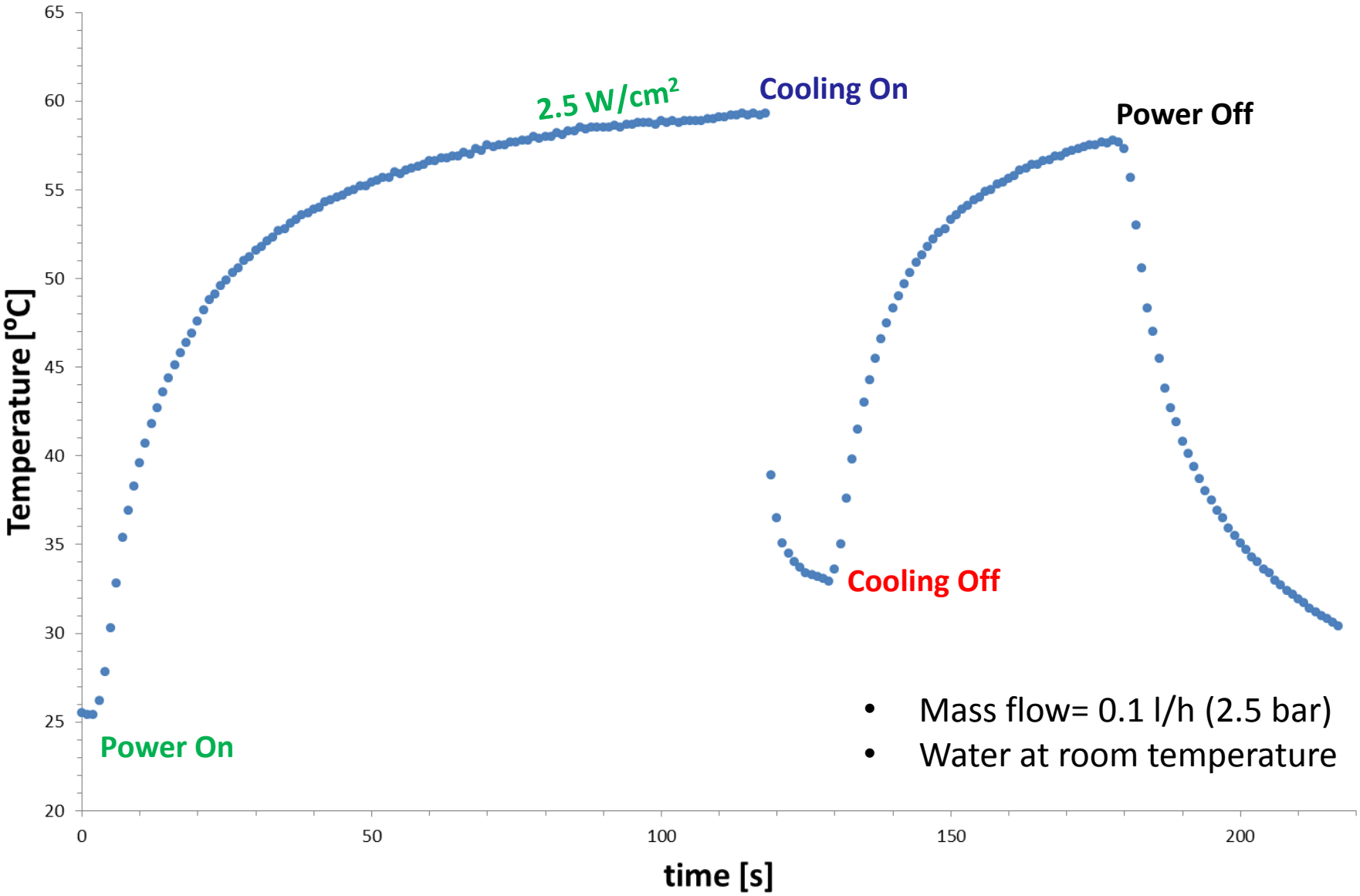
↘ Nothing unexpected, though…

- 5W @ DCD/DHP
- Mass flow= 0.1 l/h (2.5 bar)
- Water at room temperature

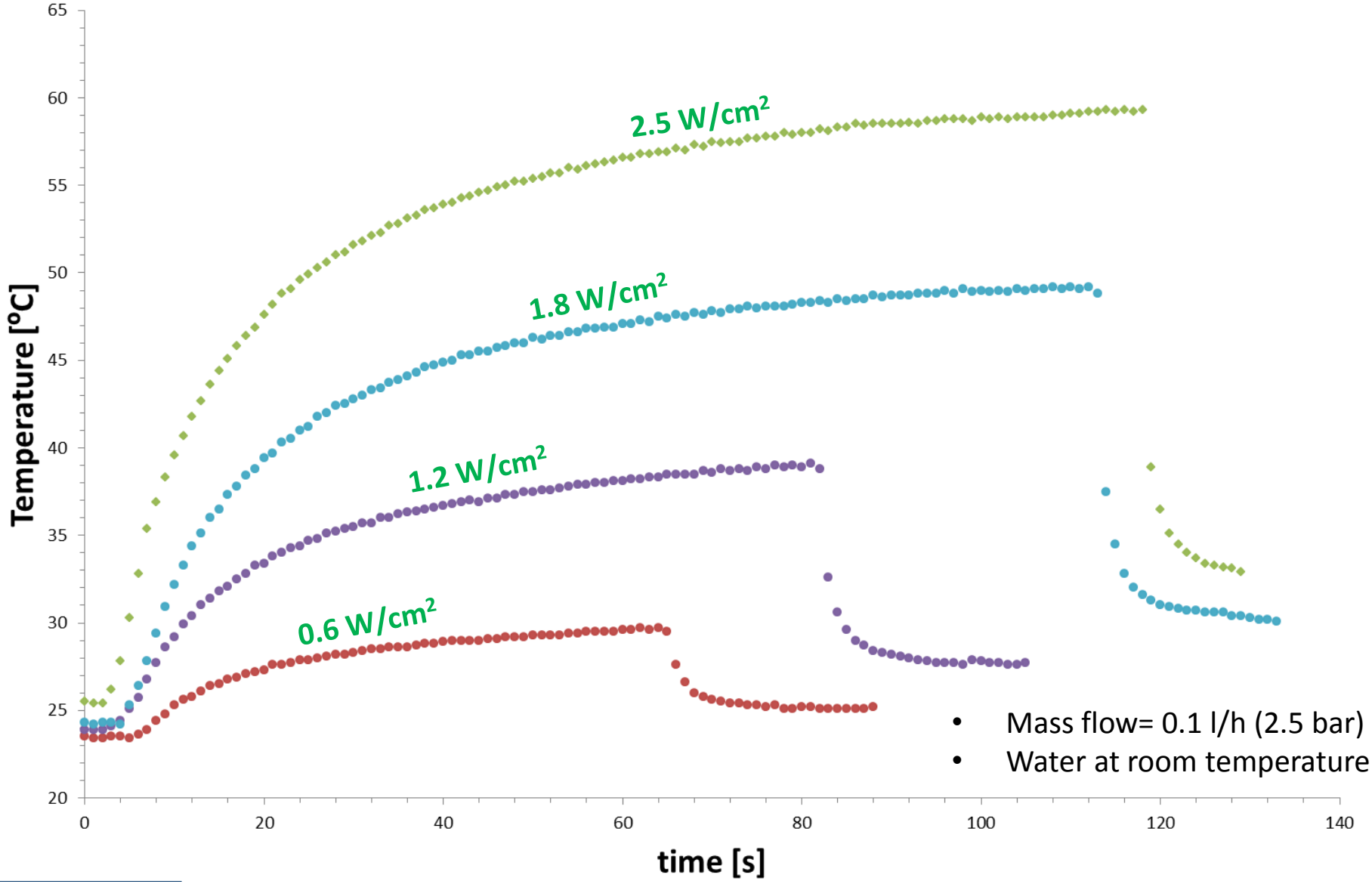
FEA Simulation



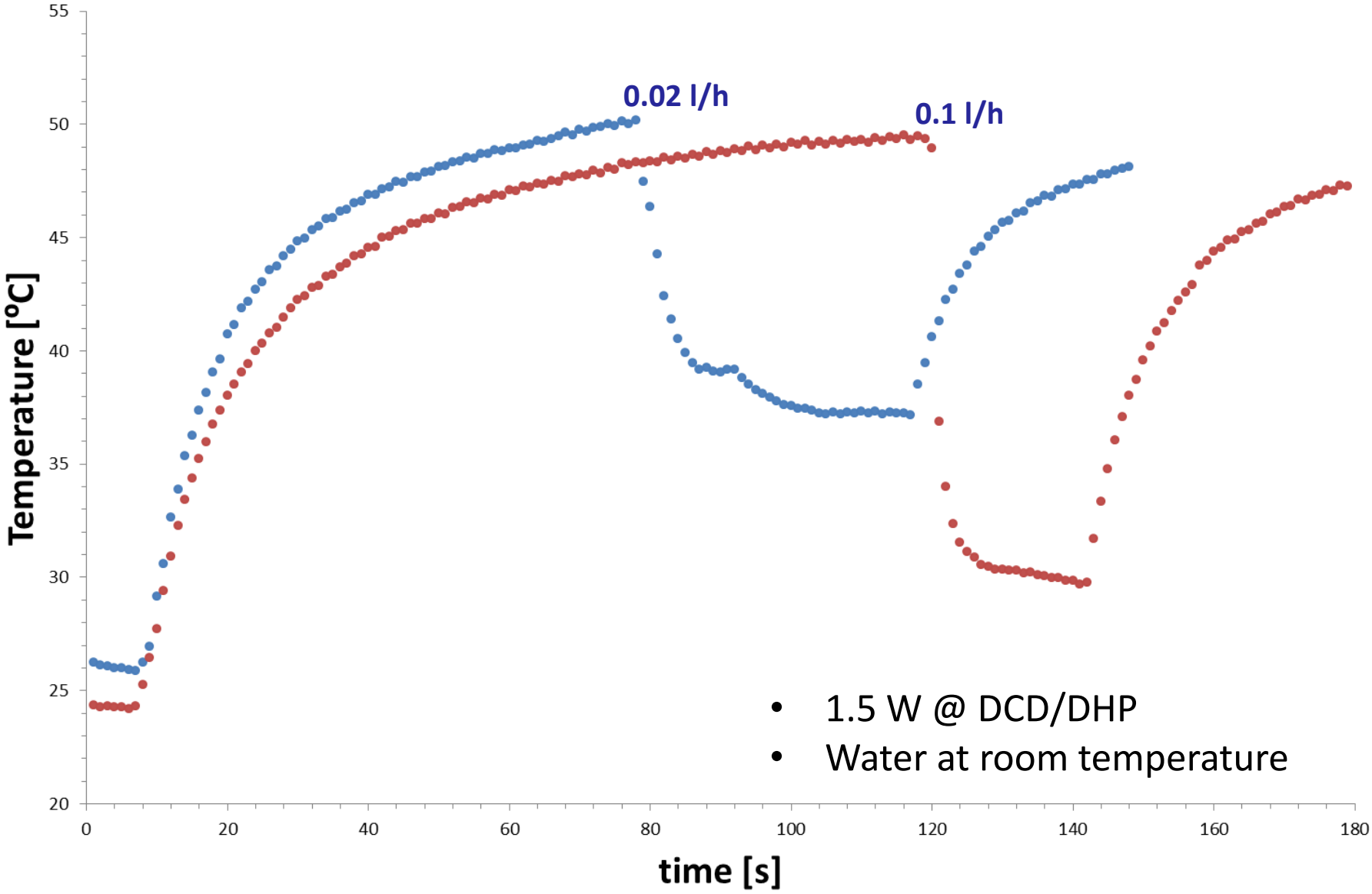
Time Evolution Temperature



Time Evolution Temperature

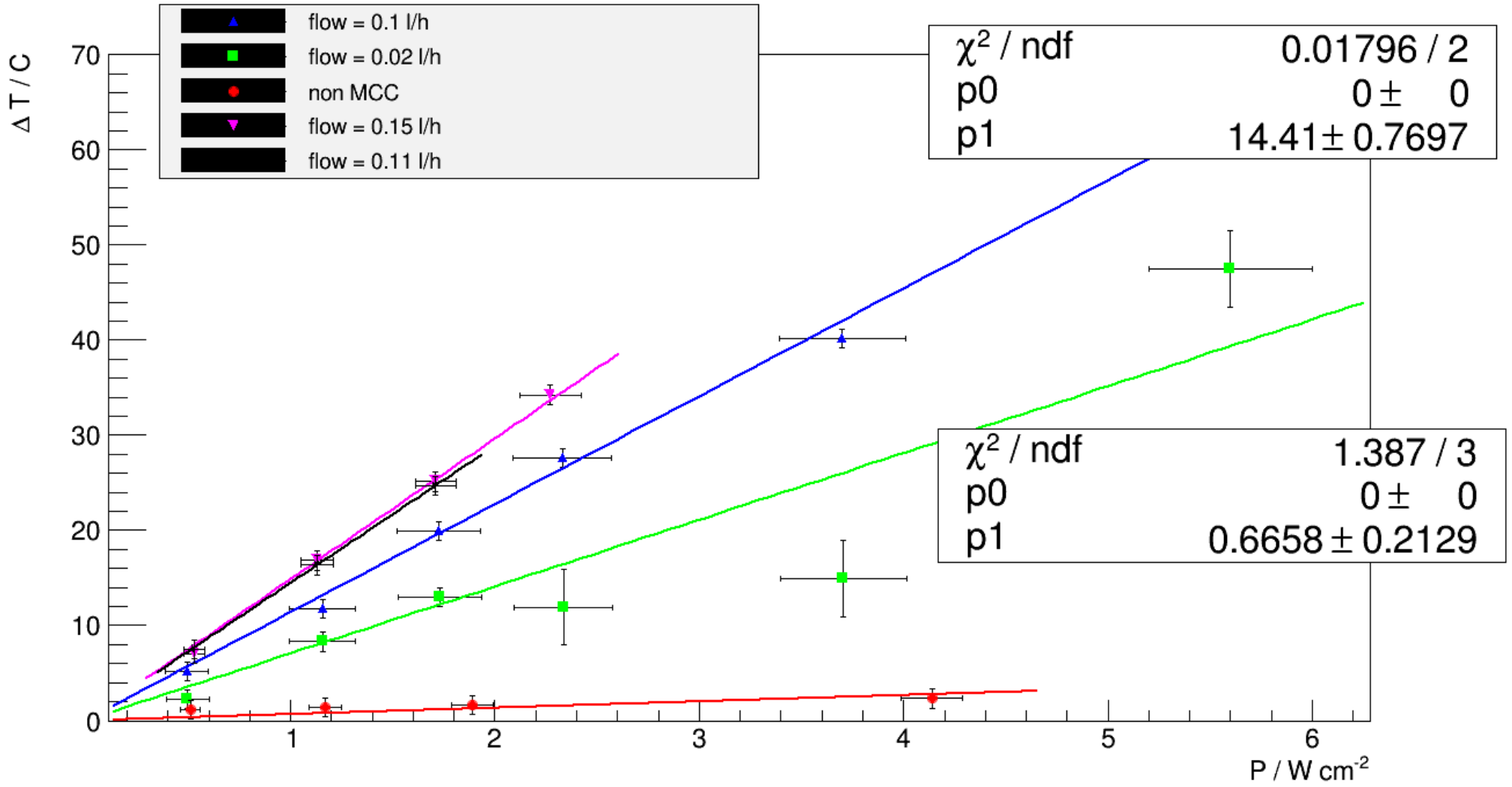


Mass Flow Impact



- 1.5 W @ DCD/DHP
- Water at room temperature

Mass Flow Impact



Summary

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- The DEPFET collaboration aims to develop an ultra-transparent solution for vertex detectors at Belle II and ILC
- A special thinning technique yields a self-supporting frame that requires no external support structure
- In the all-silicon ladder concept the material in the active region stays within a tight budget of 0.15% X_0/layer
- DEPFET samples for ladders and petals have been produced and submitted to thermo-mechanical tests, proving the feasibility of the cooling concept
- The first tests on ladders with integrated micro-cooling circuits show that this novel cooling scheme holds great promise

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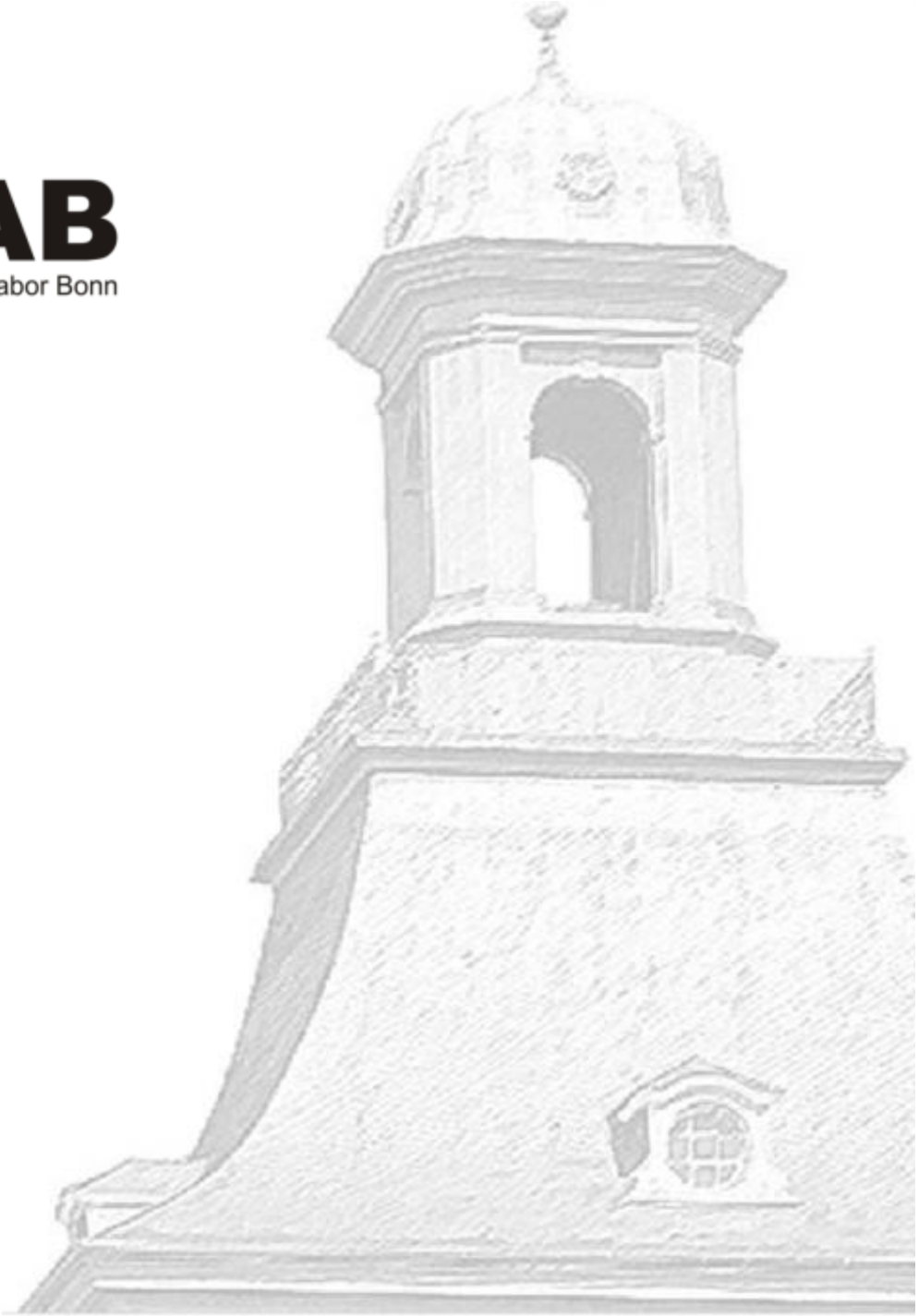
SI LAB
Silizium Labor Bonn



Thank you

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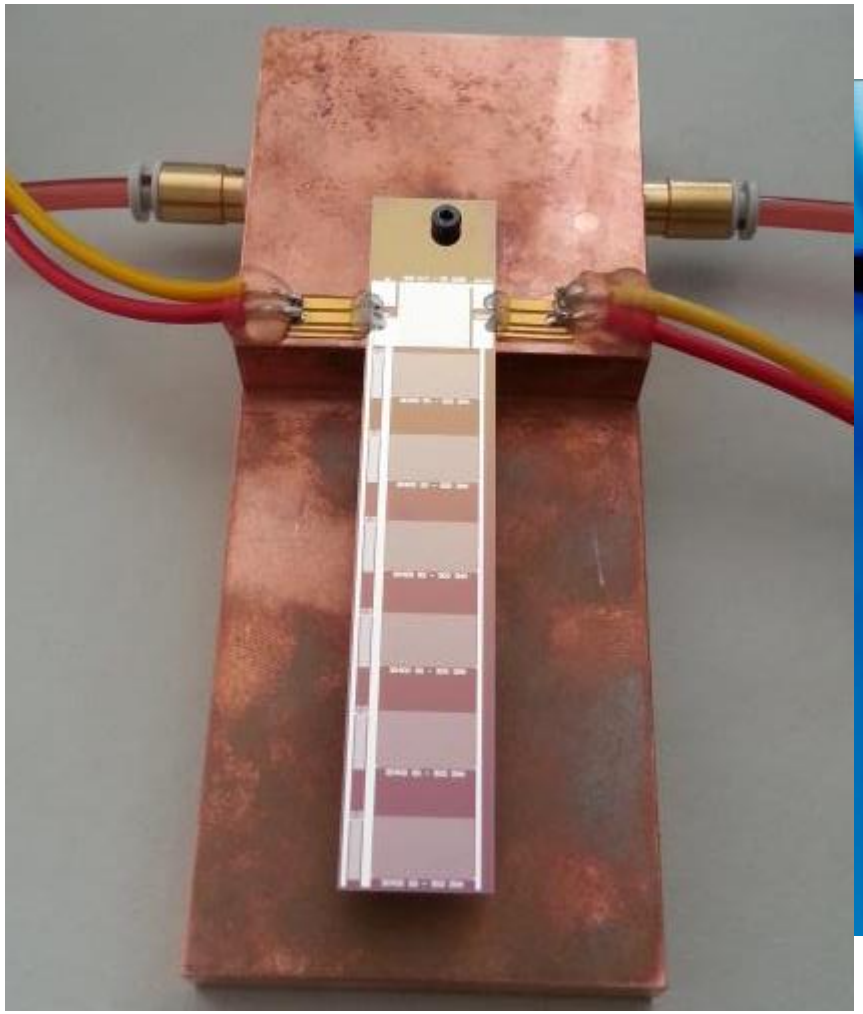
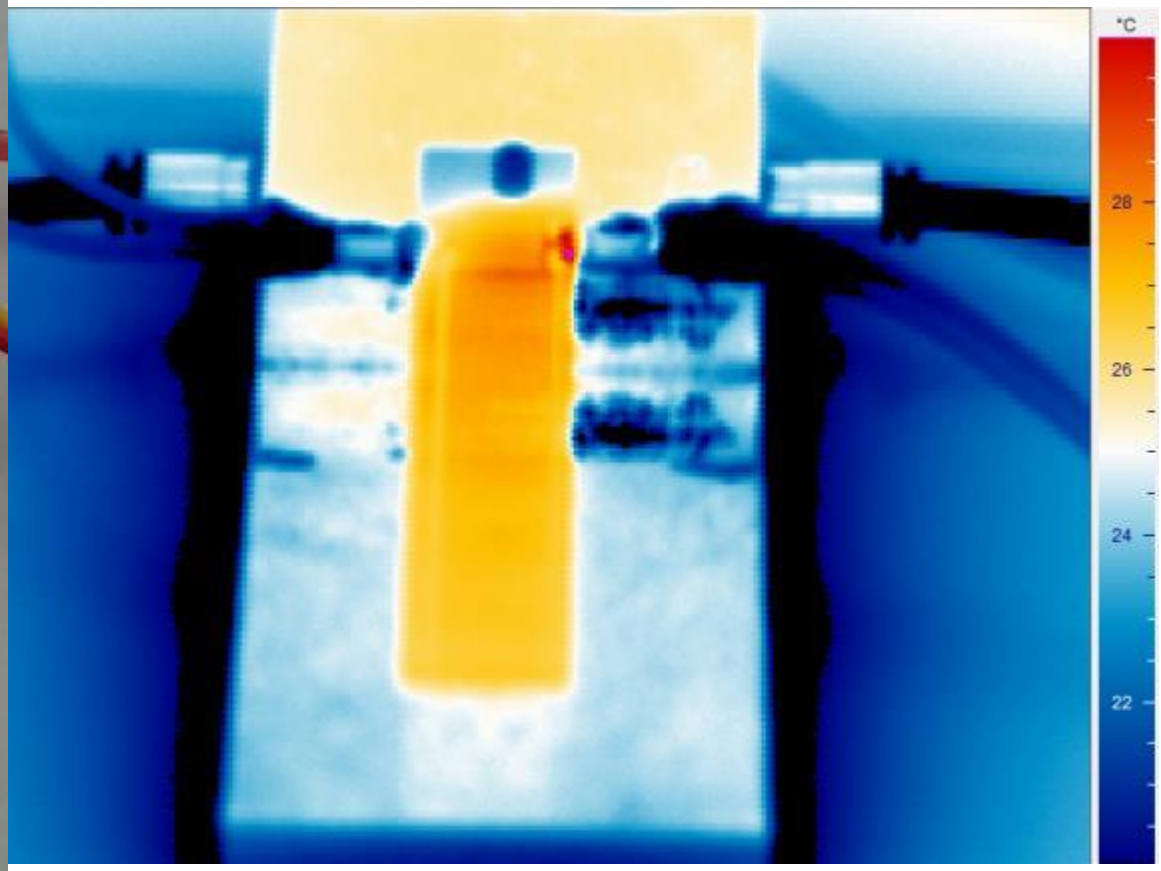
Cross Check Nominal Cooling Option





- Non-MCC option for x-check
- Cu Cooling Block + Lab chiller

Velocity Profile

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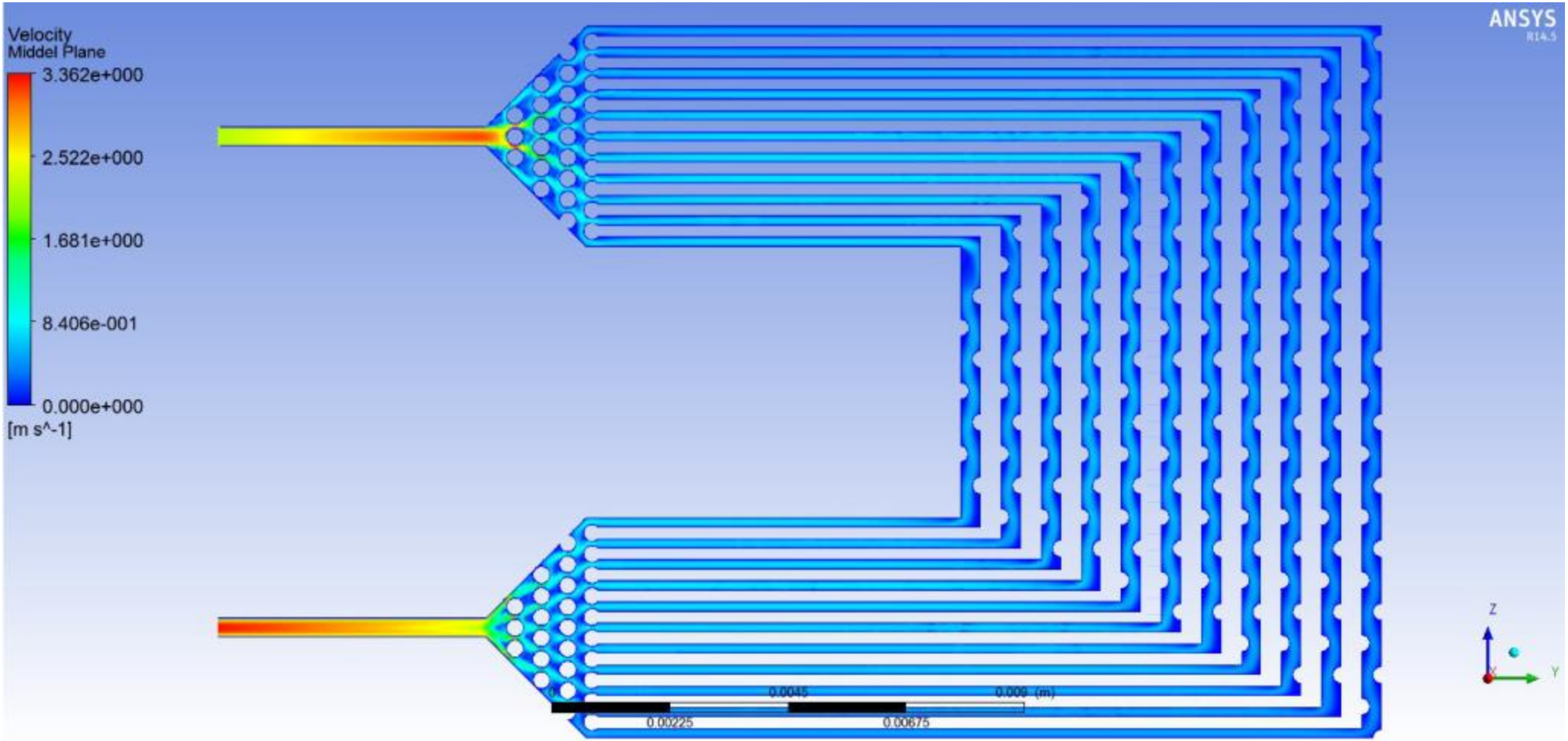

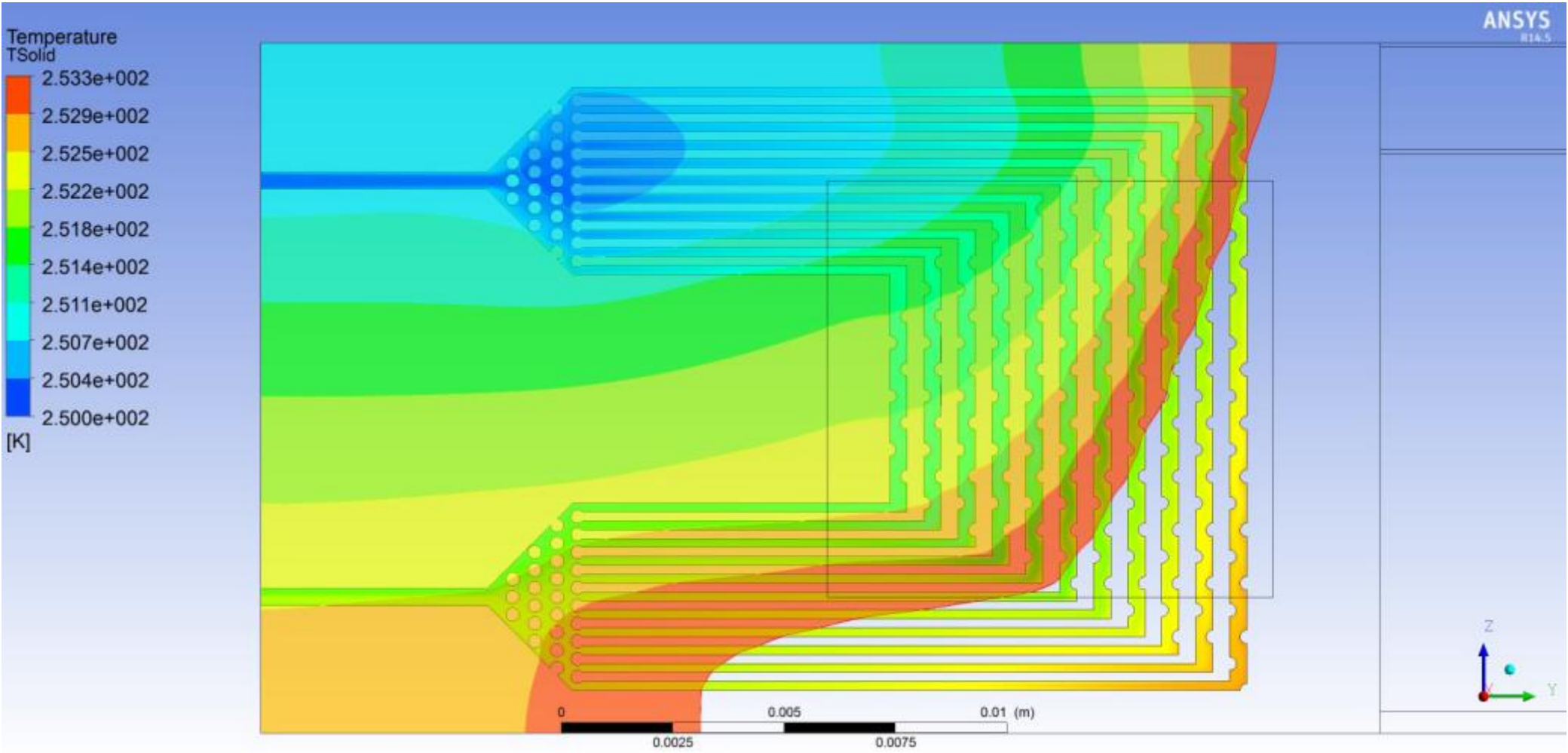
Temperature
TSolid
2.533e+002
2.529e+002
2.525e+002
2.522e+002
2.518e+002
2.514e+002
2.511e+002
2.507e+002
2.504e+002
2.500e+002
[K]
ANSYS
R14.5
0
0.005
0.01 (m)
0.0025
0.0075
Z
Y

CO_2 Case: Simulation

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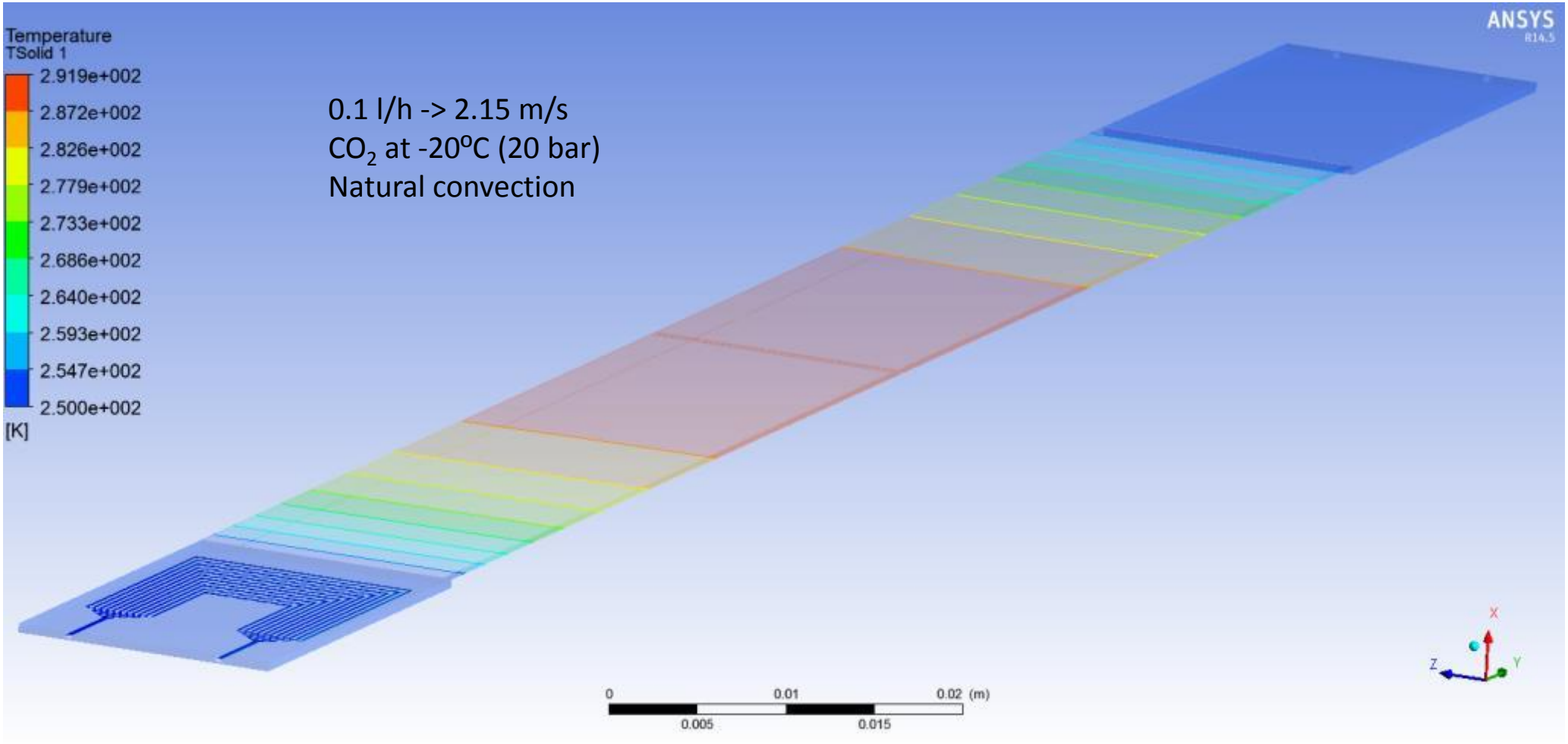
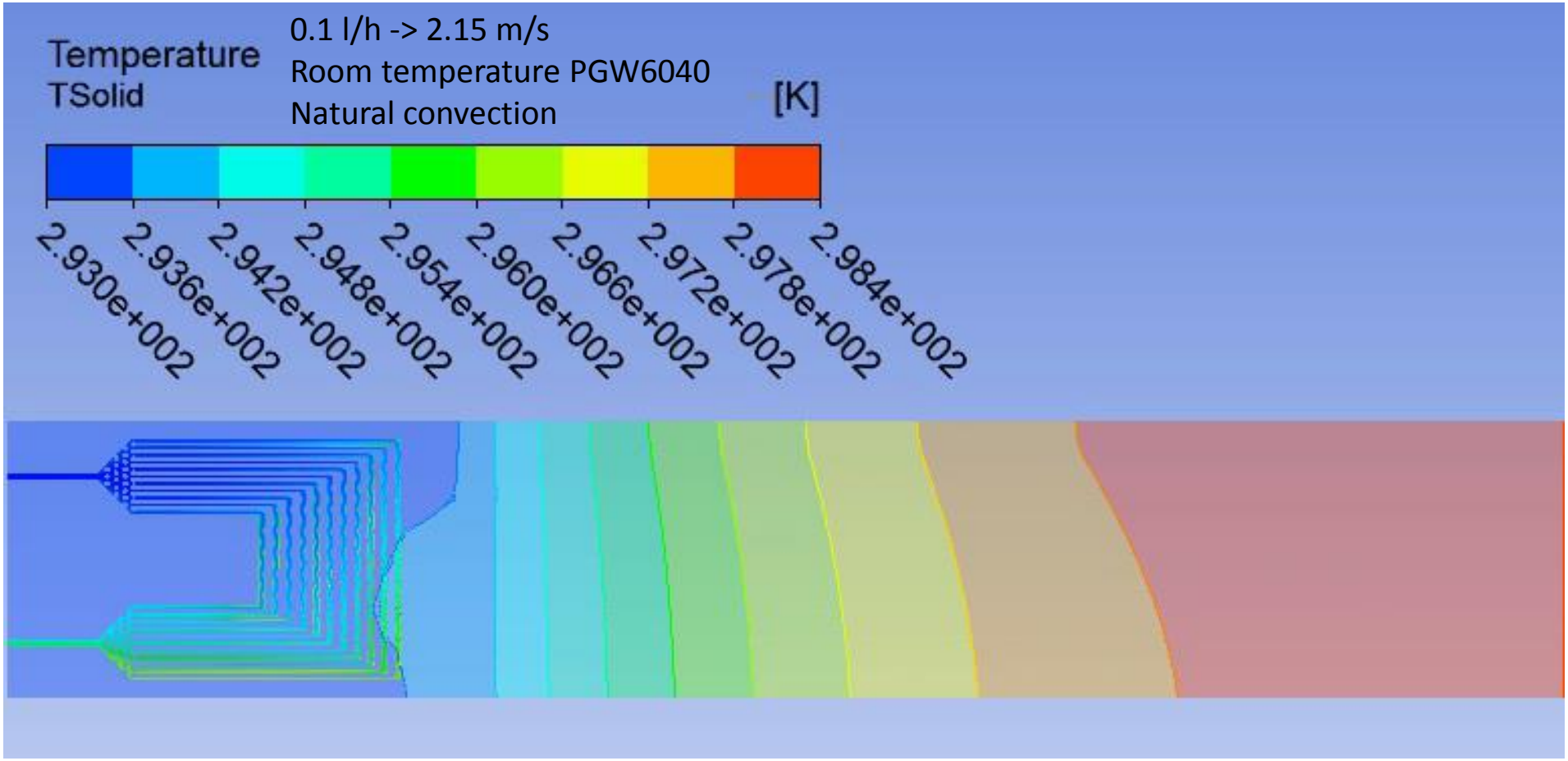
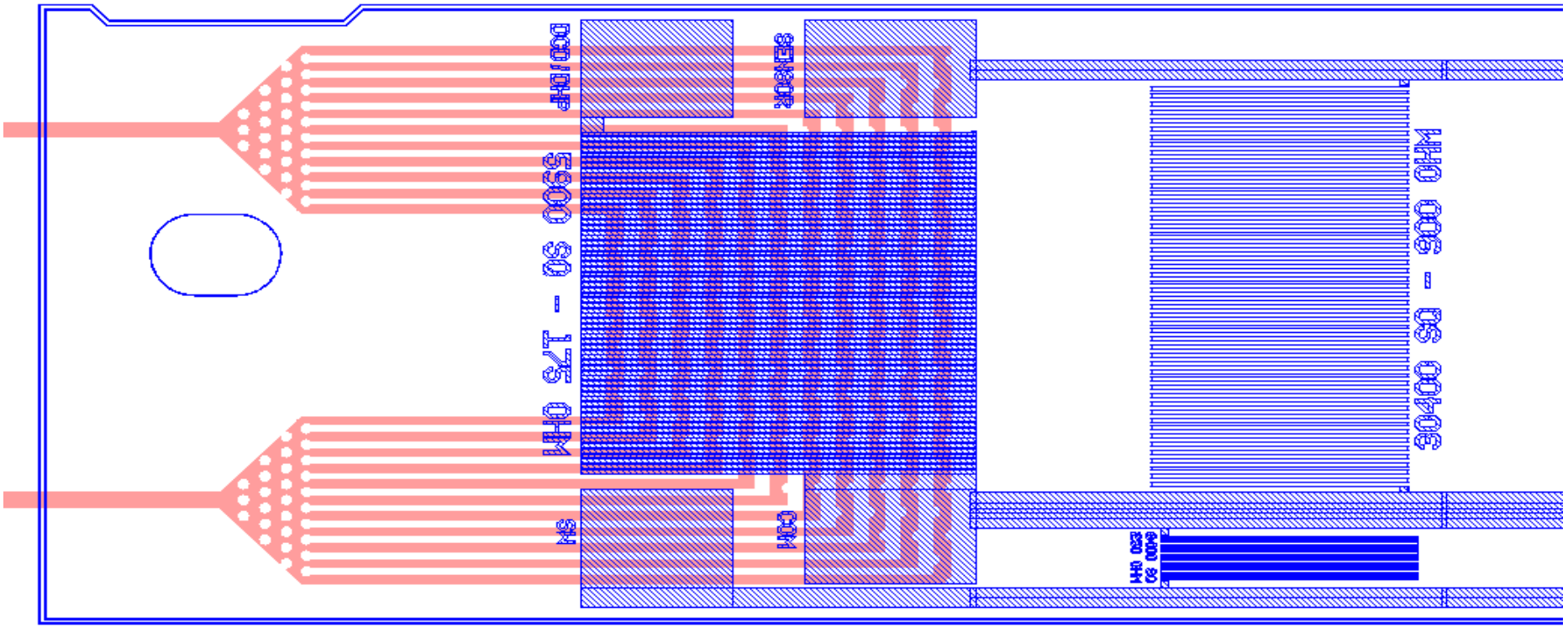


PGW6040 Case: Simulation

PGW6040: 60% Propylene Glycol, 40% Pure Water



Test Vehicle



Aluminum layer with resistor meanders on 75 µm thin top wafer

Starting Point

No heat load on the back!

Start Point

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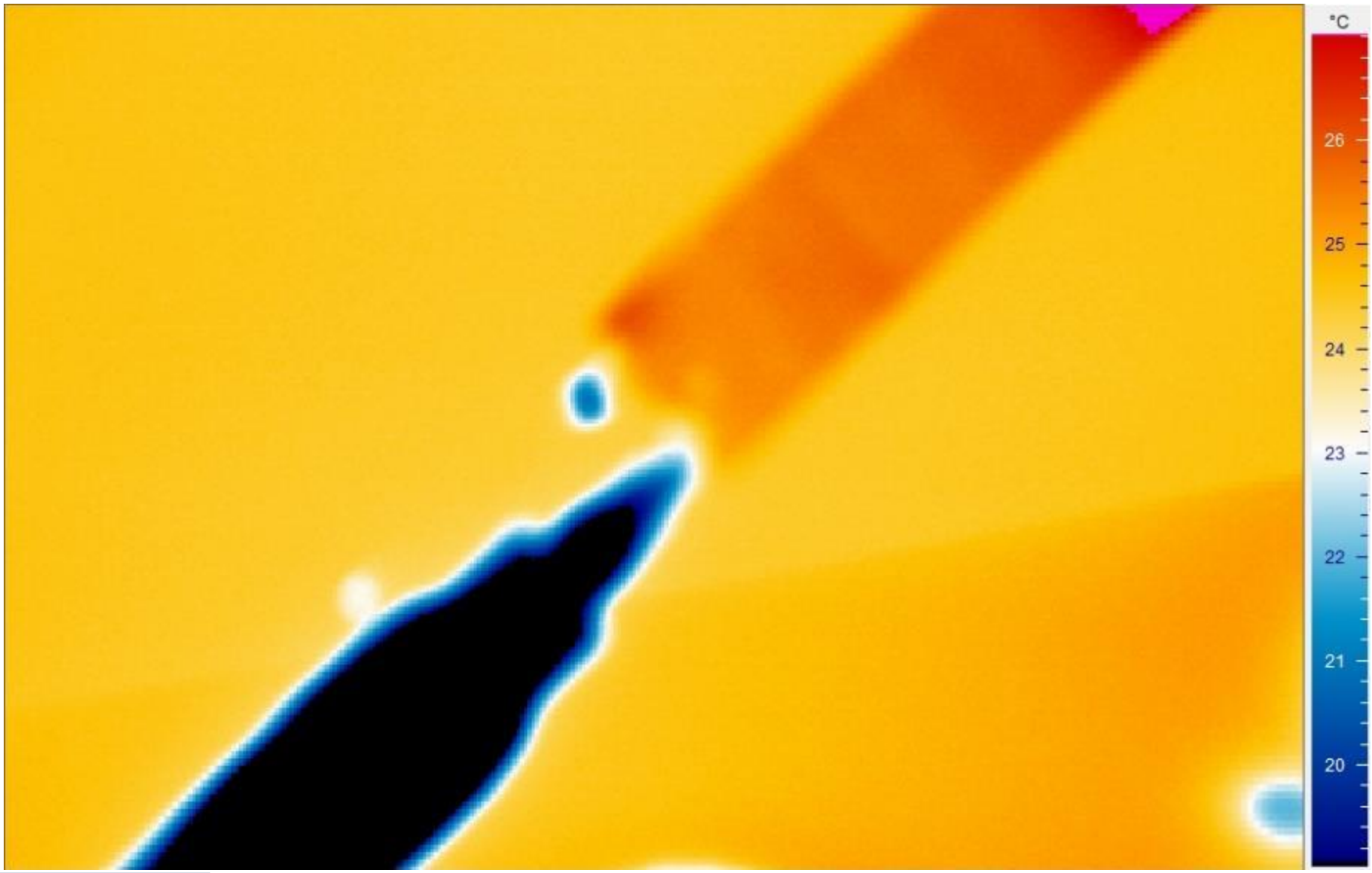

Coolant Flowing

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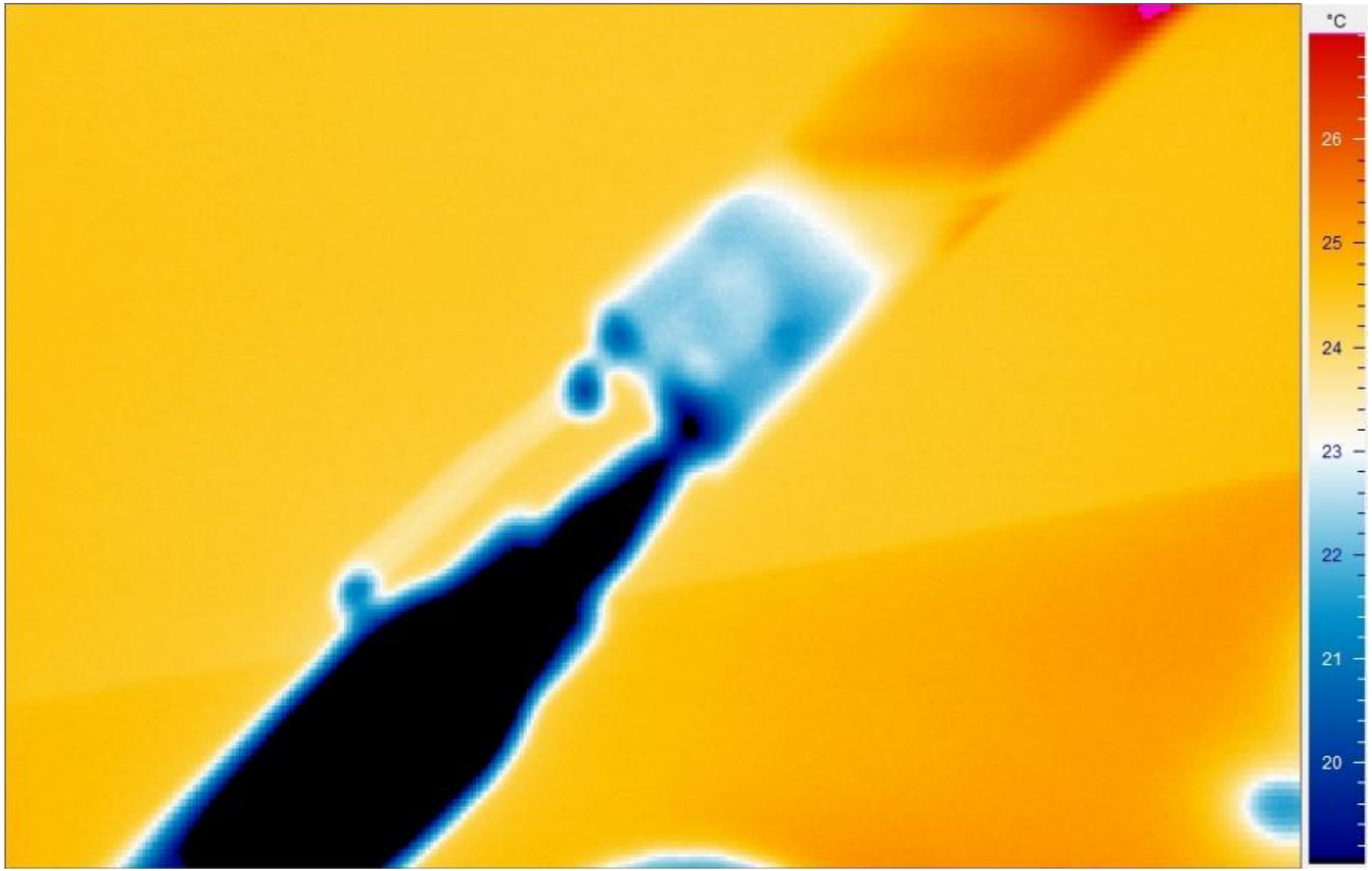

End Point

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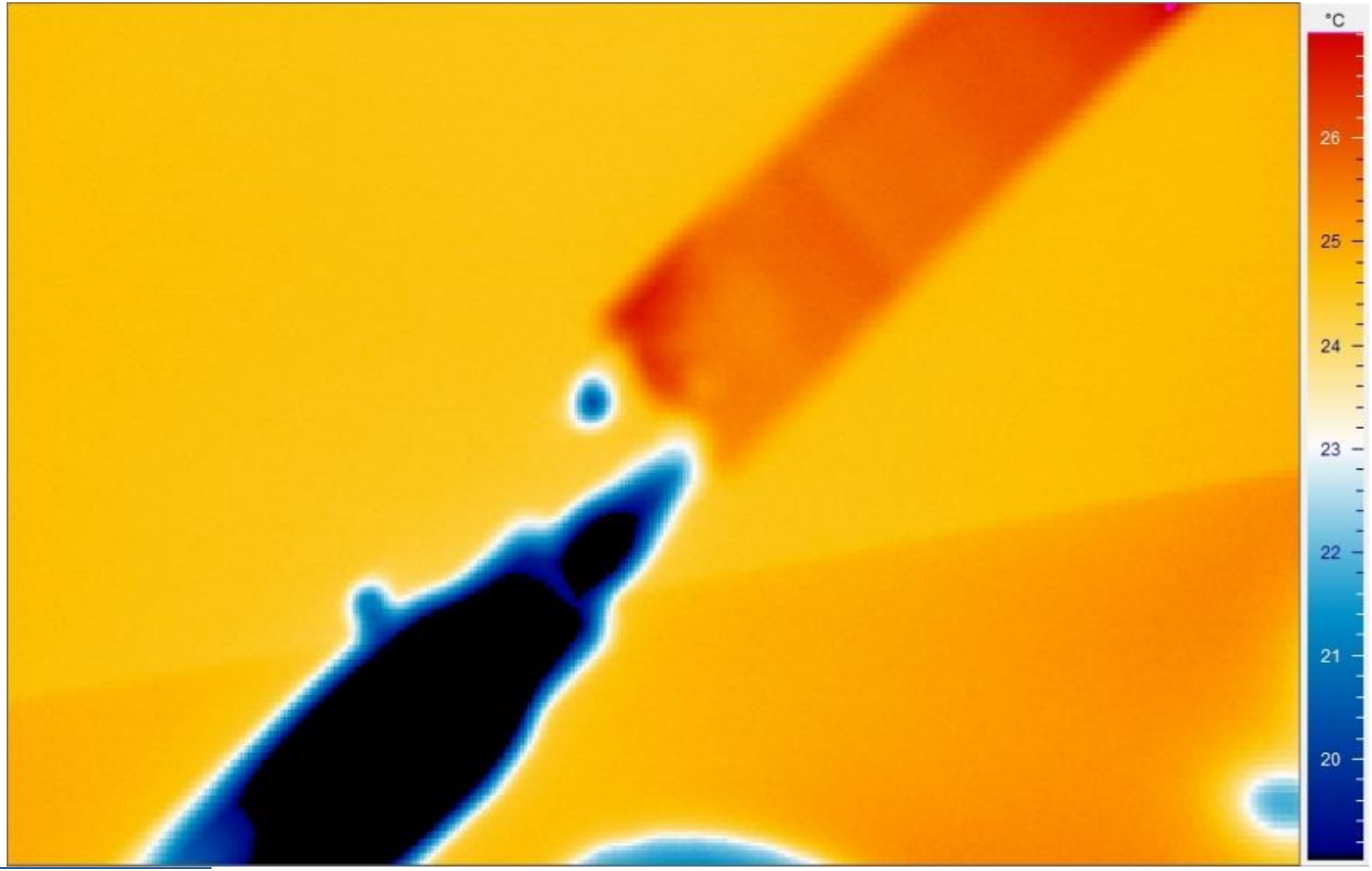
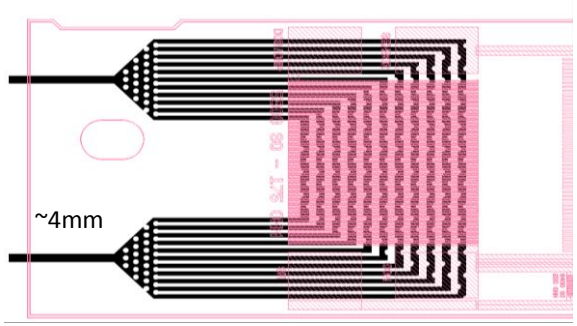
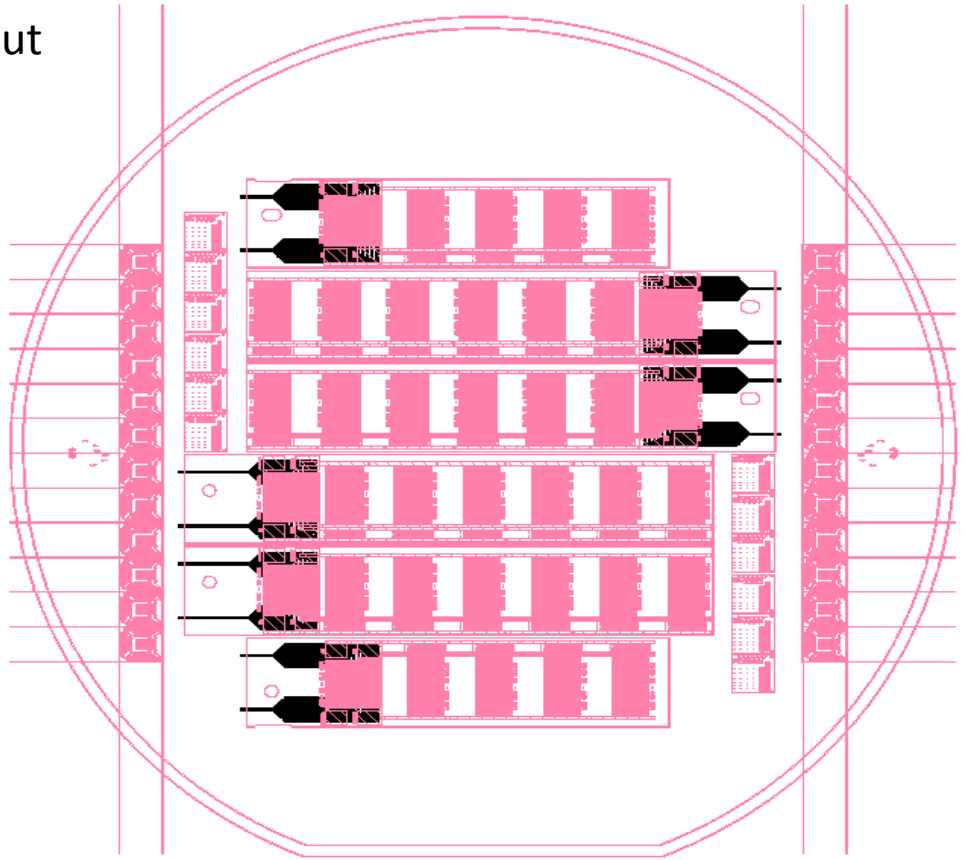
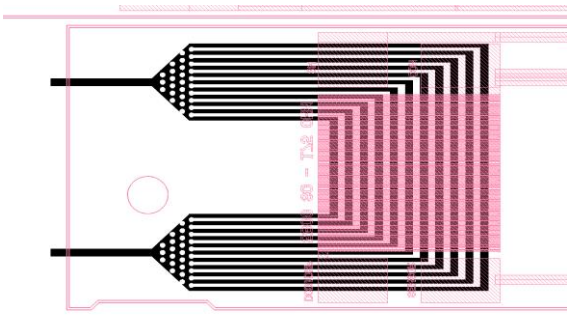


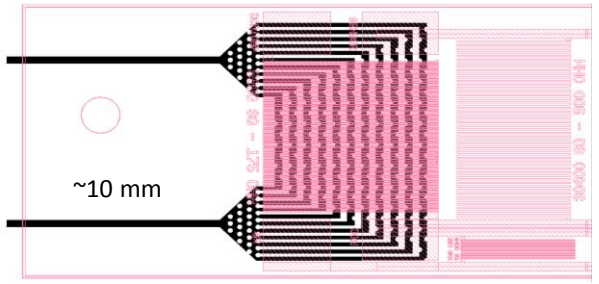
First Prototype Production

- 5 wafers with PXD9 thermal dummy layout
- Various channel geometries
- 1 wafer laser cut
- 4 more wafers before cutting
- Thinning of sensitive region

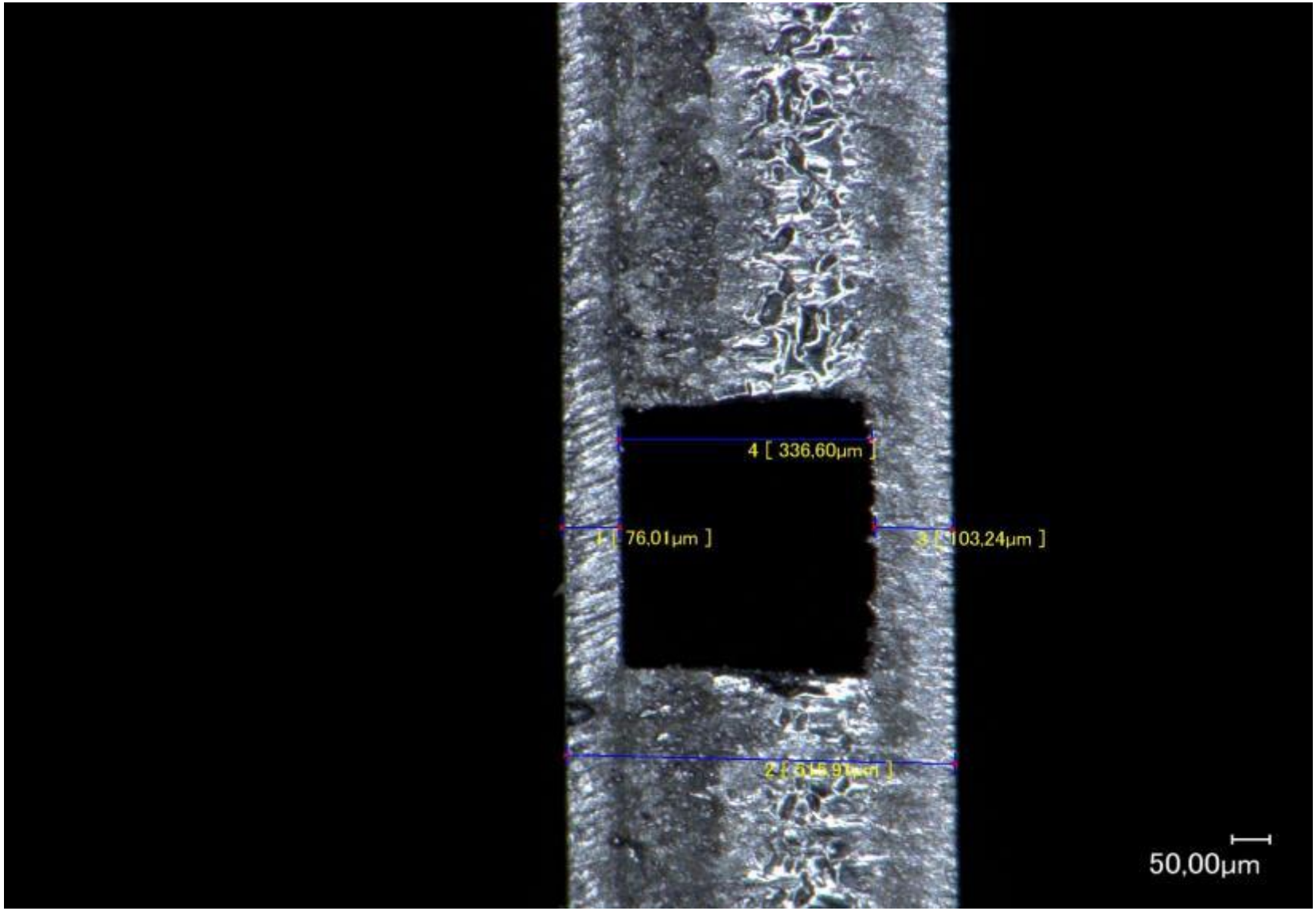




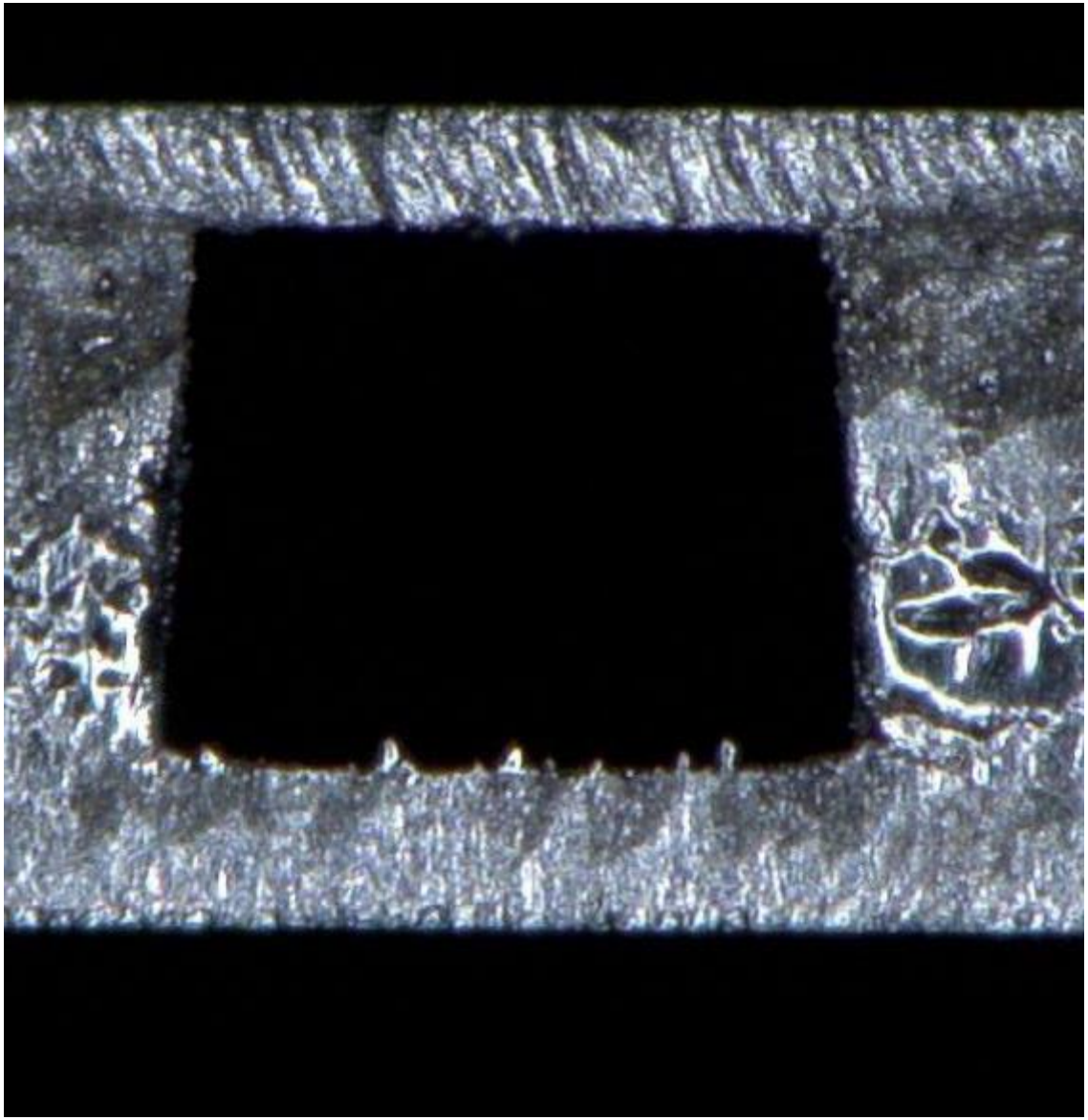




Inlet and Outlet

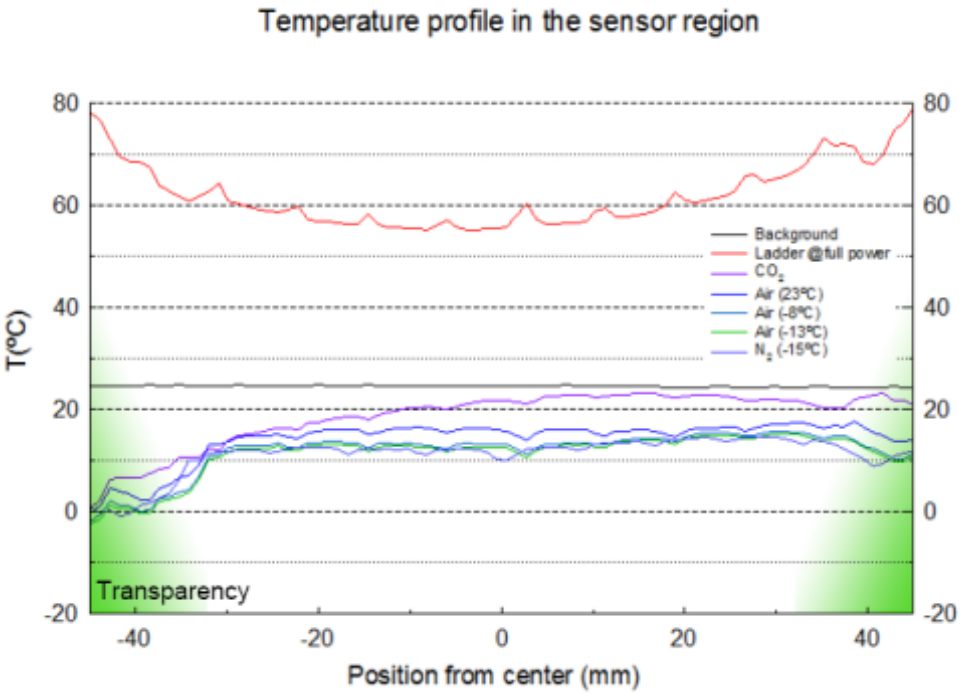


Inlet Detail

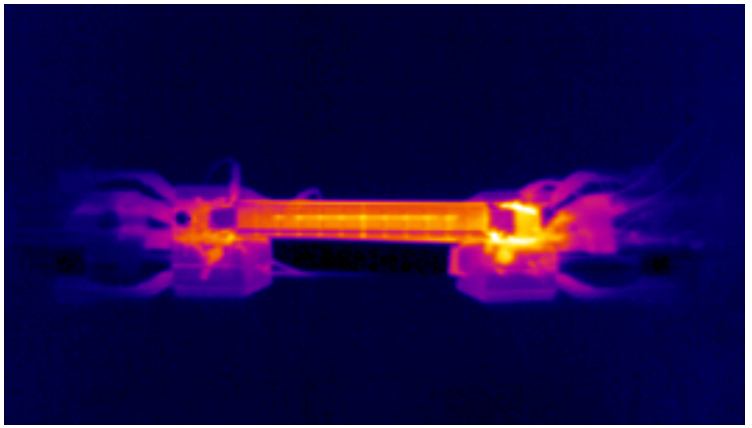


PXD Mockup

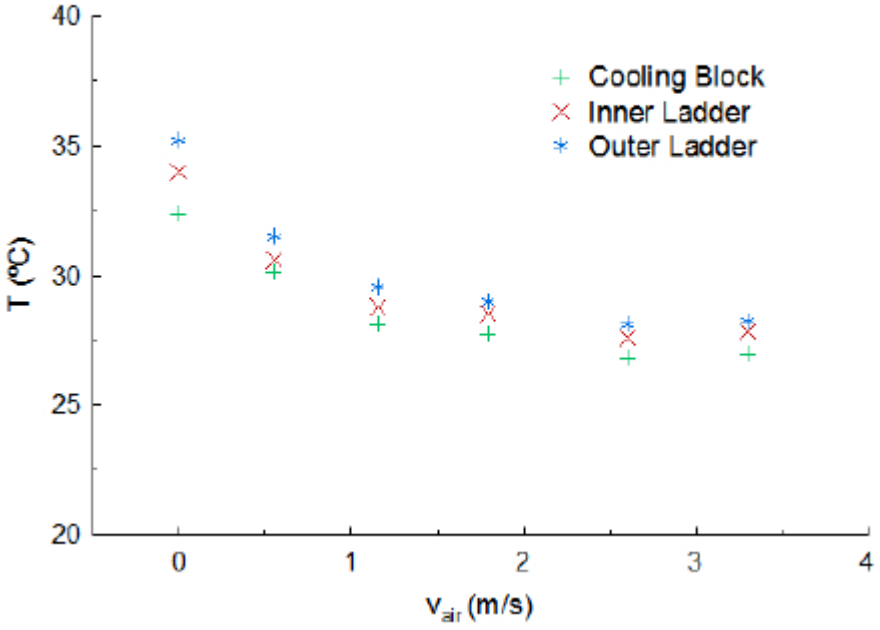
- CO_2 cooling the end of the ladders
- The detector is flushed with cold nitrogen



The results obtained match the simulations



Variation of temperature with air injection speed.



Sensor Deformation

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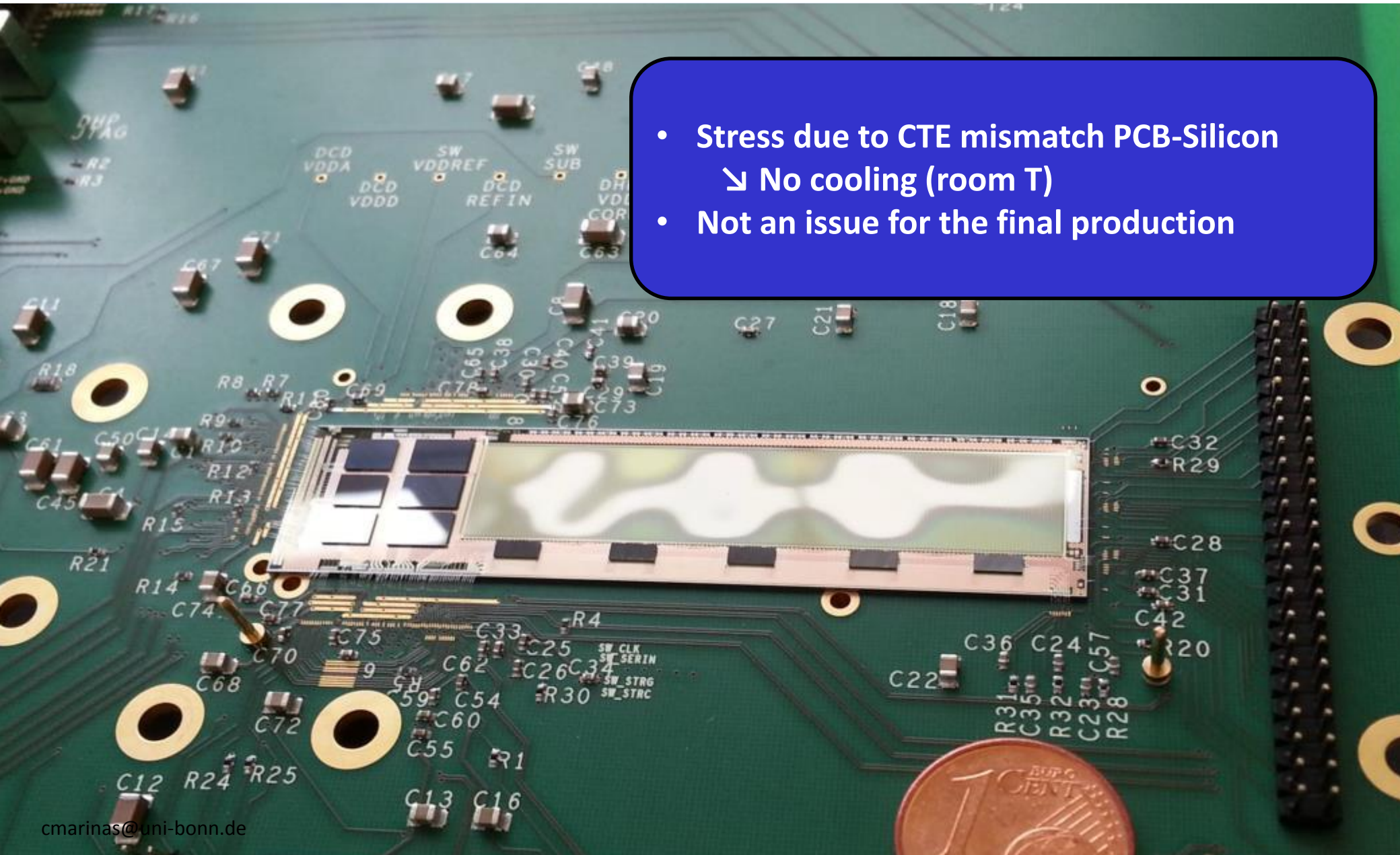

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CO_2 Cooling Plant

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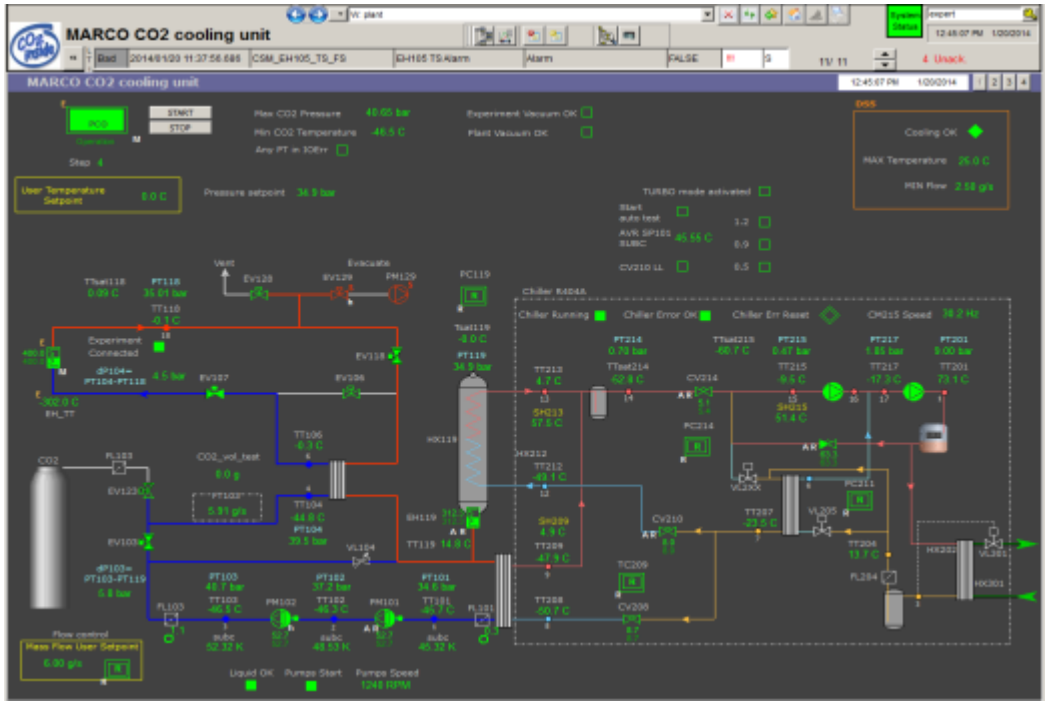

- Connected (only) to the SVD
- Additional close loops with heaters for tuning

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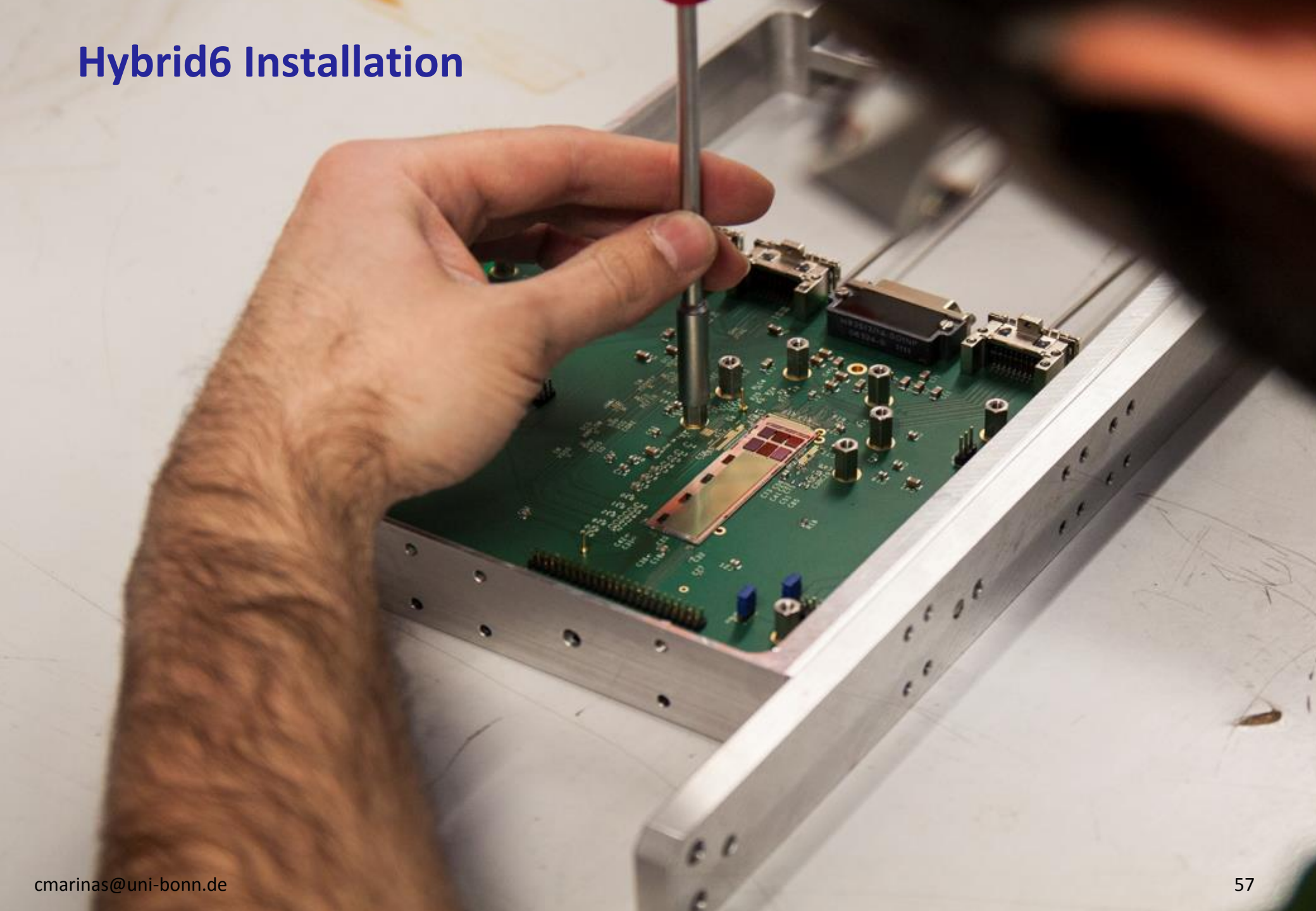
Hybrid6 Installation



TB Cooling Block

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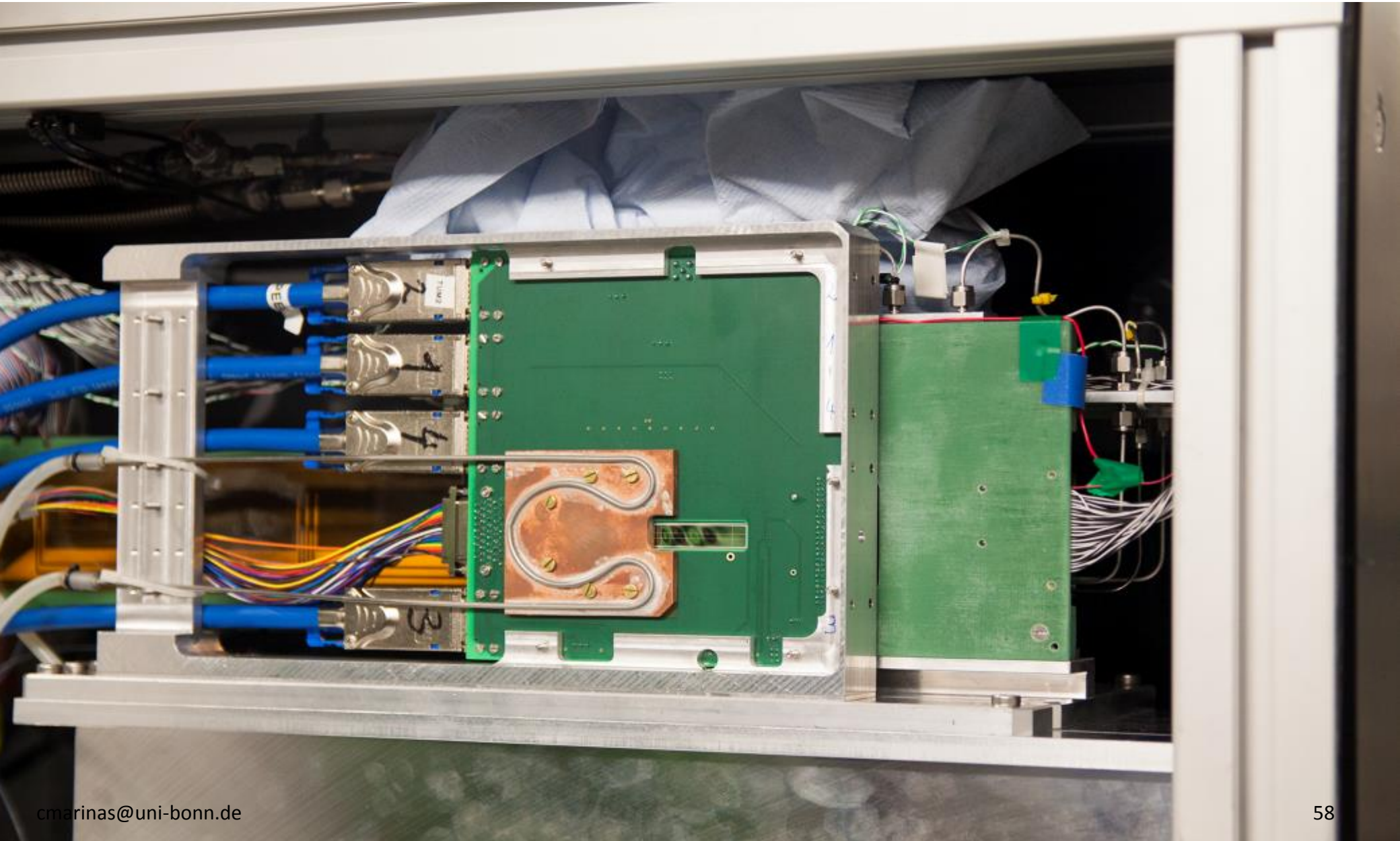
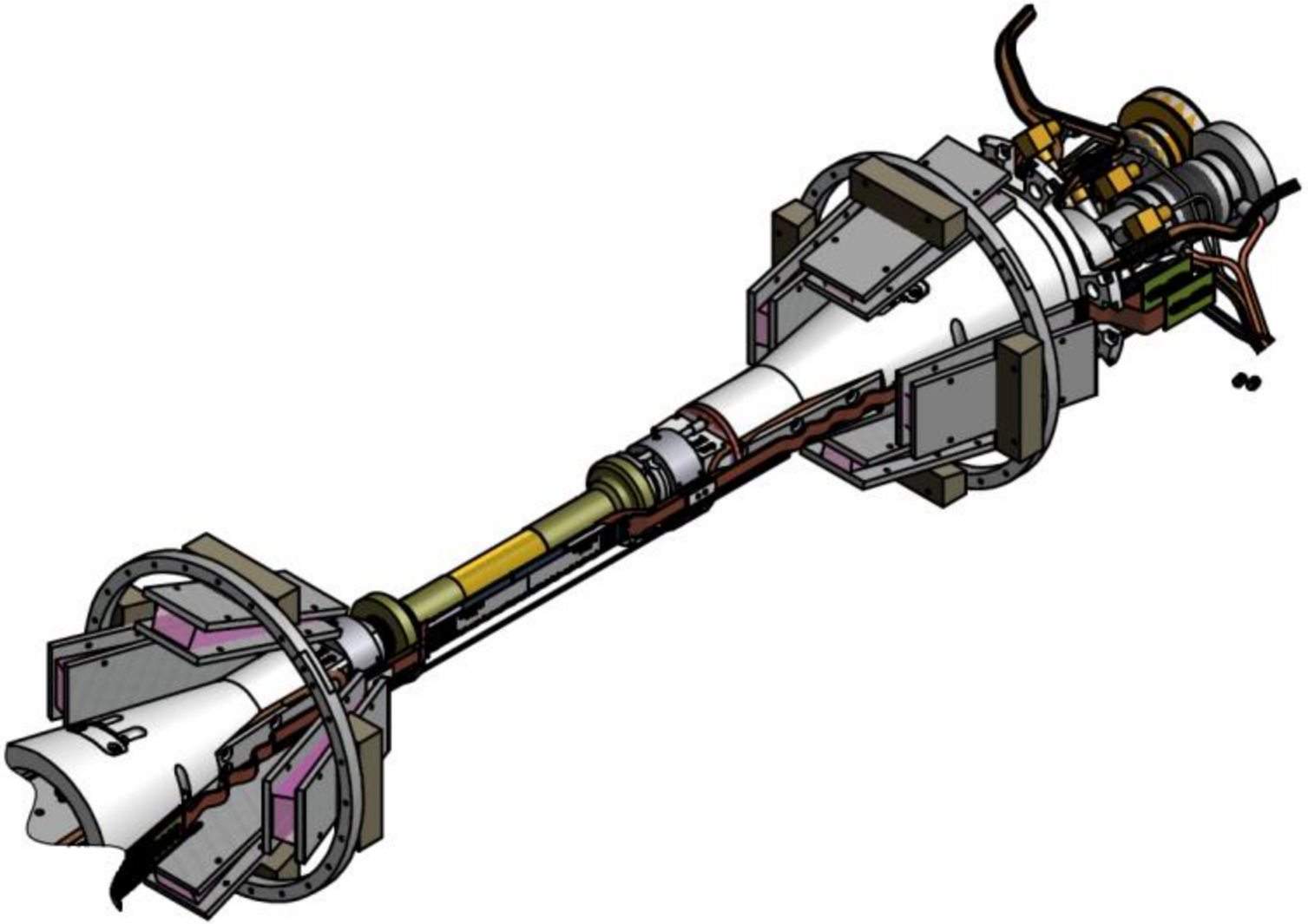
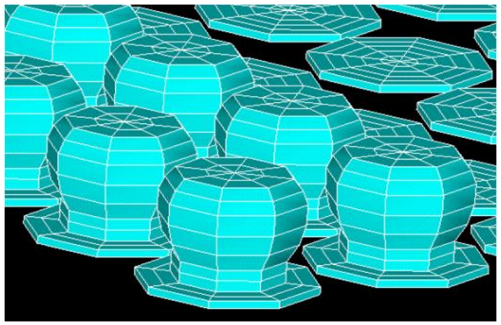


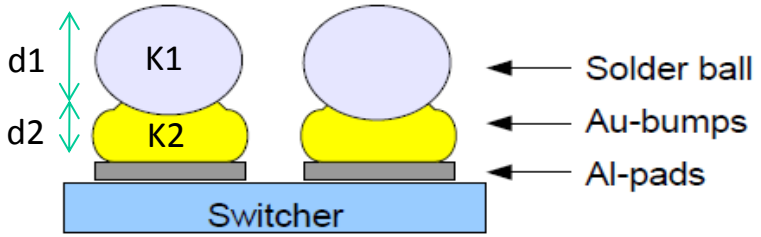


BGA Model simplification

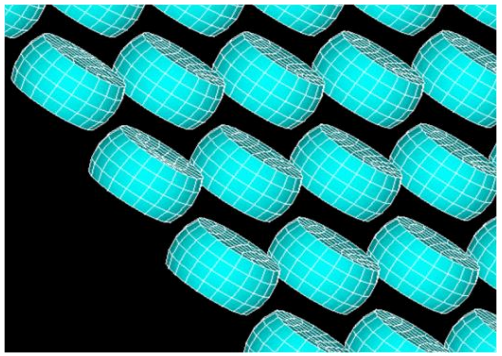


Real life

Time consuming!



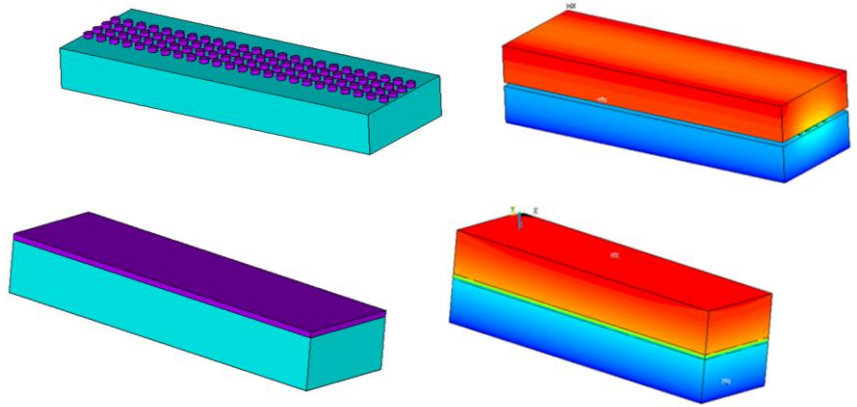
Thermal conductivity weighted by the diameter



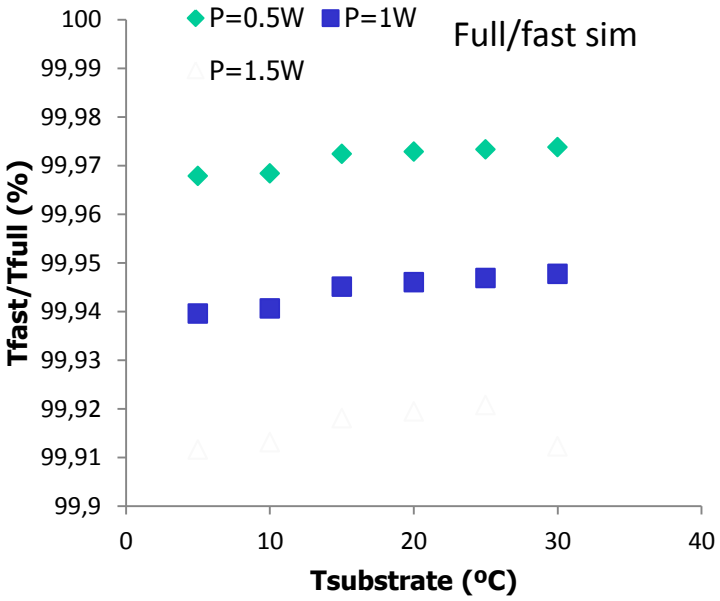
Simple model k_{weight}

$$k_{weight} = 57 \frac{W}{m \cdot K}$$

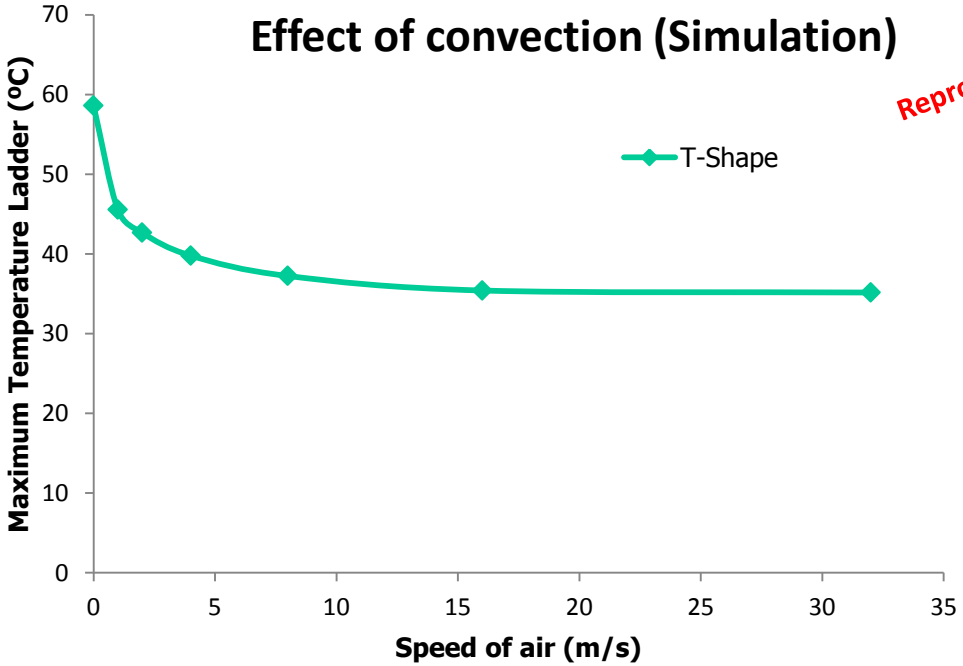
$$k_{eff} = 6 \frac{W}{m \cdot K}$$



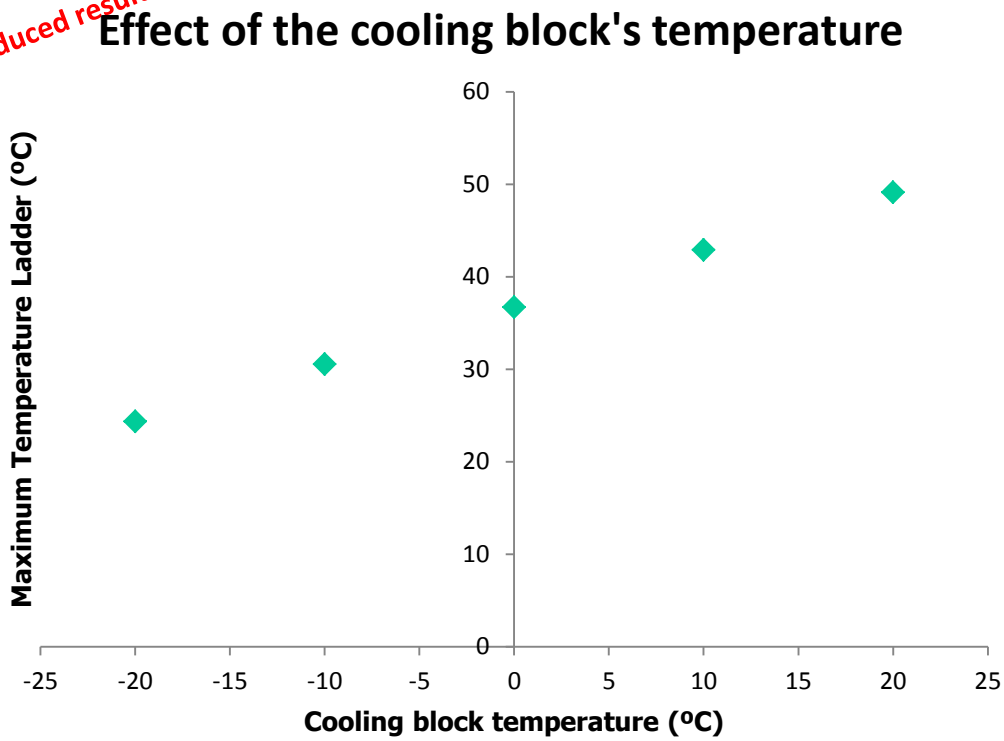
Simplest model implemented in the simulation



Validation of the simulations



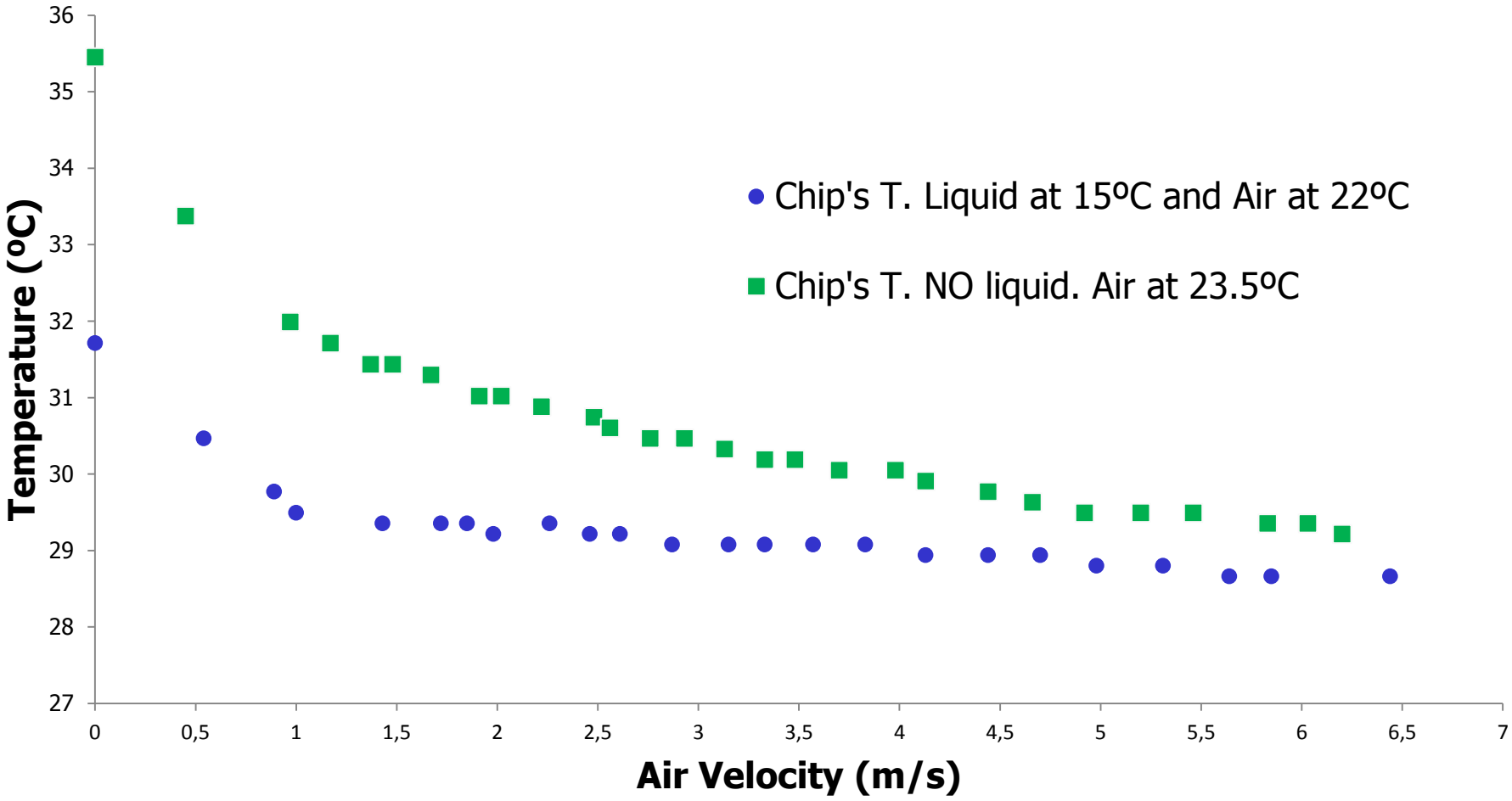
Reproduced results!



- Convection
  - → Air is the best option to cool the center of the ladder
  - → Saturation at high speeds

- Conduction
  - → No big influence in the center
  - → Needed to prevent the DCD heat to enter into the sensitive region

Influence of Convection



- The air flowing is an effective mechanism to cool the center of the module
- Once the air is blowing, the T varies slow, independently of the speed (at this range).

ILC Beam structure

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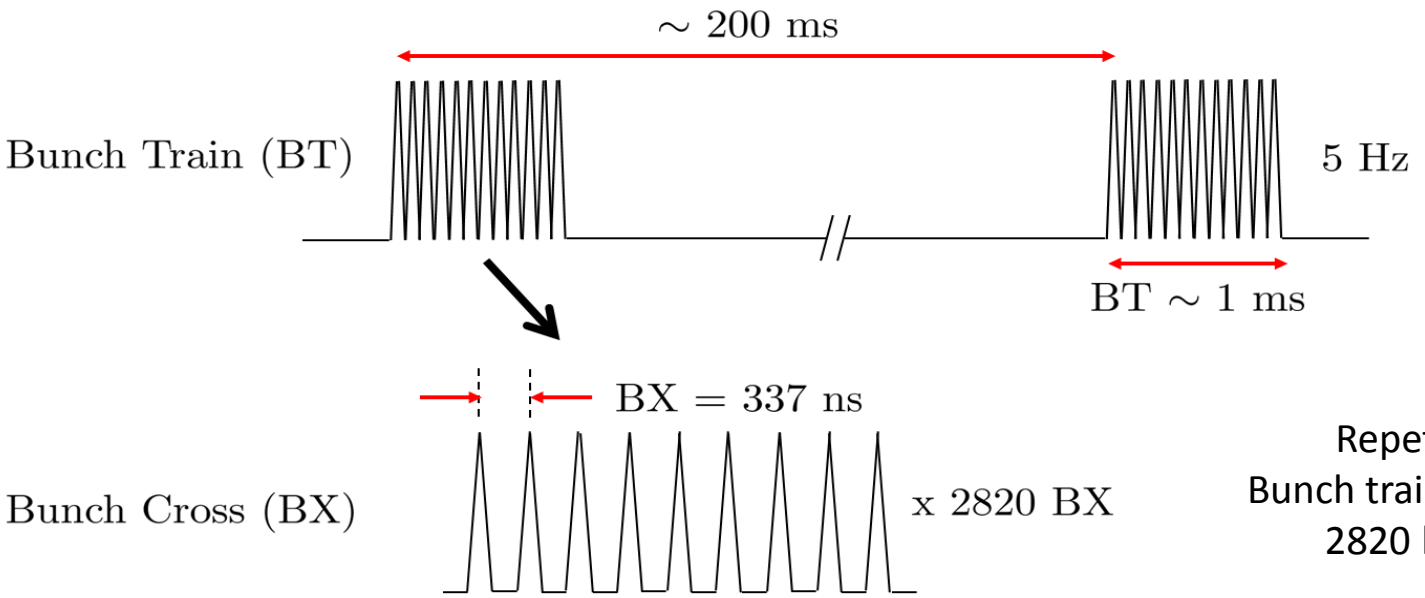
- *<u>WARNING</u> the design is strongly correlated to the beam time-structure*

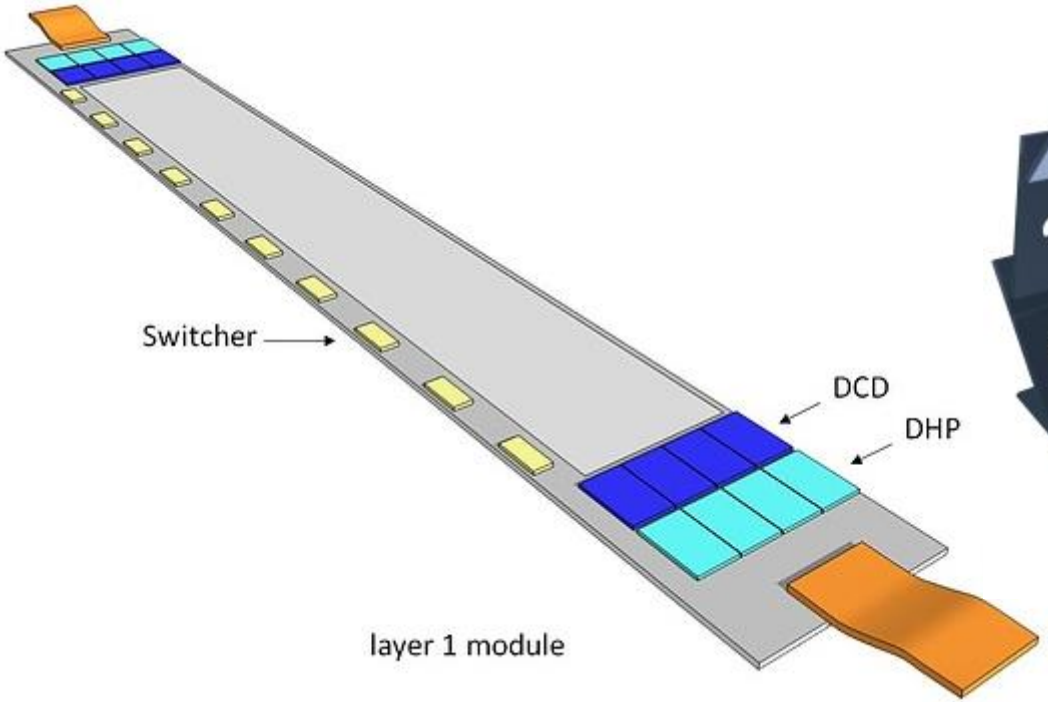


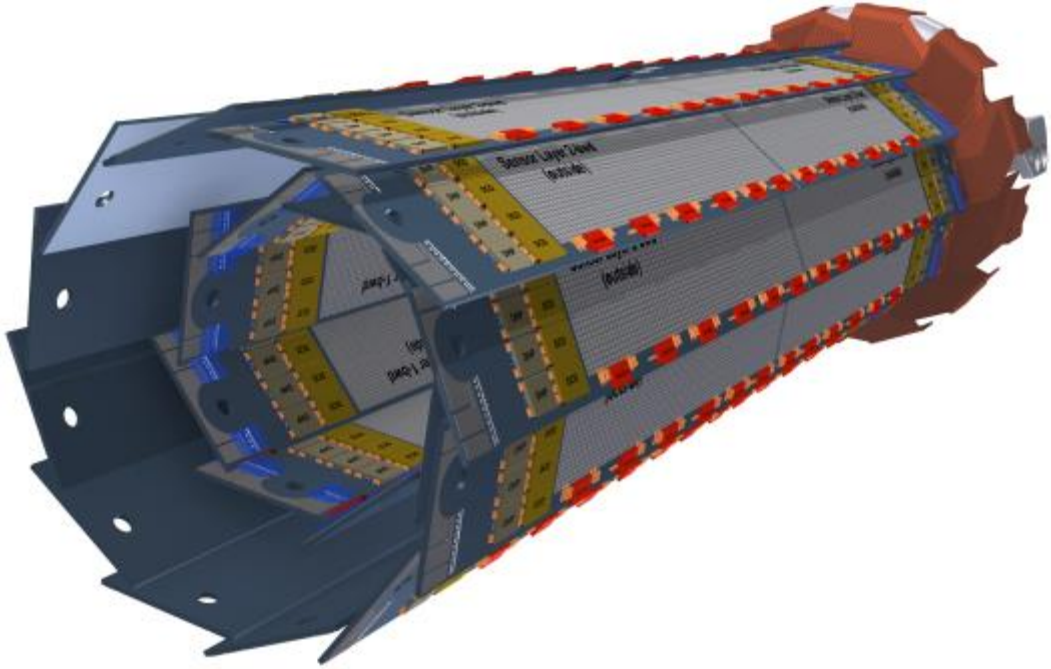
Repetition rate of 5Hz
Bunch train of 1ms every 200ms
2820 bunches per train

➢ Impact on the Vertex Detectors:

- Beam structure allows for power pulsing
  Switching of the detectors between bunch trains (power cycling)
  → Air cooling → Minimal material budget
- Bunch disambiguation
  Readout not possible in 337ns → Time slicing instead of time stamping

Belle II Cooling strategy





- The material budget must be minimal, no active cooling is allowed inside the acceptance
- The major amount of heat is dissipated in the readout chips, at both ends of the ladder
- The most straightforward solution:
  - Massive structures outside the acceptance to cool down the readout chips
  - The center of the ladder must be cooled using cold air