ATLAS HL-LHC Tile Calorimeter Upgrade

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on behalf of the ATLAS Tile calorimeter system

ACES 2014

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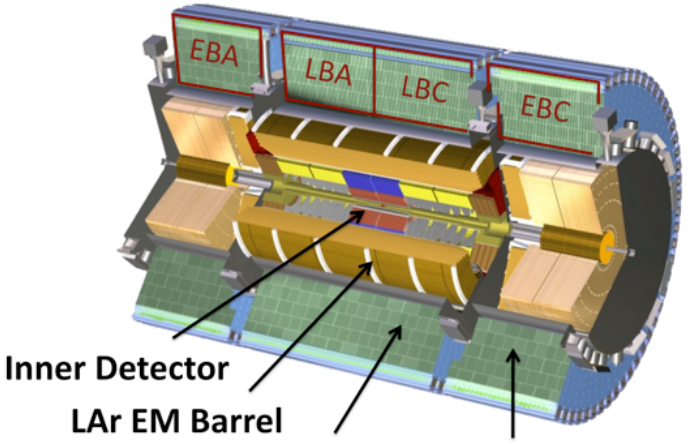
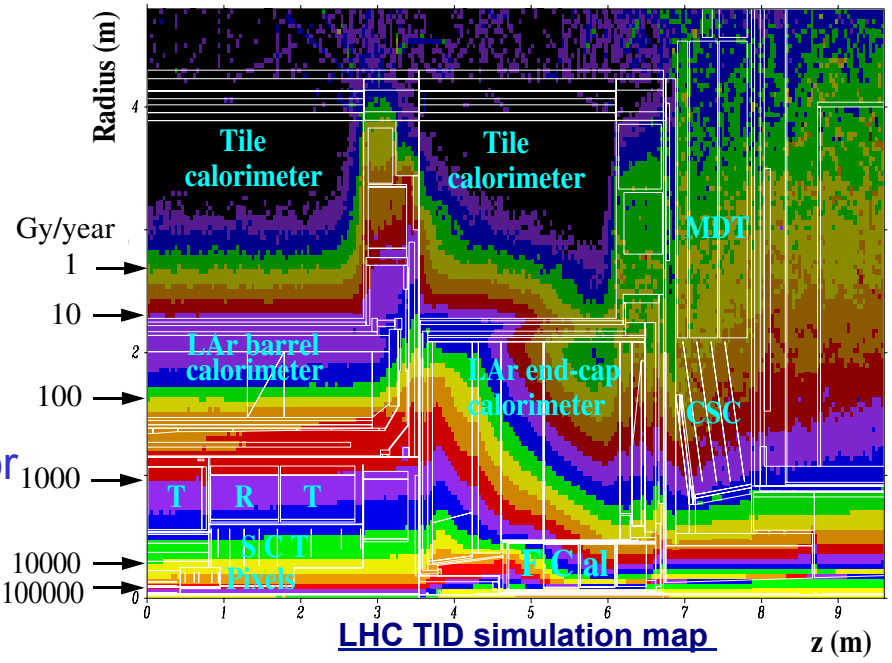
Upgrade of the Tile calorimeter

- Performance of the Tile calorimeter during LHC Run 1 has been excellent
  - Read-out electronics at full potential despite the amount of LVPS trips
  - Radiation damage only on most exposed scintillators (Gap/Crack and MBTS)
- Phase - 0 upgrade (2015)
  - Refurbishment of on-detector readout electronics
  - New low voltage power supplies
  - Improvement of Laser and Cesium calibration systems
- Phase - I upgrade (2019)
  - D-Layer muon trigger
  - Replacement of gap and crack scintillators
- Phase - II upgrade (~2024)
  - Major replacement of on- and off-detector electronics
  - New active HV dividers for the PMTs

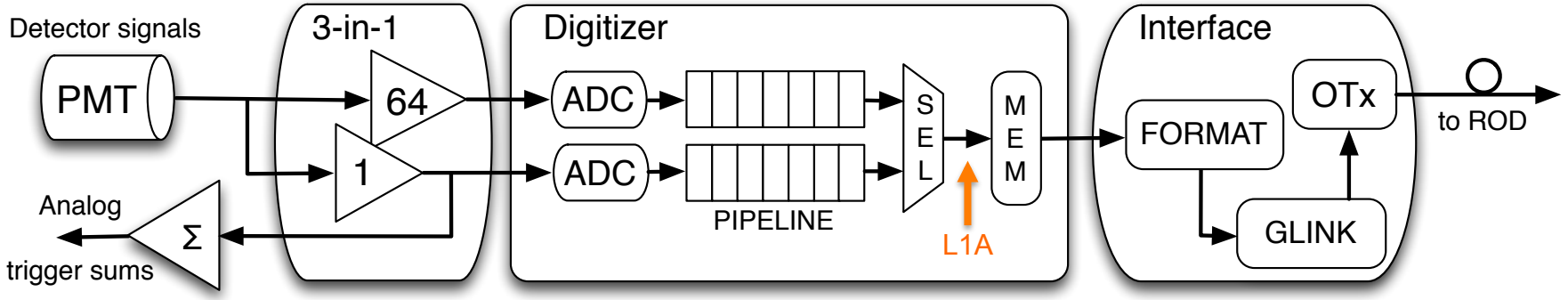




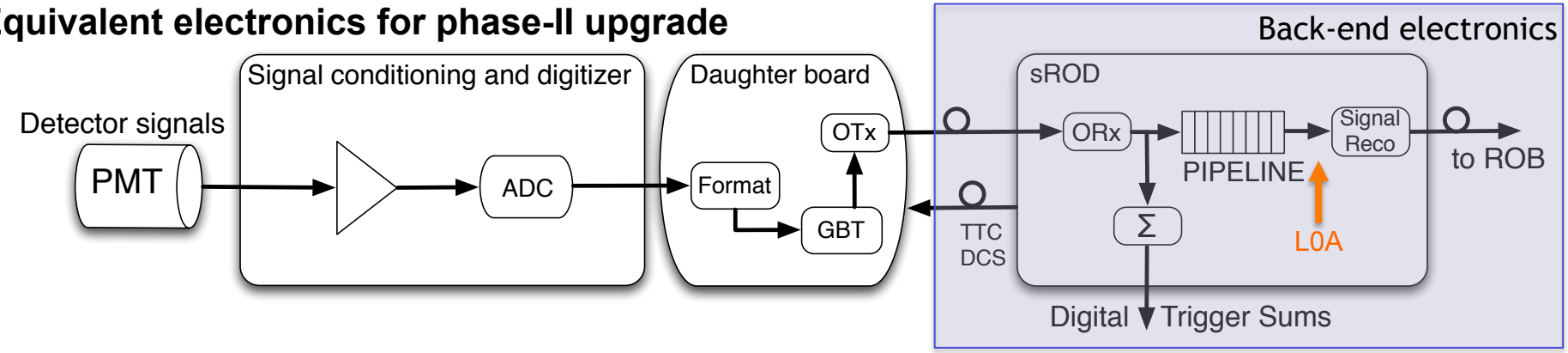
LHC TID simulation map

Phase-II upgrade

Present front-end electronics



Equivalent electronics for phase-II upgrade

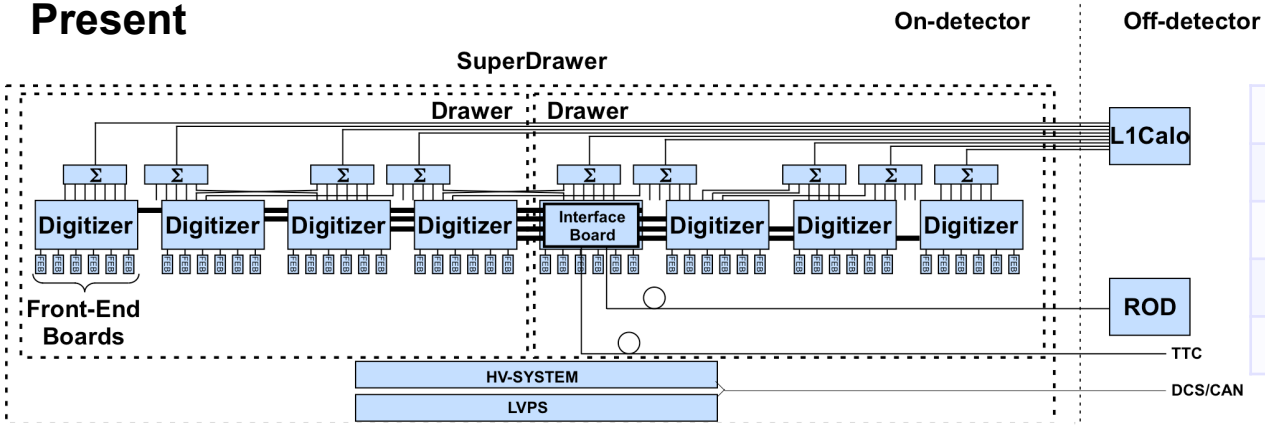


- Tile's plans for the upgrade phase-II of the LHC are to completely replace the front-end and back-end electronics introducing a new read-out strategy
  - Full digitization of signals at BC rate and transmission to off-detector electronics
  - Reduction of single point failures
  - Digital input to trigger Levels 0 and 1

Changes in the electronics

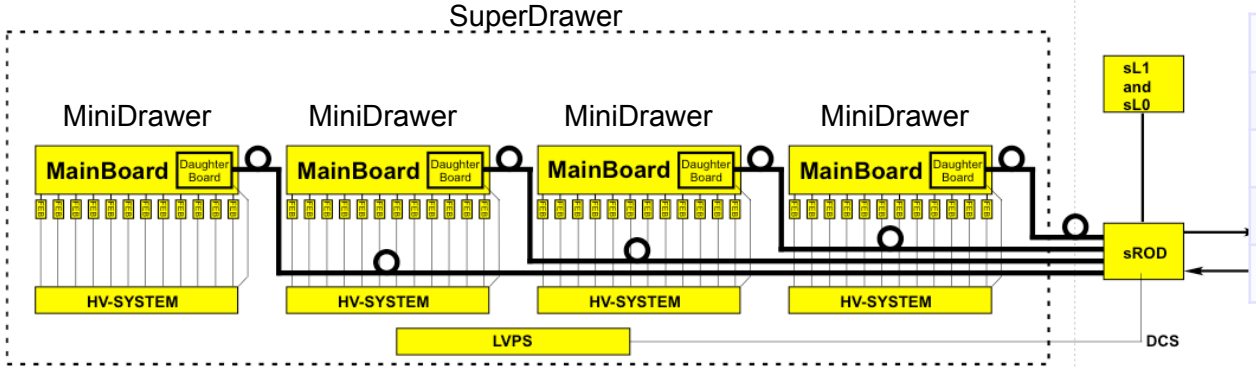
- Aim to cope with luminosity increase and reduce single point failures (improve reliability)
  - **Fewer failure-prone connectors** with the challenge of routing **more fiber optic and LV cables**
  - **Smaller DAQ elements** by introduction of mini-drawers
  - **Increase the redundancy in the read-out path** from the cell to the backend
  - Similar **redundancy in the power distribution** and introduction of Point-Of-Load regulators

Present



Total data rate	~165 Gb/s
Number of links	256
Data rate per link	640 Mb/s
Links per super-drawer	1 (+1)
Data rate per super-drawer	640 Mb/s

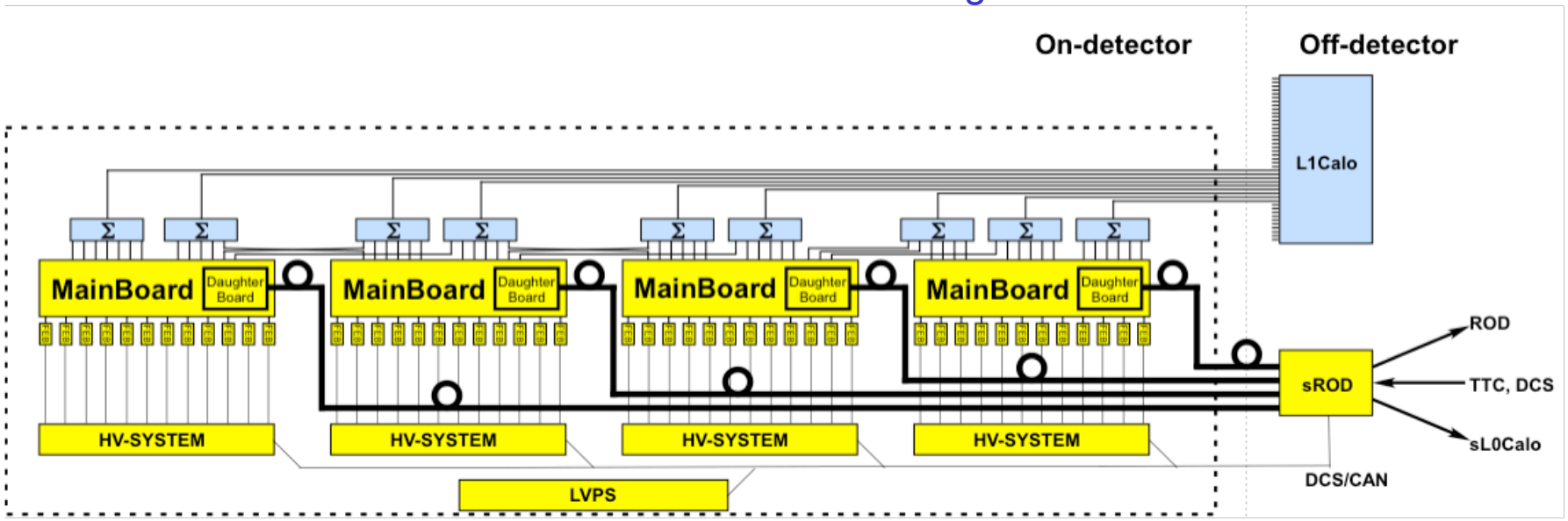
Proposal for phase-II



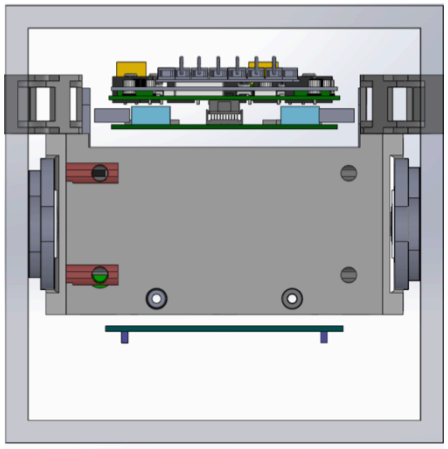
Total data rate	~40 Tb/s
Number of links	4096
Data rate per link	10 Gb/s
Links per super-drawer	4x4 (+4x4)
Data rate per super-drawer	160 Gb/s

Hybrid demonstrator

- In order to test the technology for phase-II upgrade we are developing a **hybrid demonstrator** slice containing the new components but **compatible at the functional level with the current design**
  - Redundancy against SPF
  - Radiation tolerance up to 100 kRad
  - Error correction and triple redundant designs
  - Sampling and read-out in all BCs
  - Precision of 16 bits above noise level in two 12 bit gains



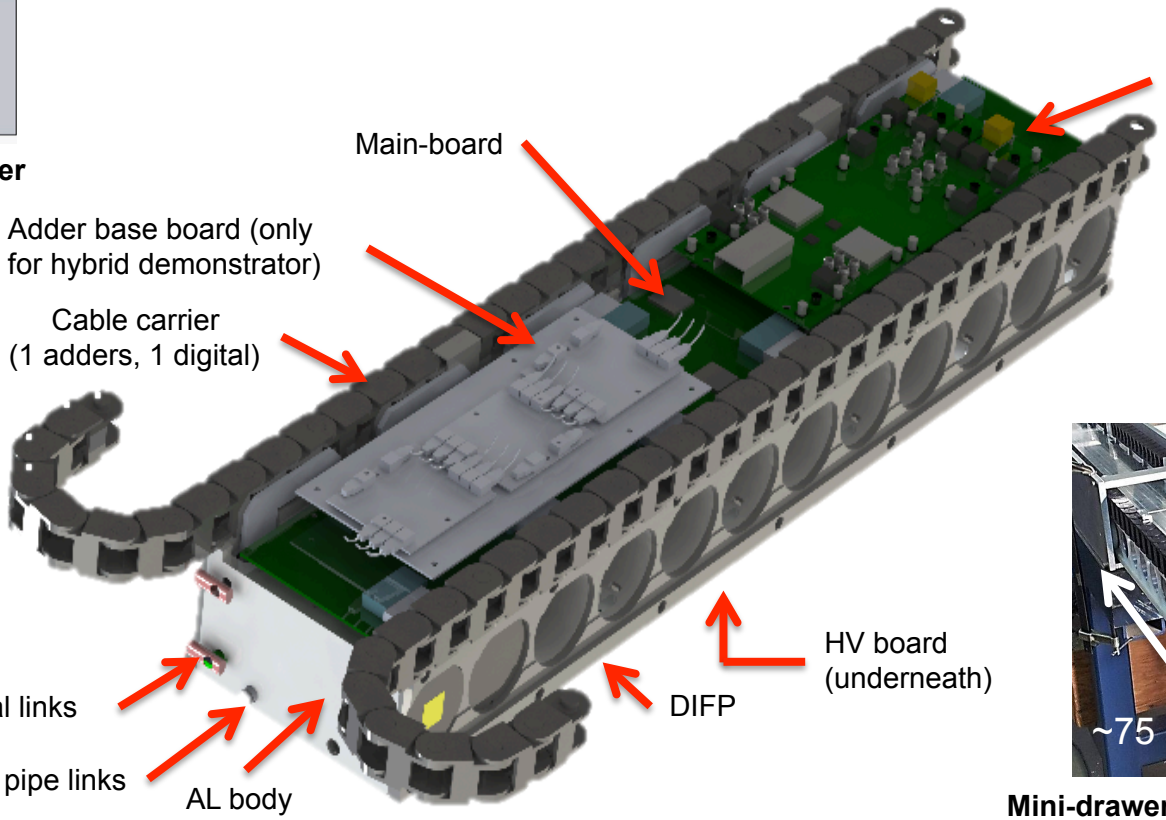
Mini-drawers

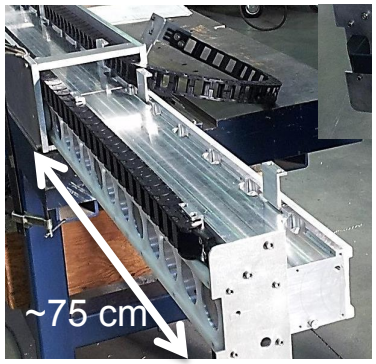


Cross section of a mini-drawer

- Super-drawer demonstrator will be composed of 4 mini-drawers, each one containing
  - 12 front-end boards: 1 out of 3 different options
  - 1 main-board: for the corresponding FEB option
  - 1 daughter-board: single design
  - 1 HV regulation board: 1 out of 2 different options
  - 1 adder base board + 3 adder cards: for hybrid demonstrator

Required assembly of 45 PMT blocks with new active dividers

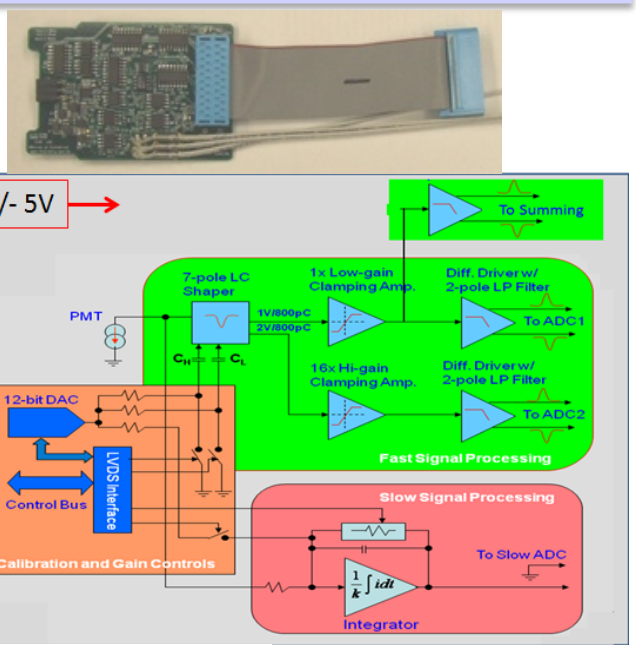


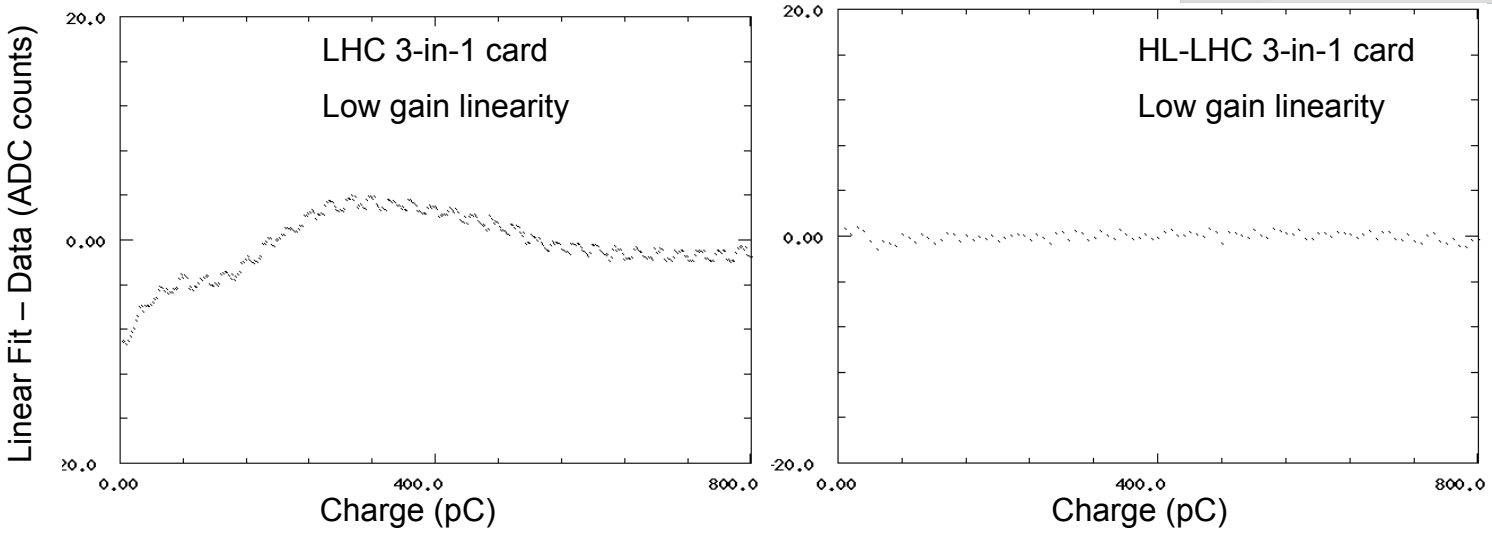


Mini-drawer with cable carriers

Front-end board option 1: New 3-in-1

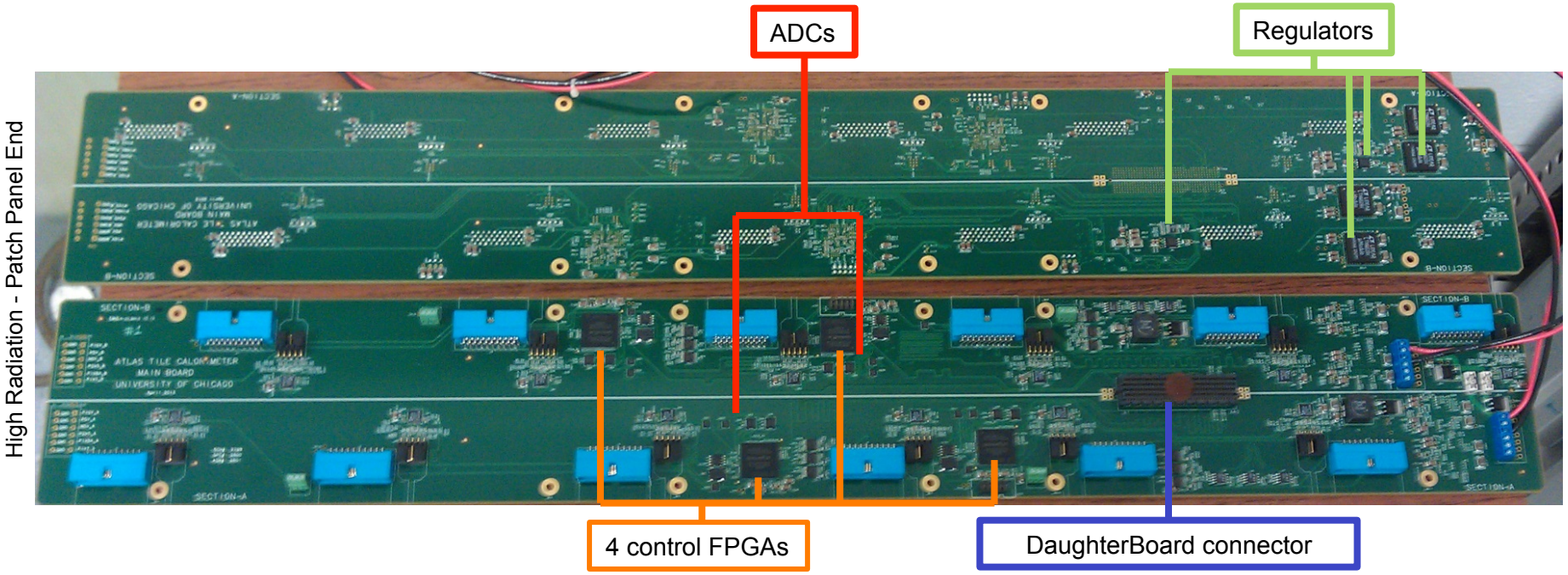
- Based on current 3-in-1 cards that provide 3 functionalities
  - Analog output in two different gains with different ratio than before (1:32 as opposed to 1:64)
  - Charge injection calibration
  - Integrator read-out for dedicated and in-physics calibration data
- HL-LHC design requires improved radiation tolerance and better performance
  - One component failed radiation test for sLHC, reverted to previous
- Produced and tested first ~100 cards, started assembly of new PMT blocks





This option will be used in the hybrid demonstrator since it can provide the analog output to the present Level 1 trigger

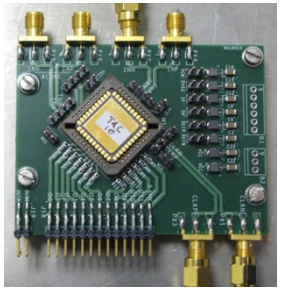
Mainboard for new 3-in-1 FEBs



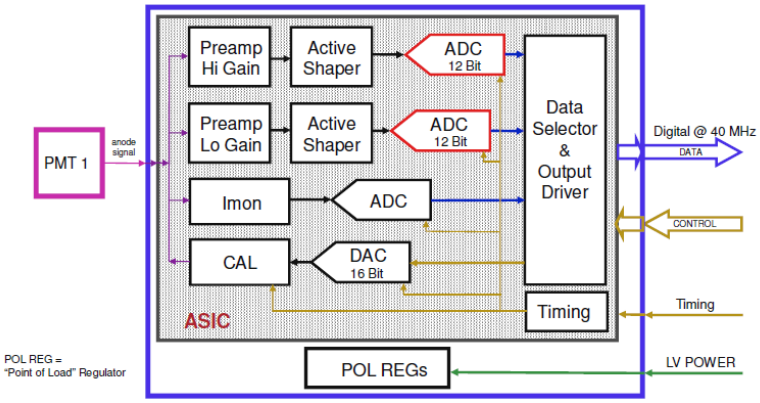
- Mainboard digitizes signals from FEBs with independent discrete ADCs
  - Mainboard is split into two halves
  - Each cell will be read-out by two PMTs, one on each side of the mainboard
  - Samples are transferred serially to the daughterboard at 600 MHz
  - Commands are sent in parallel to 2 control FPGAs on each side
- This front-end board + mainboard option will be evaluated together with the other two in test beams starting in 2015

Front-end board option 2: FE-ASIC

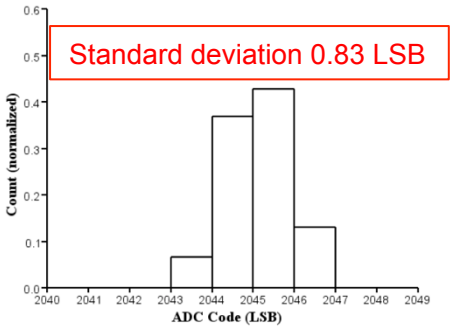
- Second option for a front-end board is based on an ASIC using IBM CMOS 130 nm technology
- FATALIC ASIC provides shaping in 3 gain ranges (1,8,64)
  - Third version being tested
- TACTIC ADC is a 12-bit ADC@40 MHz
  - First version delivered in January
  - Low power consumption 61 mW
  - Measured noise smaller than one LSB
  - Bad integral non linearity due to bad coupling of amplifier capacitors
  - Second version needed
- Next steps
  - Design front-end board with FATALIC and TACTIC for spring 2014
  - Design of fourth version of FATALIC with 3 TACTIC ADCs embedded by May 2014 for delivery by November 2014
  - Design of Mainboard for this Front-end board option

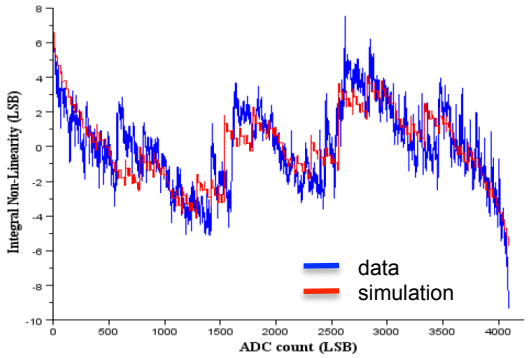


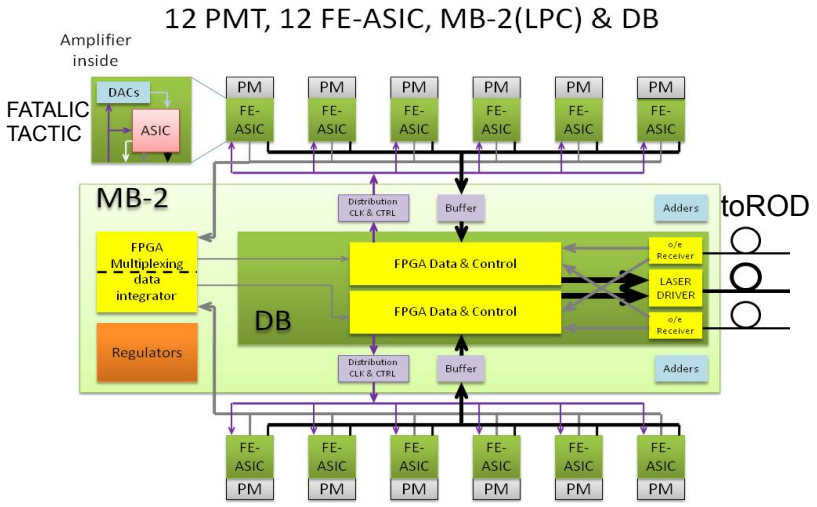
TACTIC ADC



Conceptual Design of FE-ASIC Front-End Board

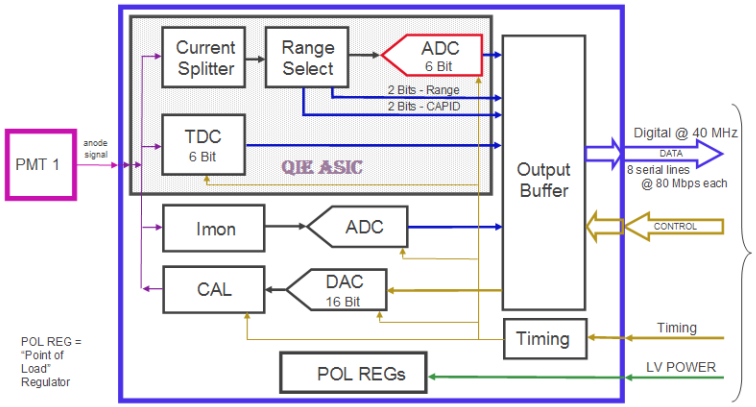




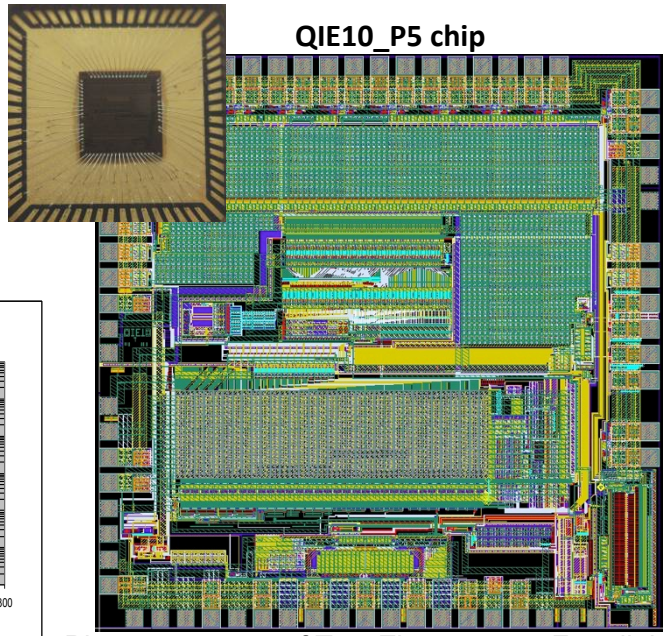


Front-end board option 3: QIE ASIC

- Third option for the front-end board is a charge integrator (different concept)
  - Performs a on-chip digitization with radiation tolerant design
  - Needs 4 clock cycles to acquire the data
  - Outputs a 17-bit dynamic range in 10 bits: 6-bit ADC value, 2 bits range (4 ranges), 2 bits CAPID
  - Clean measurement every 25 ns: No pulse shaping
  - Can be very useful against pile-up but requires technology change decision
  - Collaboration between ANL and FNAL
- Status with QIE10 design
  - 20 chips in hand, another 40 delivered soon
  - Passed noise, dynamic response and TDC tests
  - OK for TID test up to 50 kRad
  - No SEUs in Shadow Register up to 6E12 p/cm2
- Next steps:
  - Front-end board for this option soon
  - Full drawer tests in summer 2014 and Test beam in 2015

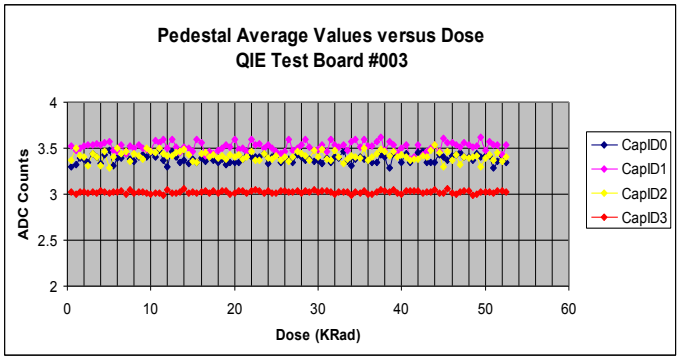


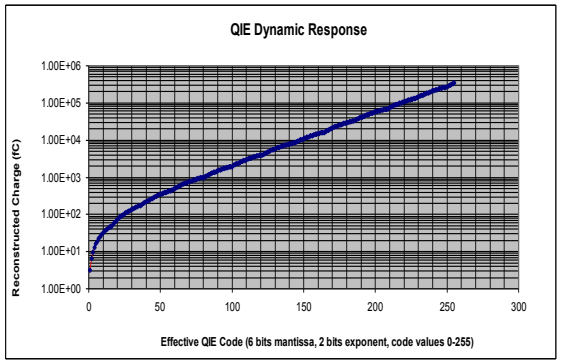
Conceptual Design of QIE Front-End Board



QIE10_P5 chip

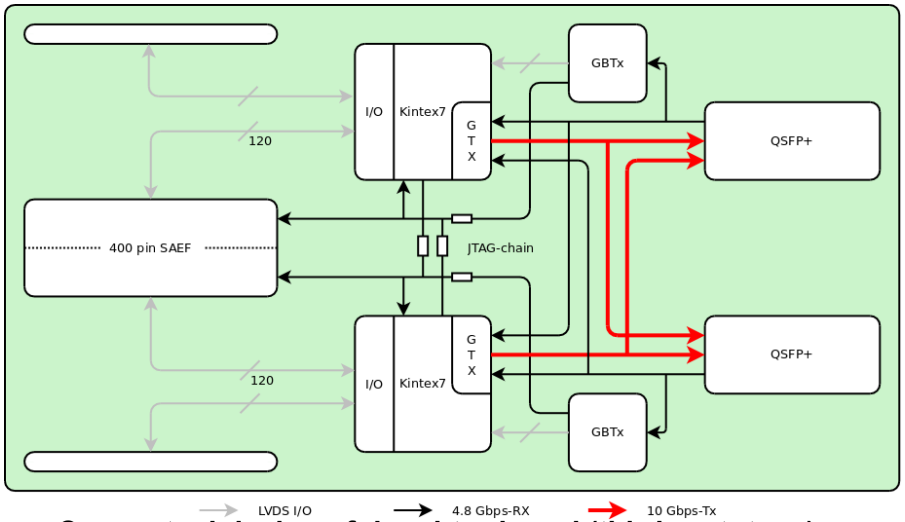
Picture courtesy of Tom Zimmerman, Fermilab



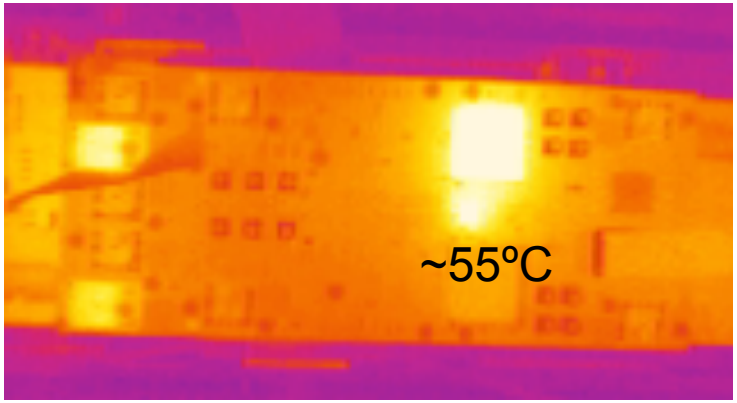


Daughter-board

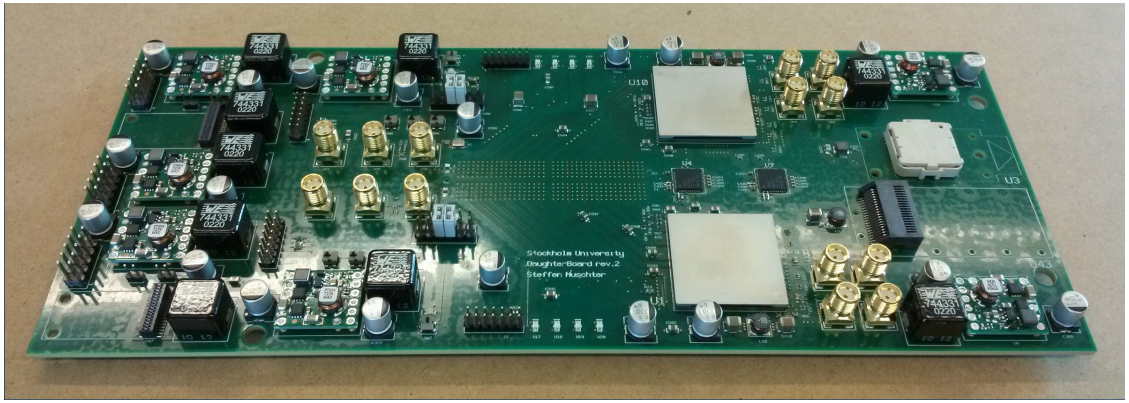
- Daughter-board provides GBT communication with back-end electronics
  - **Redundant** system on a single PCB + triple redundant FPGA programming
  - Two Kintex 7 FPGAs
  - Two QSFP modulators at 40 Gb/s
  - Two GBTx chips so firmware can be uploaded
  - Implementing GBT-FPGA protocol
- Status
  - First prototype tested in 2011
  - Second prototype manufactured in 2012
  - Third prototype delivered in few weeks
  - Radiation testing this week
  - Required heat dissipation for FPGAs as expected



Conceptual design of daughter-board (third prototype)

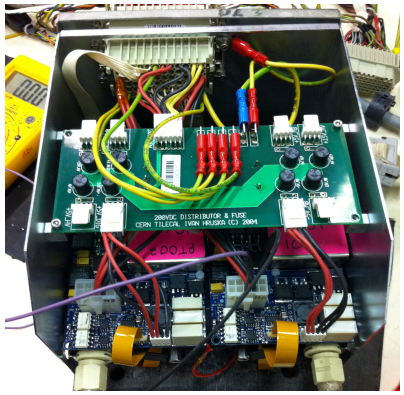


Infra-red image showing one programmed PFGA

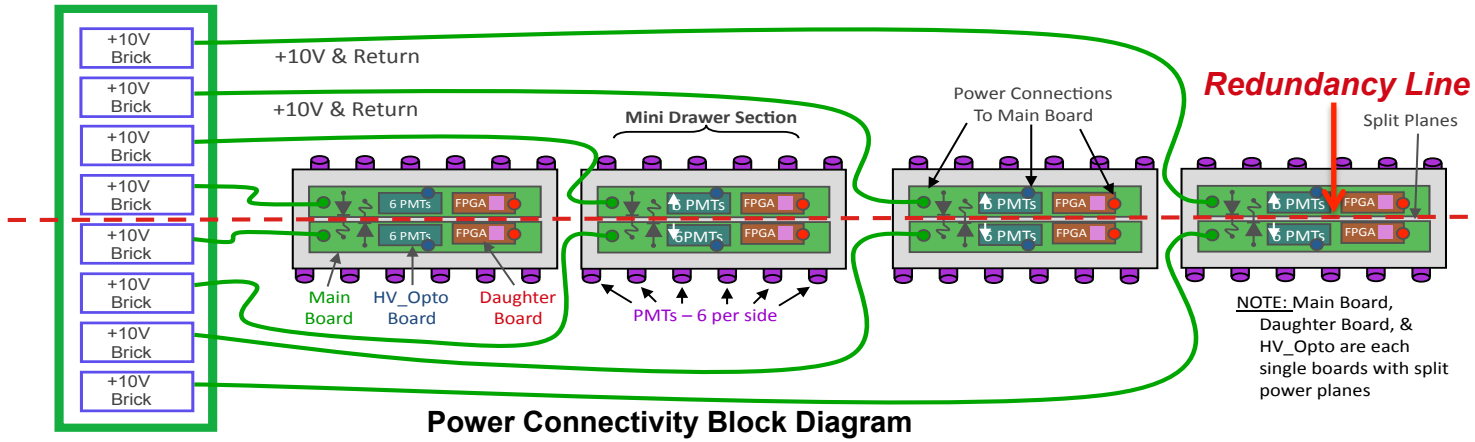


Second prototype of daughter-board (still with one modulator and one PPOD)

Low Voltage power distribution

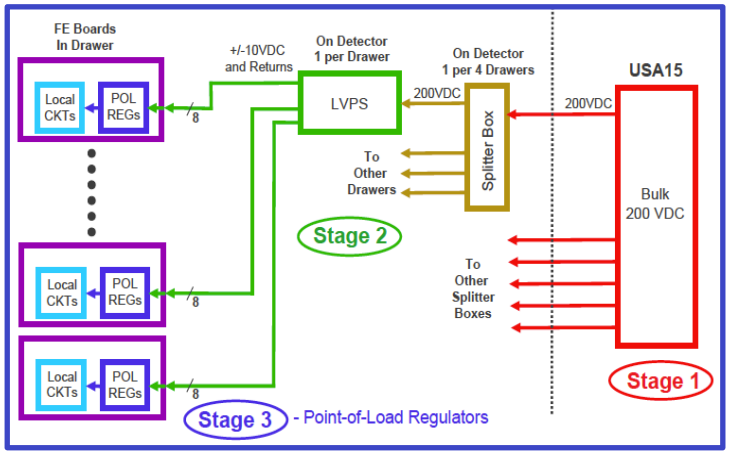


LVPS with two V8.0.1 bricks



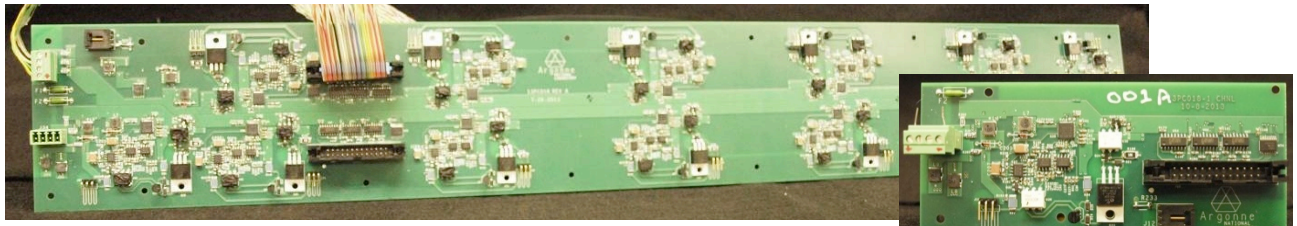
Power Connectivity Block Diagram

- Based on a three stage power distribution system
- Stage 1: bulk 200VDC PS in USA15
  - Provide power to four super-drawers
- Stage 2: LVPS boxes in front of super-drawers
  - New design providing only +10V in 8 separate bricks
  - Each brick serving half a mini-drawer
  - Require a factor 2 in the current output for redundancy
  - Produced and tested 3 units, 6 more ready for April 2014
- Stage 3: Point-of-Load regulators
  - Point to point connection from brick to mainboards
  - If one brick stops working, redundancy supply provides power through diode on the mainboard
  - Completed TID tests on 5 commercial off-the-shelf regulators
  - NIEL and SEE tests to be done in March 2014



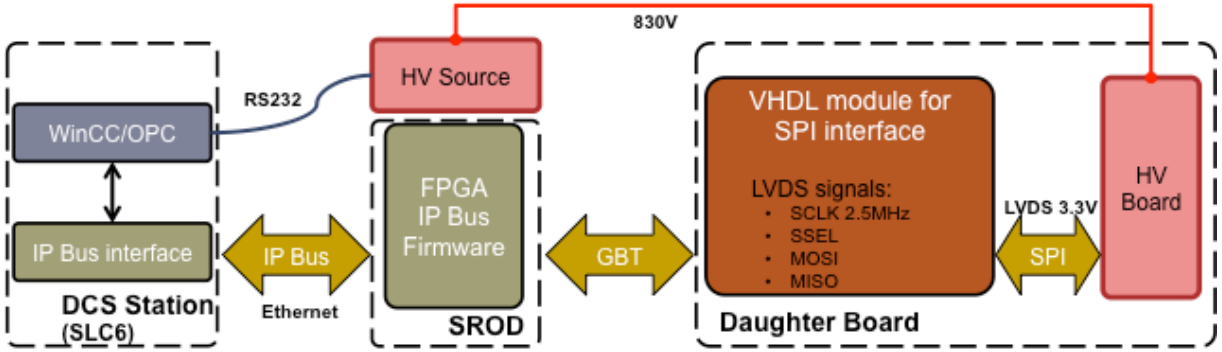
High Voltage power distribution

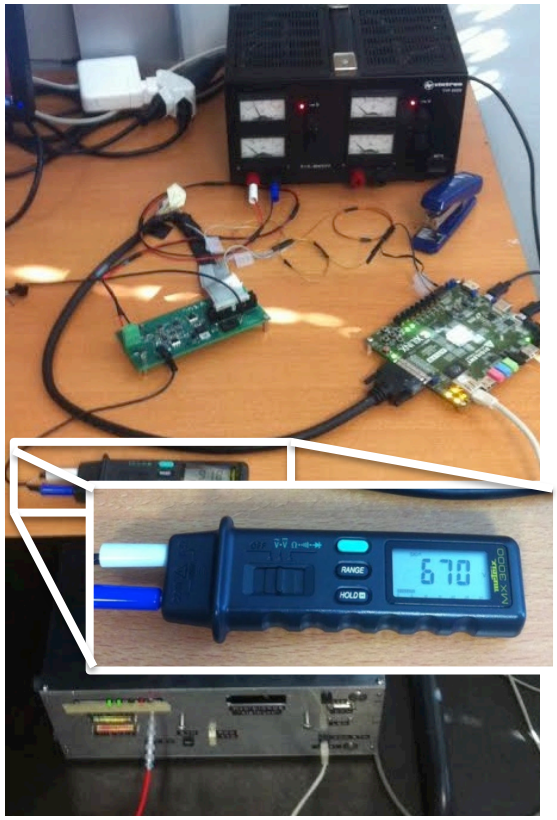
- Two options to provide HV to the PMTs based on commercial off-the-shelf components
- Front-end regulation (HV_Opto) largely based on existing design
  - Local HV_micro replaced by Kintex-7 FPGA on the daughter-board
  - Introducing possibility of switching on/off individual PMTs
  - Control of HV settings via VHDL module: Done
  - Interface to DCS through super-ROD via OPC server: Implementation in progress
  - First board tested: Radiation testing in March 2014
- Remote regulation from USA15 for individual PMTs
  - Regulated HV distributed via 100 m long multi-conductor cables
  - Measured small noise and small voltage drop (~10 mV in 800V)



First prototype of HV_Opto board ready

Single Channel Board for tests





Front-end links

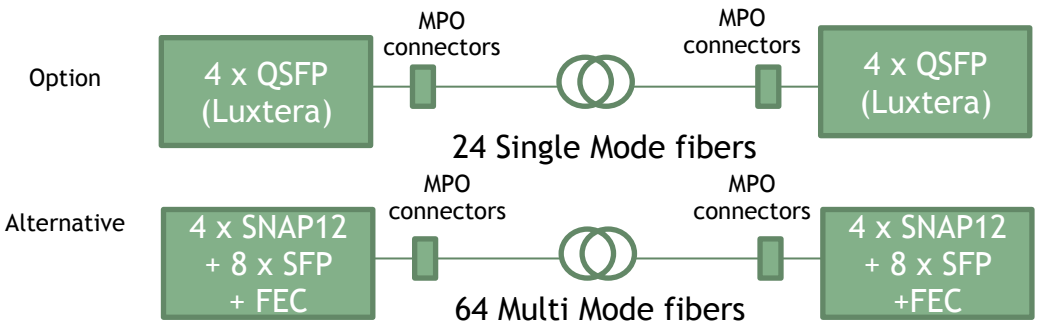
See poster by Alexander Paramonov

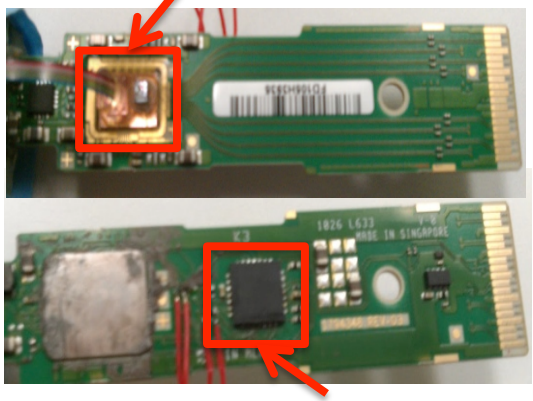
- Directly modulated lasers (including VCSELs)
  - Have been qualified at ~10 Gb/s per link with a Bit Error Rate (BER) ~10^{-12}
  - Increasing bandwidth increases problems
  - Commercial VCSEL arrays (SNAP12) have shown Single Event Upset (SEU) at ~10^{10} p/cm^2
  - Also these use Multi Mode fibers which are more expensive

10^{-12} BER = ~900 errors per day

10^{-18} BER = 1 error in ~1000 days

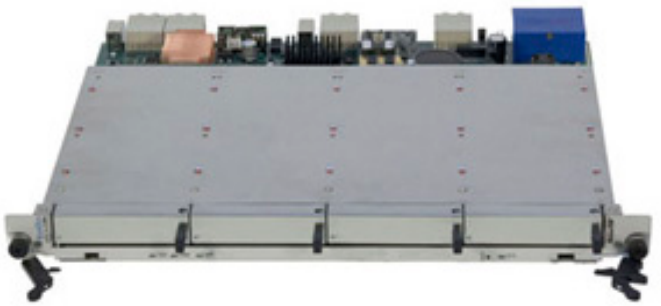
- A commercial off-the-shelf solution exists that uses single mode fibers at high transfer rates from Molex using Silicon Photonics technology developed by Luxtera (QSFP Active Optical Cable)
  - Can operate above 40 Gb/s (4x10) with BER < 10^{-18}
  - Made out of 130 nm Silicon On Insulator CMOS which should be very radiation hard
  - Radiation tests showed no SEU at TID of 165 kRad and fluence of 8x10^{11} p/cm^2
  - Problem is the PIC microcontroller used for configuration and monitoring survives ~20 kRad
  - Replacement is being developed
- QSFPs are the preferred option for the demonstrator
  - Less fibers vs lower clock frequency



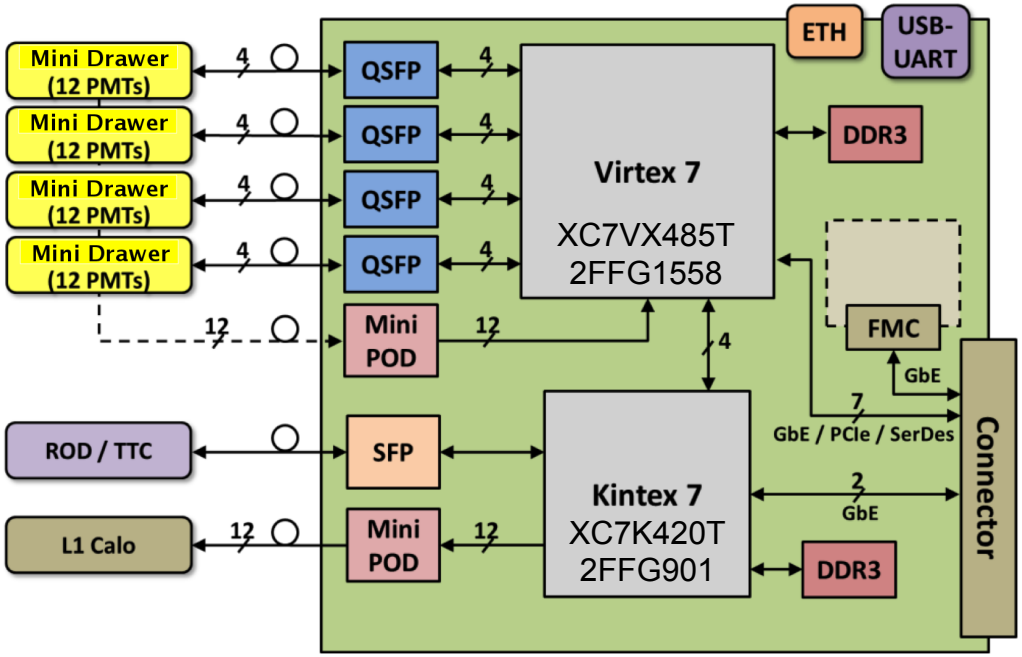


Trigger pre-processor (Super-ROD)

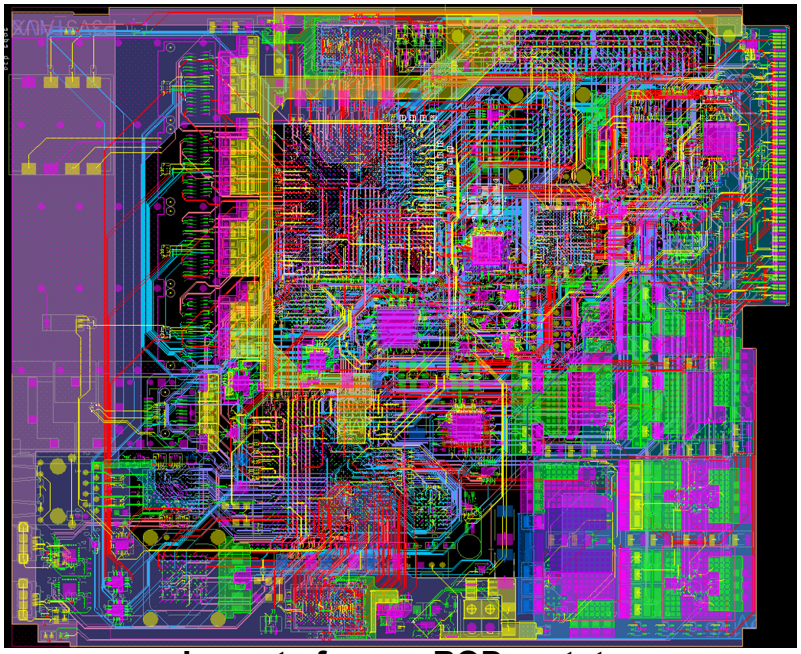
- Super-ROD is the interface with the on-detector electronics
  - Prototype compliant with double size AMC (180.6 mm x 148.5 mm)
  - Read-out of a complete super-drawer (4 mini-drawers)
  - Corresponding to ¼ of input links of the design for phase-II
  - Equipped with 4 QSFPs, 1 MiniPOD TX, 1 MiniPOD RX, 1 SFP
  - One Virtex 7 with 48 GTX@10Gb/s for front-end communication
  - One Kintex 7 with 28 GTX@10Gb/s for back-end communication
  - 512 MB DDR3 SDRAM and 1 Gb flash per FPGA
- First prototype ready for manufacturing
  - Stack-up 16 layers in ~1.7 mm with NELCO N4000 13 SI dielectric



ATCA carrier blade for super-ROD prototype

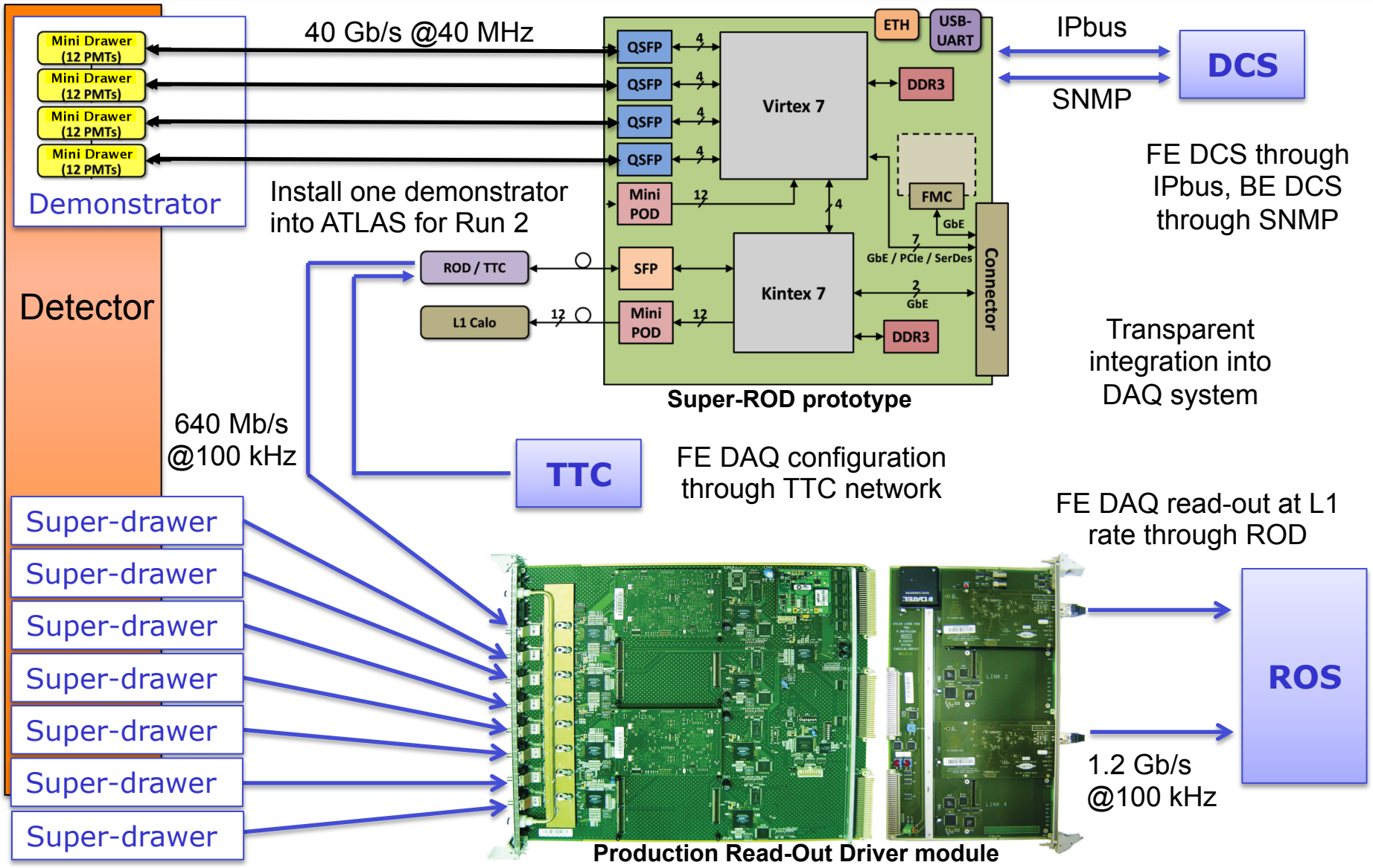


Conceptual design of super-ROD prototype



Layout of super-ROD prototype

Integration of the demonstrator



A portable test-bench for upgraded electronics

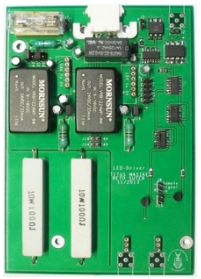
- Complete stand-alone and portable test-bench for upgraded Tile electronics (Prometeo) is under design
  - Stand-alone test-bench to assess the QA of the electronics
- Hardware
  - Based on a Virtex 7 evaluation board
  - QSFP module provides optical connection
  - HV and LED driver boards test response of PMTs
  - 16 channel ADC mezzanine to digitize the output of trigger cables
- Software
  - Based on IPbus, QT framework
  - Modular implementation to allow particular test implementation
- Status
  - All hardware components in hand, casing and cabling in progress
  - Firmware under design
  - Tests being finalised

A Portable ReadOut ModulE for Tilecal ElectrOnics
PROMETEO

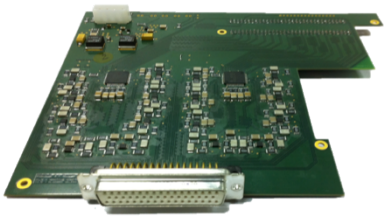
Virtex7 evaluation board

QSFP FMC module

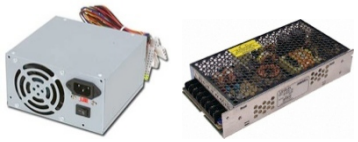
HV PS



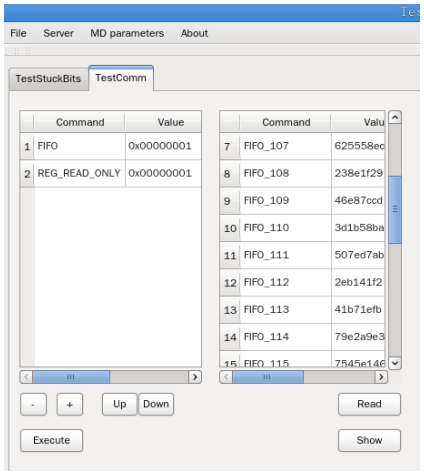
LED driver



16 channel ADC (hybrid demonstrator only)



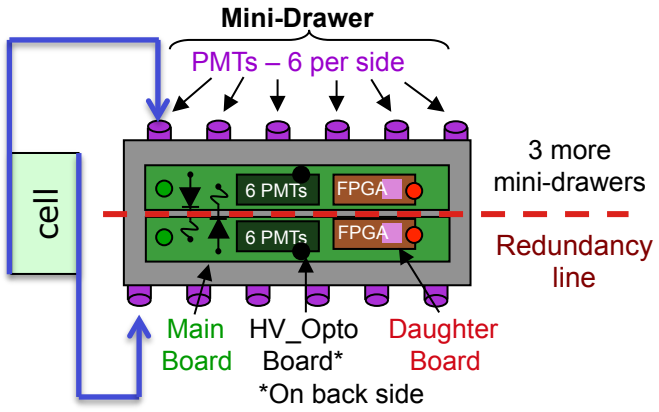
System power supply (commercial ATX + 24V)



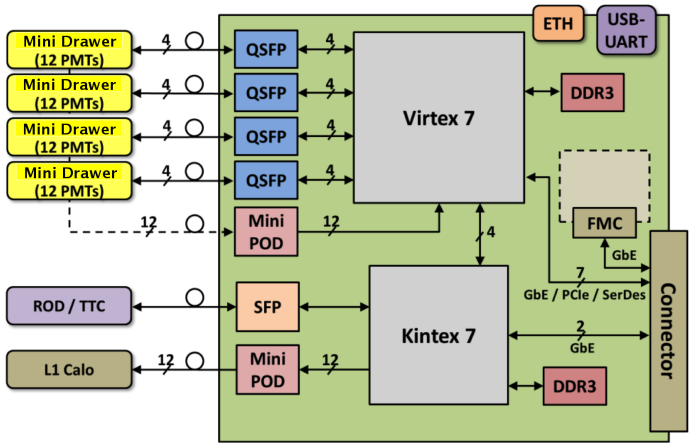
Test communication software panel

Conclusions

- Tile R&D for HL-LHC is well established
- Challenge to read-out per module as much data as we read-out today for the entire detector
- Developing different front-end board and HV distribution options
- Adopted GBT and QSFP AOC modulators a baseline
- Implemented redundancy in all front-end elements
- Developing an early prototype of the electronics for Run 2
- Further choices pending test beam performance in 2015



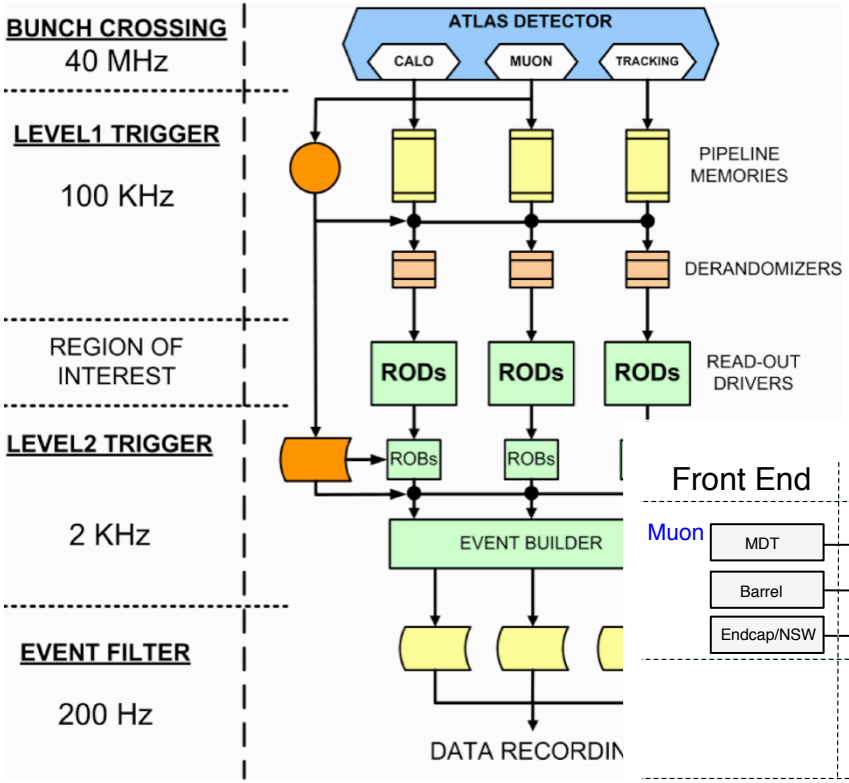
Cartoon of a mini-drawer for phase-II upgrade



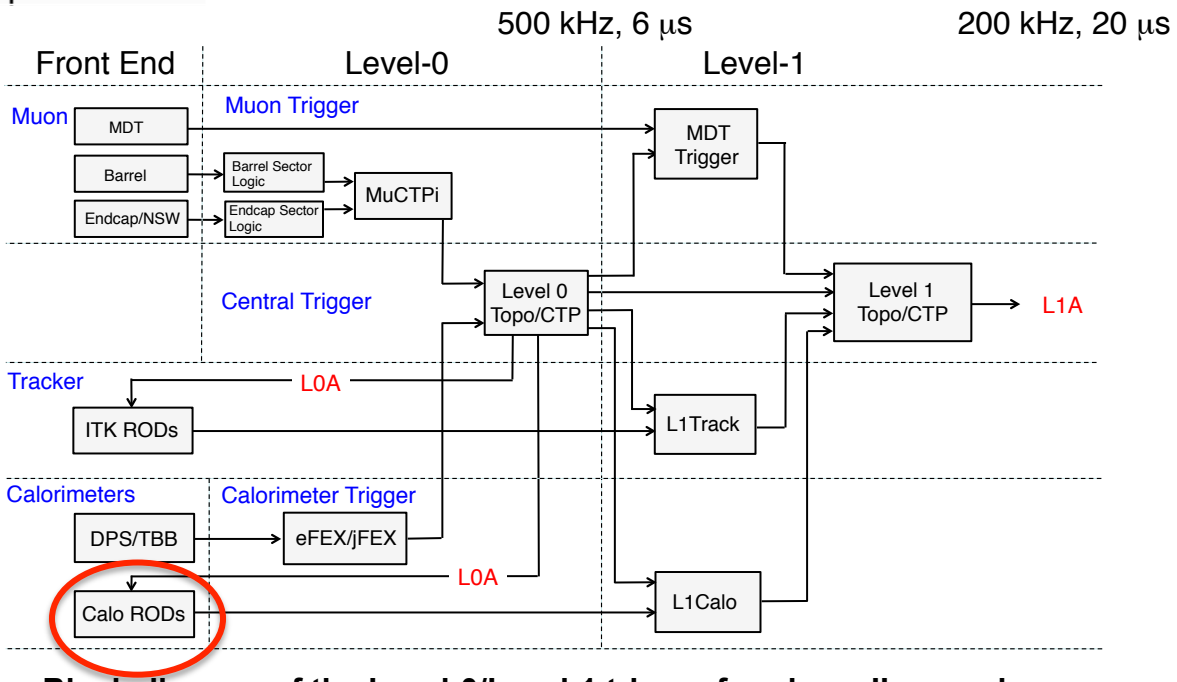
Cartoon of a trigger pre-processor for phase-II upgrade

Backup

ATLAS T/DAQ changes

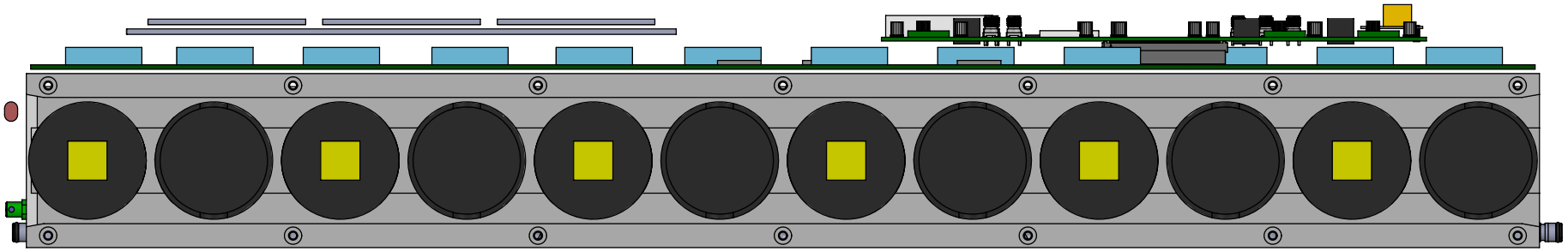


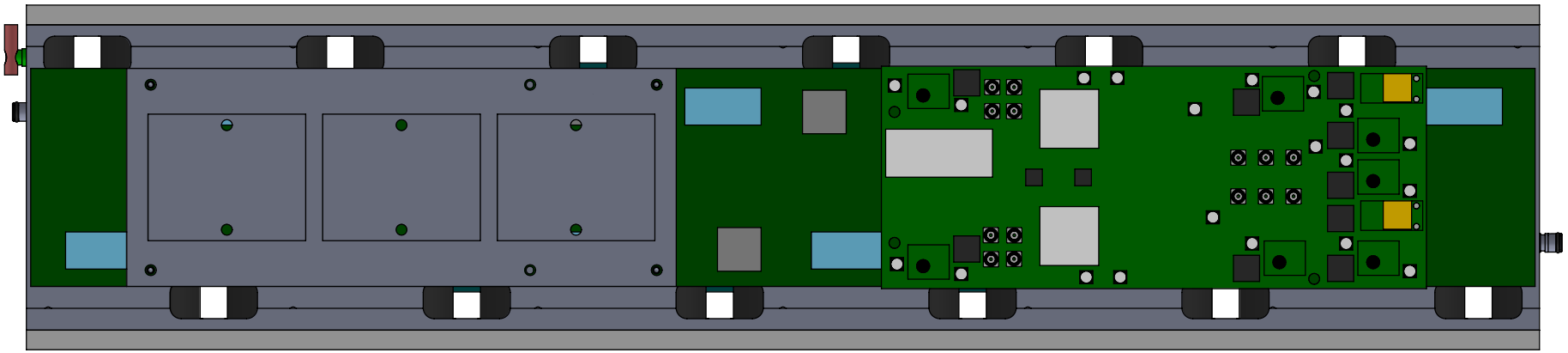
Current Trigger and DAQ architecture



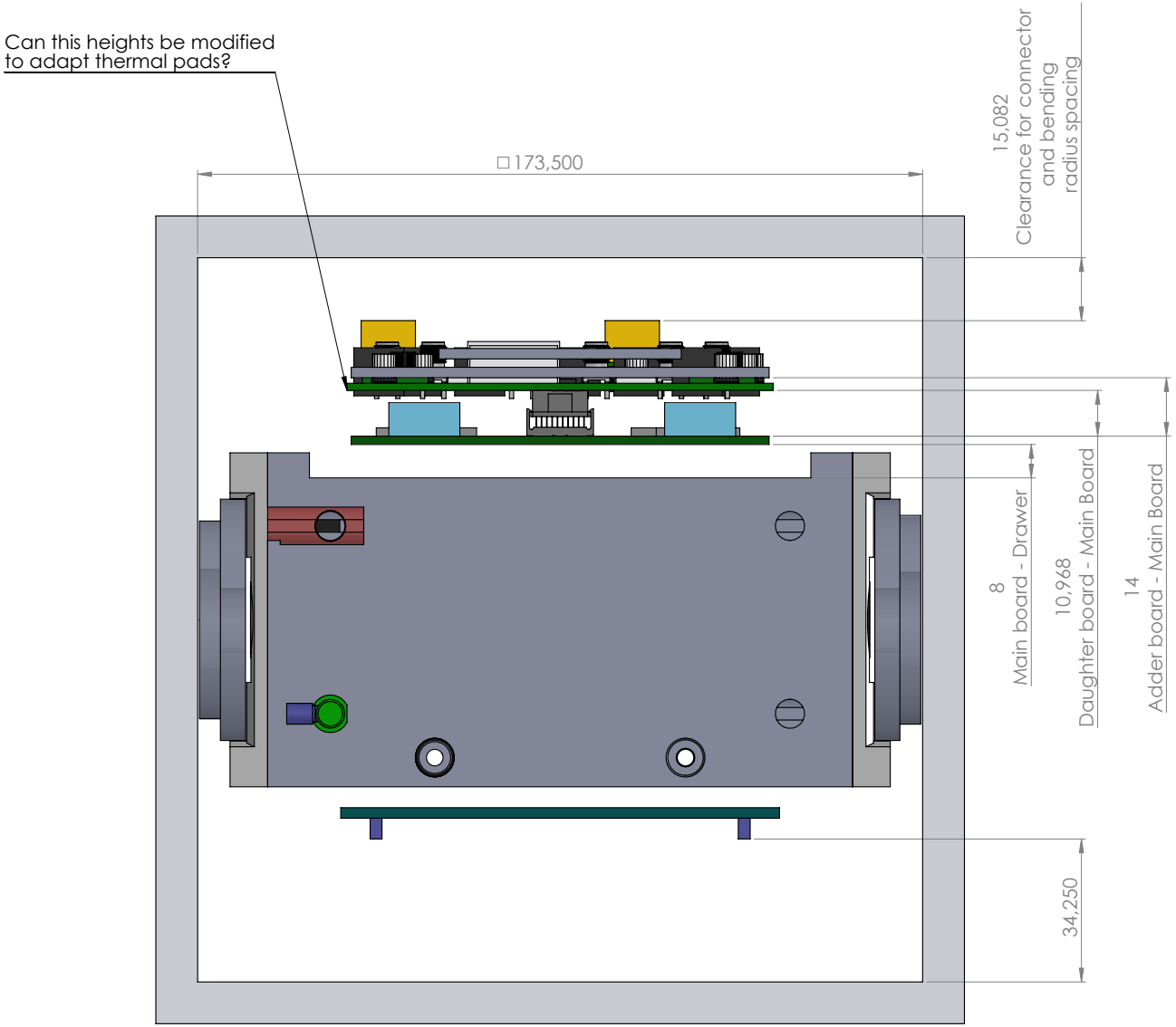
Block diagram of the Level-0/Level-1 trigger for phase-II upgrade

Mini-drawer CAD view





Mini-drawer cross section view



Front-end data format

Option 1: Full FEC

Word	95 82	81	80	79 68	67 56	55 44	43 32	31 0
n	Integ	0	Empty - misalignment word					FEC
n+1	Integ	1	G(0)	BCID	LG-Ch3	LG-Ch2	LG-Ch1	FEC
n+2	Integ	1	G(1)	BCID	HG-Ch3	HG-Ch2	HG-Ch1	FEC
n+3	Integ	1	G(0)	BCID	LG-Ch3	LG-Ch2	LG-Ch1	FEC
n+4	Integ	1	G(1)	BCID	HG-Ch3	HG-Ch2	HG-Ch1	FEC
n+5	Integ	1	G(0)	BCID	LG-Ch3	LG-Ch2	LG-Ch1	FEC
n+6	Integ	1	G(1)	BCID	HG-Ch3	HG-Ch2	HG-Ch1	FEC
..	..	..	..	.....	.....	.....	.....	.....
n+25	Integ	0	Empty - misalignment word					FEC
n+26	Integ	1	G(0)	BCID	LG-Ch3	LG-Ch2	LG-Ch1	FEC
n+27	Integ	1	G(1)	BCID	HG-Ch3	HG-Ch2	HG-Ch1	FEC

Word	95 82	81	80	79 68	67 56	55 44	43 32	31 0
n	Integ	0	Empty - misalignment word					FEC
n+1	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	FEC
n+2	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	FEC
n+3	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	FEC
n+4	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	FEC
n+5	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	FEC
n+6	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	FEC
..	..	..	..	.....	.....	.....	.....	.....
n+25	Integ	0	Empty - misalignment word					FEC
n+26	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	FEC
n+27	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	FEC

Two links are needed to read all the data

Option 2: CRC

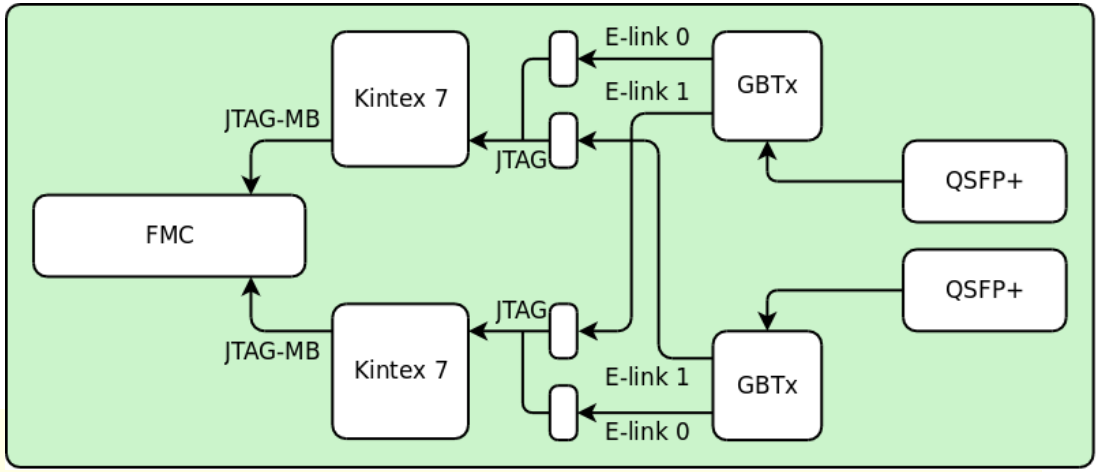
Word	95 91	90	89	88	87 76	75 64	63 52	51 40	39 28	27 16	15 0
n	Integ	1	Empty - misalignment word								CRC
n+1	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	LG-Ch3	LG-Ch2	LG-Ch1	CRC
n+2	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	HG-Ch3	HG-Ch2	HG-Ch1	CRC
n+3	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	LG-Ch3	LG-Ch2	LG-Ch1	CRC
n+4	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	HG-Ch3	HG-Ch2	HG-Ch1	CRC
n+5	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	LG-Ch3	LG-Ch2	LG-Ch1	CRC
n+6	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	HG-Ch3	HG-Ch2	HG-Ch1	CRC
....	....	....	...	.....	.....	.....	.....	.....	.....	.....	.....
n+25	Integ	1	Empty - misalignment word								CRC
n+26	Integ	1	G(0)	BCID	LG-Ch6	LG-Ch5	LG-Ch4	LG-Ch3	LG-Ch2	LG-Ch1	CRC
n+27	Integ	1	G(1)	BCID	HG-Ch6	HG-Ch5	HG-Ch4	HG-Ch3	HG-Ch2	HG-Ch1	CRC

Each link has a complete copy of the data

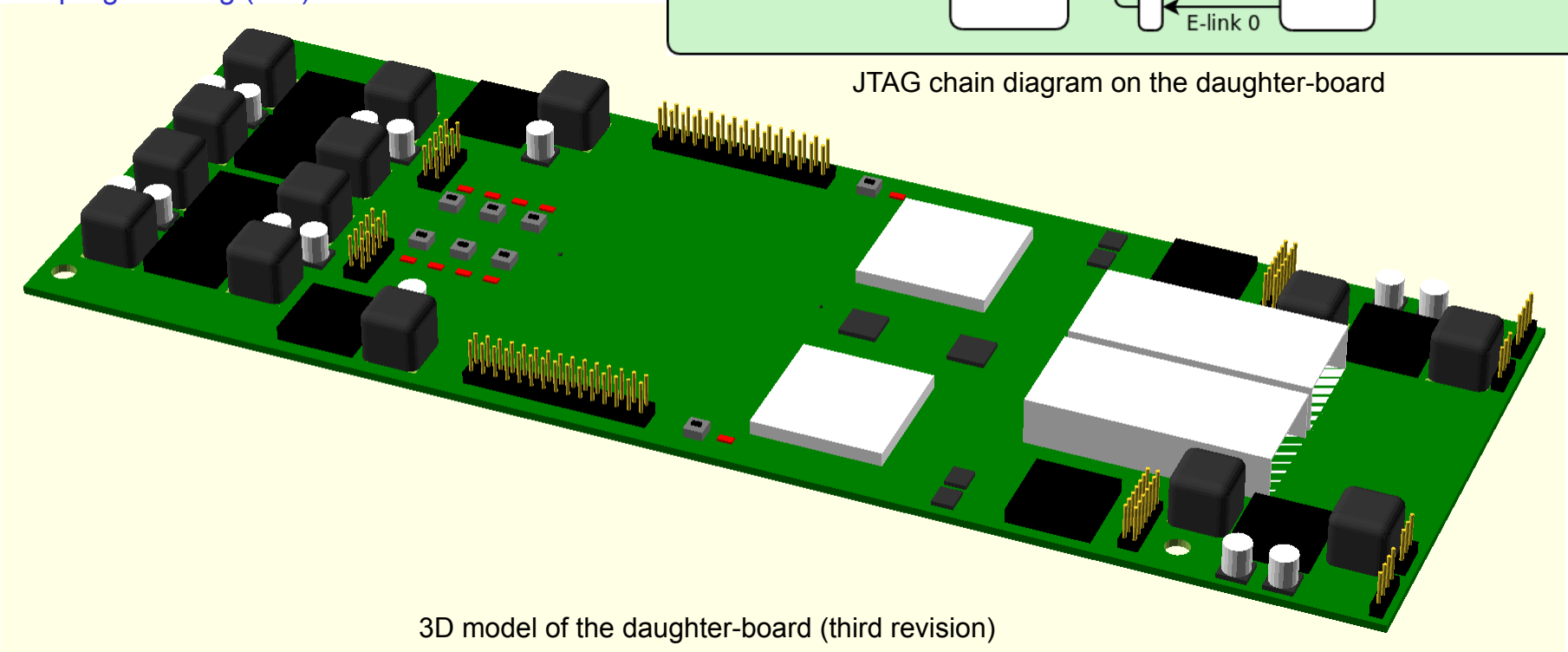
- Planning to use a 16-bit CRC error detection as opposed to a 32-bit forward error correction
- Back-end will have 2 copies of the same data and chose on the one without a CRC error on the fly

Third revision of the daughter-board

- Removed PPOD and add QSFP+
- Adapted to 10V supply
- Separated DB and MB JTAG chains
- Two GBTx chips allow remote FPGA programming from one QSFP+ module at a time
- Headers for HV_opto control (2x15 pins), single ended or differential communication (2x5), and GBTx programming (I2C)

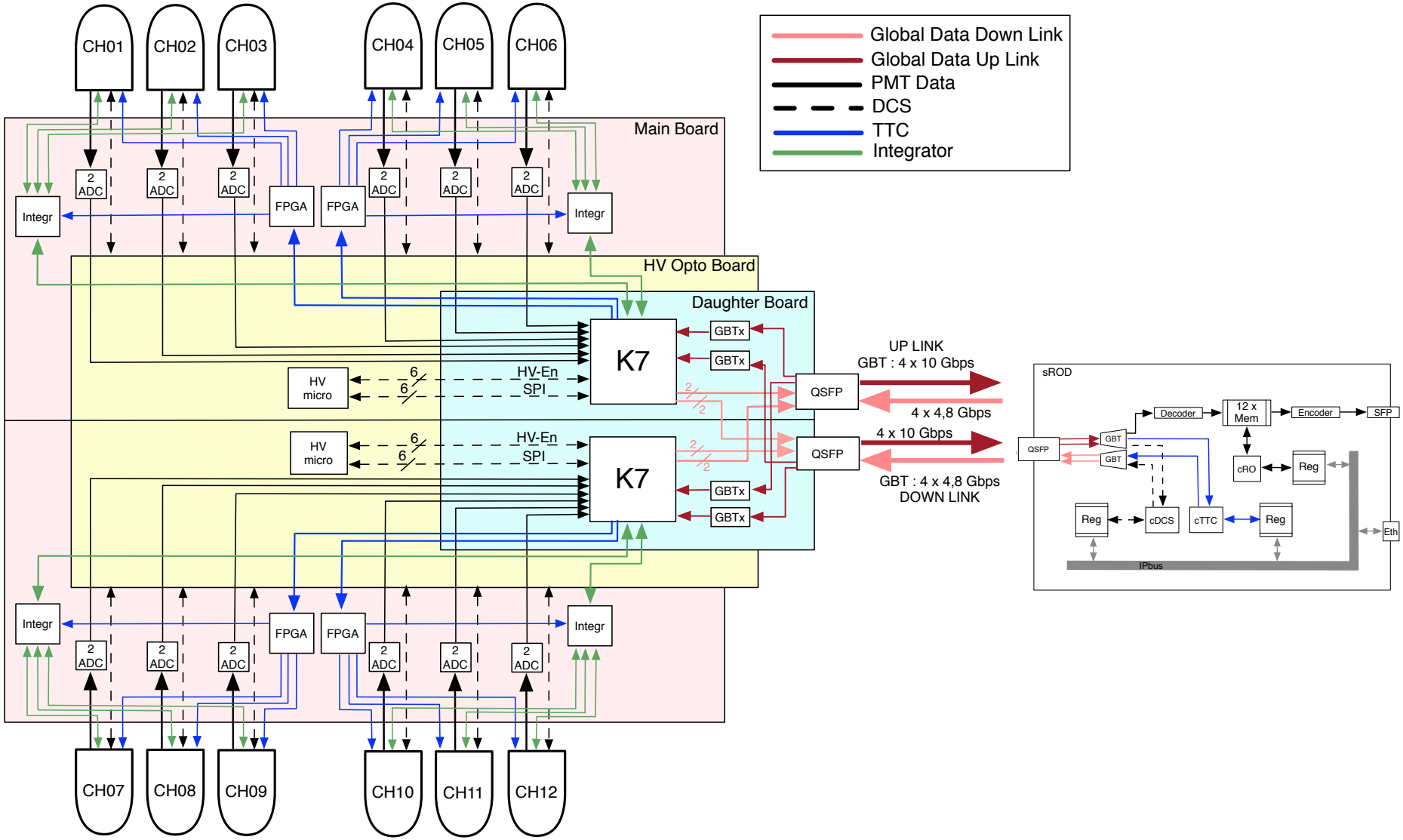


JTAG chain diagram on the daughter-board

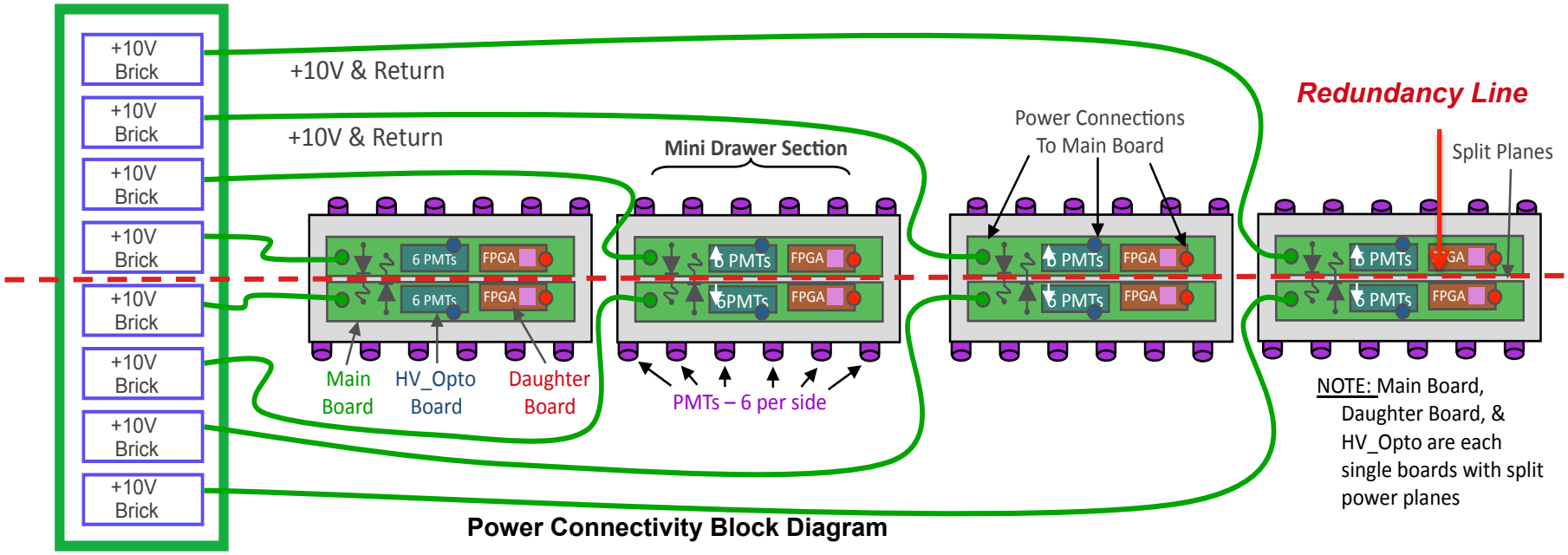


3D model of the daughter-board (third revision)

Data links


Global Data Down Link
Global Data Up Link
PMT Data
DCS
TTC
Integrator
CH01
CH02
CH03
CH04
CH05
CH06
CH07
CH08
CH09
CH10
CH11
CH12
Main Board
HV Opto Board
Daughter Board
2 ADC
FPGA
Integr
K7
GBTx
HV micro
HV-En
SPI
QSFP
UP LINK
GBT : 4 x 10 Gbps
4 x 4,8 Gbps
4 x 10 Gbps
GBT : 4 x 4,8 Gbps
DOWN LINK
sROD
GBT
Decoder
12 x Mem
Encoder
SFP
cRO
Reg
cDCS
cTTC
Eth
IPbus

Redundancy in the electronics



- One of the lessons we have learnt from the electronics consolidation process in ATLAS during the LS1 is that we need to think the electronics to maximize the redundancy in case of failure, minimize the coverage damage in case of failure
- A double read-out for the cell should be accompanied by a redundant data path from the PMT up to the back-end electronics
  - Split the super-drawers into four independent mini-drawers
  - Split each mini-drawer into two independent halves (one cell read-out by one side)
  - Use redundant powering scheme

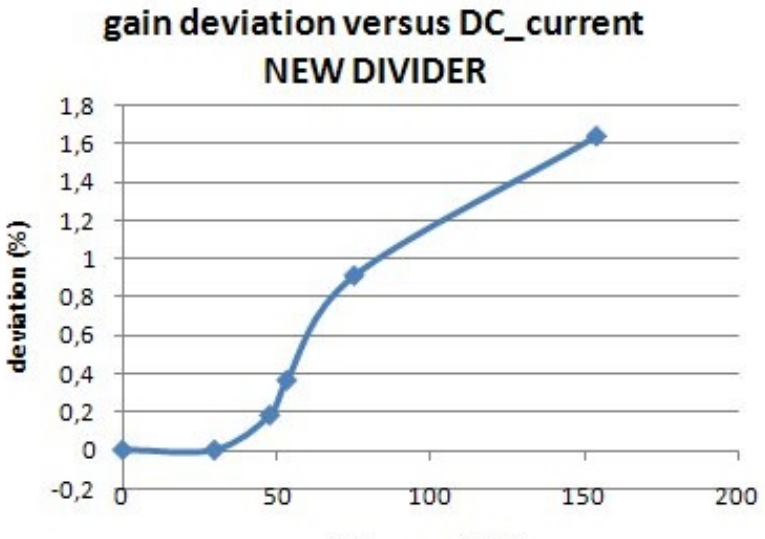
Active dividers

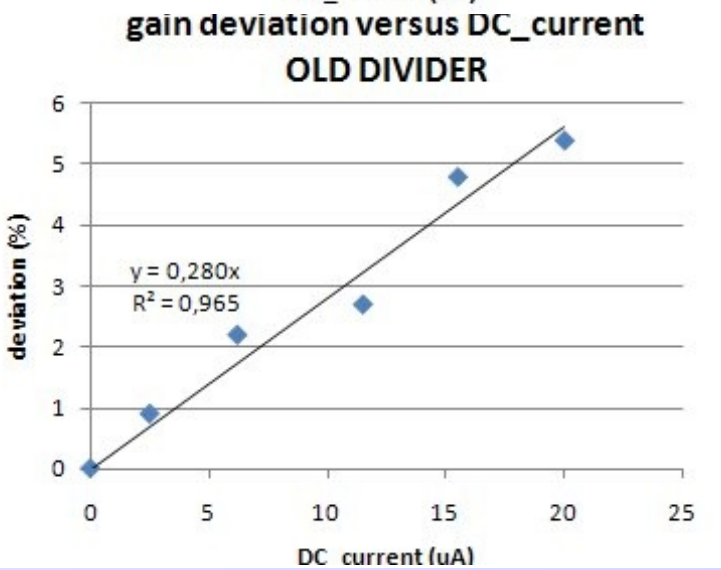
- Passive HV dividers of PMTs will be replaced by active ones
  - Offer better linearity and sustain higher current

  New Divider: ~1% non linearity at ~75 μA
  Old Dividers: ~2% non linearity at ~7.5 μA

- First version already produced
  - Tested for NEIL up to 1.5×10^{13} 1 MeV n/cm^2 in September 2013
  - Rejected huge number of first batch due to bad HV cable welding
  - Gamma irradiation in the next few weeks

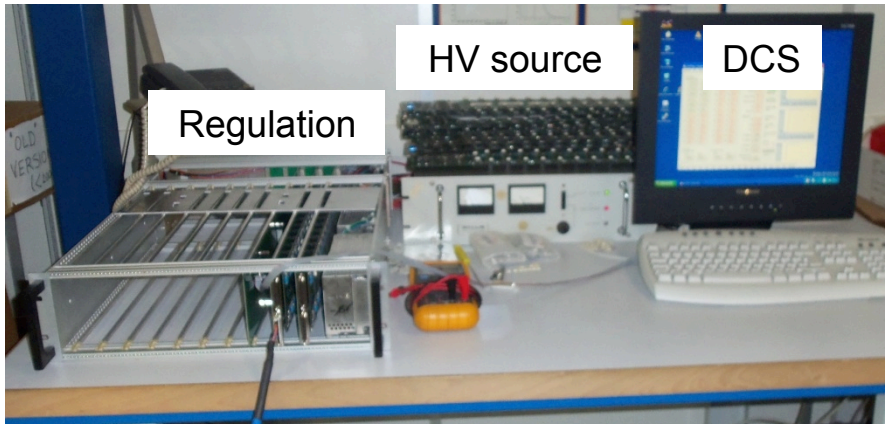
- Massive test of active dividers in Run 2
  - Replaced dividers in all MBTS and Gap/ Crack PMTs

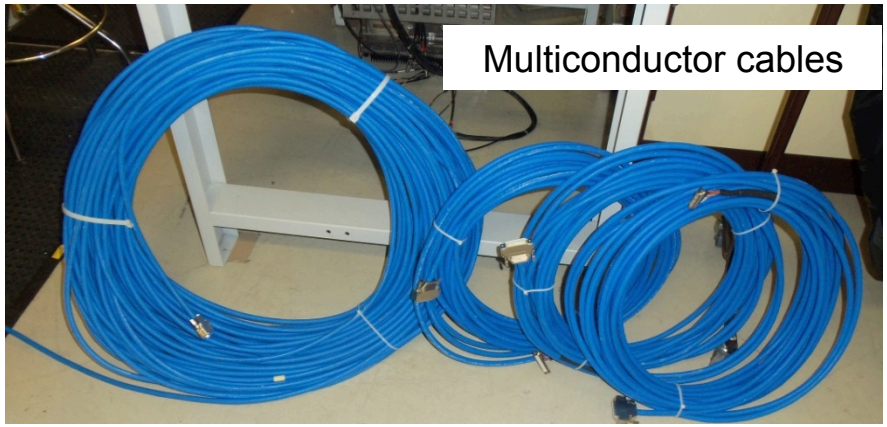


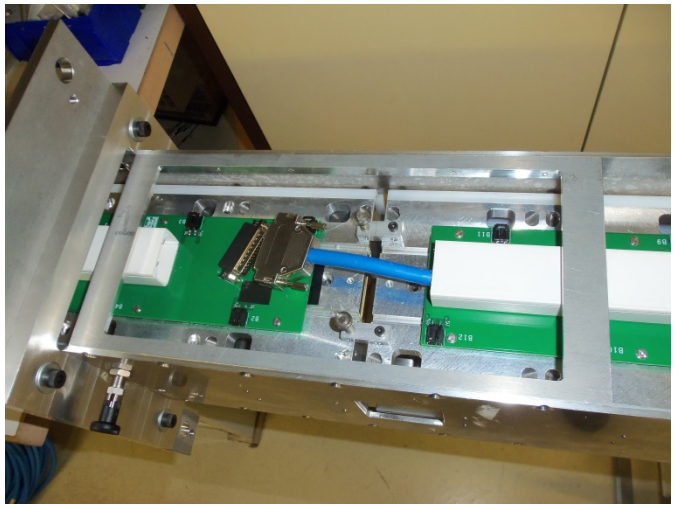


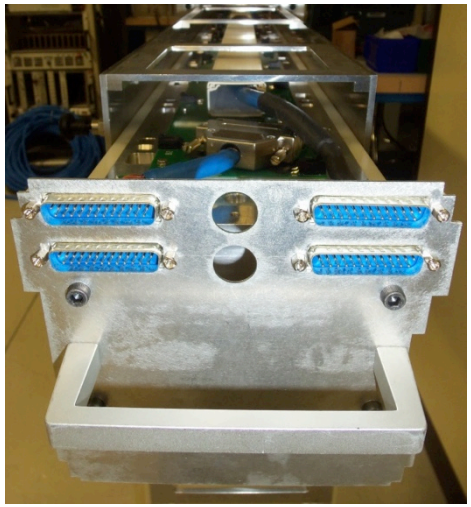
Second HV option

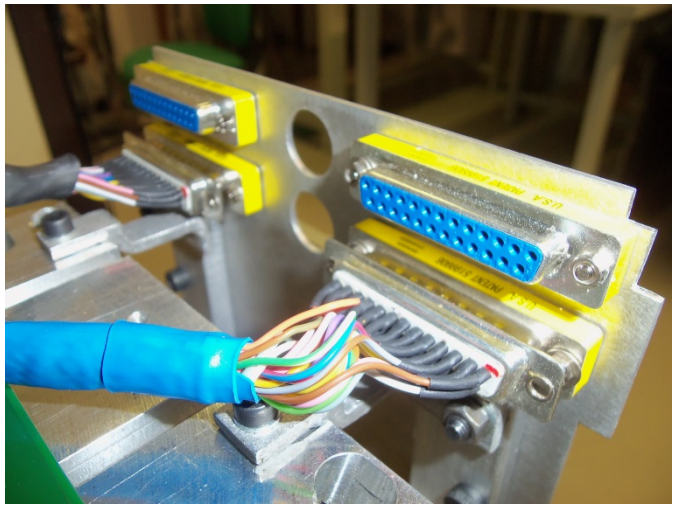
- External HV regulated from USA15 based on commercial off-the-shelf components
  - Regulated HV for each PMT distributed via multiconductor cables 100 m long
- Good progress: measured small noise and small voltage drop (~10 mV in 800V)



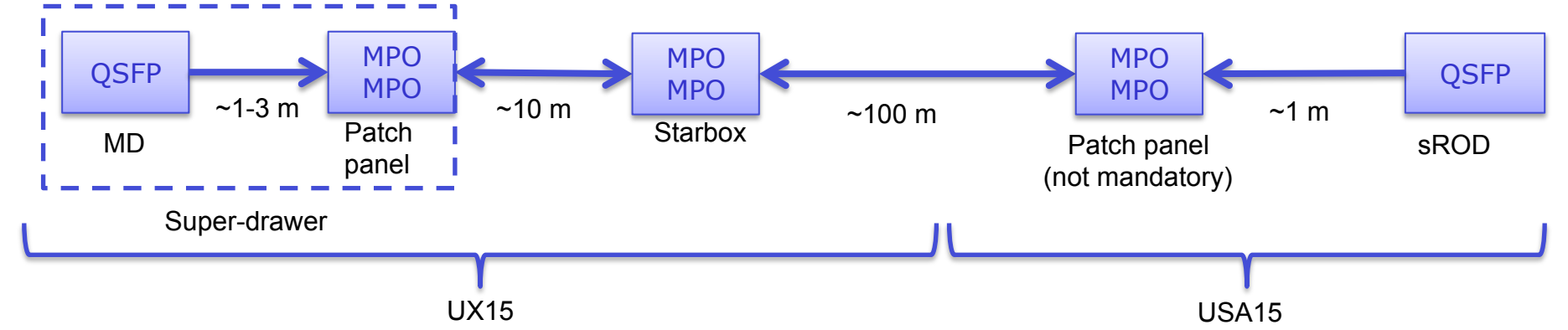








Services



- We need 8 QSFP front-end links per super-drawer
  - Using single mode 8F bundles with direct MPO-MPO connectors
  - Specifications allow 2.0 dB loss with expected attenuation of 0.7 dB per connection
- Distribution
  - 2 pigtails from each mini-drawer to a patch-panel on the finger of the module
  - 8 short fibers to a starbox on the face of the detector to facilitate replacement of faulty fibers
  - 1 long trunk cable from UX15 to Tile racks in USA15
  - 8 short connectors are being considered from a patch panel in USA15 to sROD inputs

MPO MPO ribbon fiber cable

ATCA shelf to be installed in USA15