Helen Hayward
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ATLAS ITK Requirements and Layout
The Future Phase II ATLAS Tracker Requirements

Guided by the physics requirements
Maintain and improve performance of existing ATLAS - ID to 3,000 fb$^{-1}$
- Tracking to $<\mu> \sim 160$–200, expect 1000 tracks per unit of rapidity
- Measure $P_T$ and direction of isolated particles (e and $\mu$),
- reconstruct vertices of pile-up events
- identify vertex of hard scatter
- Identify secondary vertices in b-jets with high efficiency and purity
- Measure tracks in the core of dense jets with good resolution
- Identify the decays of $\tau$ leptons, including impact parameter resolution
- Reconstruct tracks associated with converted photons
- The tracking must be robust against minor losses of acceptance

General ITk Requirements

Pixel

ITk Pixels.
- Fluences up to $2 \times 10^{16}$ 1MeV neq/cm$^2$
- Low mass to reduce multiple scattering ($<1.5\%X_0$ Inner, $<2.0\%X_0$ Outer)
- Inner layers removable/replaceable in a short LHC stop (clam shell)
- Approximately 10m$^2$ of pixels

Strip Detector

ITk Strips.
- Fluences up to $2 \times 10^{16}$ 1MeV neq/cm$^2$
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- Approximately 200m$^2$ of strips
# The Future Phase II ATLAS Tracker Requirements

## General ITk Requirements

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- Maintain and improve performance of existing ATLAS - ID to 3,000 fb⁻¹
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## Pixel

**ITk Pixels.**
- Fluences up to $2 \times 10^{16}$ 1MeV neq/cm²
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- Approximately $10m^2$ of pixels

## Strip Detector

**ITk Strips.**
- Fluences up to $2 \times 10^{16}$ 1MeV neq/cm²
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- ITk Strips.
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  - Approximately 200m² of strips
Baseline Layout

http://cds.cern.ch/record/1502664?ln=en
Baseline (LoI) Layout

http://cds.cern.ch/record/1502664?ln=en

Pixel Barrel x 4

Pixel Discs x 6

Beam Pipe 33mm

Polythene Moderator

eta = 0.0
eta = 1.0
eta = 2.0
eta = 3.0

r (m)

z (m)
Baseline (LoI) Layout

http://cds.cern.ch/record/1502664?ln=en

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ITk - Radiation Fluences: 1 MeV n_{eq}.cm^{-2}

Simulations with FLUKA

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ITk - Radiation Fluences : 1 MeV $n_{eq} \cdot cm^{-2}$

Simulations with FLUKA to 3,000 fb$^{-1}$
Performance of the ATLAS Phase II Tracker

Number of hits on Track

Sample of \( \bar{t}t \) events
Number of hits on muon tracks with $P_T > 5\text{GeV}$ as a function of pseudo-rapidity ($Z=0,150\text{mm}$)
Performance of the ATLAS Phase II Tracker
Number of hits on Track

$P_T$ resolution as a function of $\eta$
Comparison of current ID with & without the IBL

$P_T$ resolution as a function of $\eta$
For Upgrade tracker for different momenta
Construction of the ATLAS Phase II Tracker Detector Occupancies

Hit occupancies in different sub-detectors in the presence of 200 pile up events (peak around 0.9)

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Construction of the ATLAS Phase II Tracker Material

Particular attention put into reducing the material in the tracker volume
Note that everywhere less than 0.7Xo while in ID (+IBL) ~1.2%
Achieved through careful choice of materials, service routing etc
Performance of ATLAS Phase II Tracker Efficiencies

![Graph 1: ATLAS Simulation Efficiency vs. Brem Recovery](image1)

- **ATLAS Simulation**
  - 5GeV Muons, $<\mu>=140$
  - 5GeV Pions, $<\mu>=140$
  - 5GeV Electrons, $<\mu>=140$

![Graph 2: ATLAS Simulation Efficiency vs. Brem Recovery](image2)

- **ATLAS Simulation**
  - 100GeV Muons, $<\mu>=140$
  - 100GeV Pions, $<\mu>=140$
  - 100GeV Electrons, $<\mu>=140$

![Graph 3: ATLAS Simulation Light Jet Rejection vs. b-Jet Efficiency](image3)

- **ATLAS Simulation**
  - # $t\bar{t}$, IP3D+SV1
  - pileup=0, ITk
  - pileup=50, ITk
  - pileup=140, ITk
  - pileup=0, IBL
  - pileup=50, IBL

![Graph 4: ATLAS Simulation Primary Vertex Candidates vs. Number of Pileup Interactions](image4)

- **ATLAS Simulation**
  - Number of Pileup Interactions vs. Primary Vertex Candidates

NB Brem recovery used

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Alternate Layouts of Phase II Pixels

Conical (Barrel area 5.1 → 4.6 m²)

Fifth Pixel (optimized pattern rec)

Alpine (reduced area L modules)

Work also ongoing with coverage out to a pseudorapidity of 4
Alternate Layouts of Phase II Pixels

Conical (Barrel area 5.1 → 4.6 m$^2$)

Fifth Pixel (optimized pattern rec)

Conical A

Work also ongoing with coverage out to a pseudorapidity of 4

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Alternate Layouts of Phase II Pixels

Conical (Barrel area 5.1 → 4.6 m²)

Fifth Pixel (optimized pattern rec)

Alpine (reduced area modules)

Work also ongoing with coverage out to a pseudorapidity of 4
ATLAS Phase II Pixels

• **Candidate Sensor Technologies**
  – Choices largely driven by radiation tolerance requirements.
    • *Standard Planar Sensors*
      – Thin (150µm) High Resistivity Silicon [n-in-n *(inner layers)* or n-in-p (outer)]
      – Demonstrated to HL-LHC fluxes, Lots of experience and known vendors, mass production understood.
    • *3D sensors*
      – *Used in the IBL, Low depletion voltage after irradiation, radiation tolerant*
    • *Diamond Sensors*
      – *Good radiation tolerance, Low capacitance (noise), no cooling, BUT expensive*
      – *Used in ATLAS beam monitoring, current and replacement in 2014*
    • *CMOS*
      – *Emergent technology (used on STAR and baseline for ALICE ITS), low power, varying degrees of sensor-hybrid integration (move away from standard implementation) to a more MAPS like approach, Cheap, Need to demonstrate radiation tolerance and readout speed.*
  – Choices
    • *Extensive R&D in progress, wait for appropriate time to make decisions*
ATLAS Phase II Strips

- Sensors
  - Need to withstand $8.1 \times 10^{14}$ neq cm$^{-2}$ (no safety factor) and operate up to 500V. Including a safety factor takes us to $2 \times 10^{15}$ neq cm$^{-2}$
  - Current baseline is n-in-p FZ, 320 μm thick, 97.54 x 97.54mm$^2$
  - 1280 strips, AC coupled to FE chip, pitch 74.5μm
  - On stave/petal, sensors axial on one side, small angle stereo on the other
  - 2 lengths of strips: short = 23.82mm, long=47.75 (match track density)
  - The petal sensors use pointing strips (to beam-line) and so sensors are wedge shaped. Ideally sizes would minimize number of wafers (currently assuming 6”)

Fully populated DC-DC powered 250nm stave in December 2013
Collected signal charge at 500Vbias voltage for minimum ionising particles as a function of 1MeV neq/cm² fluence for different particle species. S/N at end of life > 23 (17) for barrel (EndCap) Need S/N >10 for efficient tracking.
Collected signal charge at 500V bias voltage for minimum ionising particles as a function of 1 MeV neq/cm² fluence for different particle species.

S/N at end of life > 23 (17) for barrel (EndCap) and barrel (EndCap) need S/N > 10 for efficient tracking.

Taken from talk of P. Rieder in Aix Les Bain (Oct 2013)

<table>
<thead>
<tr>
<th>Upgrades</th>
<th>Area</th>
<th>Baseline sensor type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALICE ITS</td>
<td>10.3 m²</td>
<td>CMOS</td>
</tr>
<tr>
<td>ATLAS Pixel</td>
<td>8.2 m²</td>
<td>tbd</td>
</tr>
<tr>
<td>ATLAS Strips</td>
<td>193 m²</td>
<td>n-in-p</td>
</tr>
<tr>
<td>CMS Pixel</td>
<td>4.6 m²</td>
<td>tbd</td>
</tr>
<tr>
<td>CMS Strips</td>
<td>218 m²</td>
<td>n-in-p</td>
</tr>
<tr>
<td>LHCb VELO</td>
<td>0.15 m²</td>
<td>tbd</td>
</tr>
<tr>
<td>LHCb UT</td>
<td>5 m²</td>
<td>n-in-p</td>
</tr>
</tbody>
</table>
Collected signal charge at 500V bias voltage for minimum ionising particles as a function of 1MeV neq/cm² fluence for different particle species. S/N at end of life > 23 (17) for barrel (EndCap). Need S/N > 10 for efficient tracking.
Conclusions

• Designing a new Inner Tracker detector to maintain and improve on the existing ID performance

• The ITK will be a pixel plus strip based tracker which can perform
  – At higher pile up conditions
  – At higher radiation environment
The End
Bonus Material
The **Current ATLAS Inner Detector (ID)**  
**Initial Specifications & Limitations**

3 layers of Pixels (PIX), 4 layers of Si micro-strips (SCT), straw tracker (TRT)  
Additional PIX-layer (IBL) to be inserted in Long Shut-Down 1 (LS1 - 2014)  
ID designed for **10 years** of operation, peak luminosity of **$1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$**  
The assumed pile up ($\mu$) was **23**, bunch crossing frequency **25ns**  
and the L1 trigger rate of **100kHz. 2 Tesla Magnetic field**

- **Current Inner Detector**
- **Radiation Damage**
- **Bandwidth Limitation**
- **Occupancy limits**

PIX: designed to withstand **$1 \times 10^{15} \text{ 1MeV neq/cm}^2$** or about **$400 \text{F}^{-1}$**

IBL: designed to about **$850 \text{F}^{-1}$**

SCT: designed to withstand **$2 \times 10^{14} \text{ 1MeV neq/cm}^2$** or about **$700 \text{F}^{-1}$**

Both SCT and PIX apply zero suppression to accommodate < $\mu$ > up to 50  
This is being expanded in LS1 to get beyond 75 (3 x $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ @ 25ns)  
However, there are "hard wired" limitations which mean one cannot go beyond this.

PIX-Limits 0.2-0.4 pixels per 25ns.  
For SCT data rate between FE chip and ReadOut Driver (ROD) limit us to  
With the occupancy expected at the HL-LHC the SCT would not be able to resolve close-by tracks in the core of High P_T jets  
The TRT will approach 100% occupancy and tracking efficiency will suffer accordingly.
The Current ATLAS Inner Detector (ID)
Initial Specifications & Limitations

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**Radiation Damage**
- PIX: designed to withstand $10^{15} \text{ 1MeV neq/cm}^2$ or about 400fb$^{-1}$
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The **Current ATLAS Inner Detector (ID)**

**Initial Specifications & Limitations**

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- The assumed pile up (\(\mu\)) was 23, bunch crossing frequency 25ns and the L1 trigger rate of **100kHz**. **2 Tesla Magnetic field**

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The Current ATLAS Inner Detector (ID) Initial Specifications & Limitations

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With the occupancy expected at the HL-LHC the SCT would not be able to resolve close-by tracks in the core of High $P_T$ jets
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The LHC roadmap (updated December 2013)

- **2009**: LHC startup, $\sqrt{s} = 900$ GeV
- **2010**: $\sqrt{s} = 7+8$ TeV, $L \sim 6 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$, bunch spacing 50ns
- **2011**: Go to design energy, nominal luminosity - Phase 0
- **2012**: $\sqrt{s} = 13-14$ TeV, $L \sim 1 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, bunch spacing 25ns
- **2013**: LS1
- **2014**: Injector + LHC Phase I upgrade to ultimate design luminosity
- **2015**: $\sqrt{s} = 14$ TeV, $L \sim 2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, bunch spacing 25ns
- **2016**: LS2
- **2017**: HL-LHC Phase II upgrade: Interaction Region, crab cavities?
- **2018**: LS3
- **2019**: $\sqrt{s} = 14$ TeV, $L \sim 5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, luminosity levelling
- **2020**: Run 1
- **2021**: Run 2
- **2022**: Run 3
- **2023**: $\sim 25$ fb$^{-1}$
- **2024**: $\sim 75-100$ fb$^{-1}$
- **2025**: $\sim 350$ fb$^{-1}$
- **2035?**: $\sim 3000$ fb$^{-1}$
Performance of the ATLAS Phase II Tracker Compared with the existing ID + IBL

<table>
<thead>
<tr>
<th>Track parameter</th>
<th>Existing ID with IBL no pile-up</th>
<th>Phase-II tracker 200 events pile-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>\eta</td>
<td>&lt; 0.5$</td>
</tr>
<tr>
<td>Inverse transverse momentum ($q/p_T$) [TeV]</td>
<td>0.3</td>
<td>0.2</td>
</tr>
<tr>
<td>Transverse impact parameter ($d_0$) [\mu m]</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Longitudinal impact parameter ($z_0$) [\mu m]</td>
<td>65</td>
<td>50</td>
</tr>
</tbody>
</table>

The expected performance of the ATLAS Phase II tracker compared to the performance of the existing ID with the addition of the IBL. $\sigma_x(\infty)$ refers to $\sigma_x$ for $P_T \to \infty$ which allows one to remove the effect of material.

Performance parameters extracted from full ATLAS simulation including realistic service routing and appropriate engineering considerations.
Performance of the ATLAS Phase II Tracker
Number of hits on Track

Good particle separation
Inside jets achieved with
Small pixel size
2 innermost pixels: $25 \times 150 \mu m^2$
2 outer pixels: $50 \times 250 \mu m^2$

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## ATLAS Phase II : Strips Material

<table>
<thead>
<tr>
<th>Element</th>
<th>% Radiation Length</th>
<th>Element</th>
<th>% Radiation Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stave Core</td>
<td>0.55</td>
<td>Petal Core</td>
<td>0.47</td>
</tr>
<tr>
<td>Bus Cable</td>
<td>0.30</td>
<td>Bus cables</td>
<td>0.03</td>
</tr>
<tr>
<td>Short-Strip Modules</td>
<td>1.07</td>
<td>Modules</td>
<td>1.04</td>
</tr>
<tr>
<td>Module Adhesive</td>
<td>0.06</td>
<td>module adhesive</td>
<td>0.06</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>1.98</strong></td>
<td><strong>Total</strong></td>
<td><strong>1.60</strong></td>
</tr>
</tbody>
</table>
Petalet layout

Top Sensors

Upper Hybrid

Lower Hybrid

Big Sensor

~8cm

~7cm
Lamb&Flag upper hybrids

- 1 lower and 2 upper hybrids designed and produced
- Population with passive components
- ASIC assembly with flip-chip bonder
- Tested with low noise of ~380ENC
Bear modules for petalet in embedded (straight bonding due to double metal layer on sensor) configuration
lower modules have noise of ~660 ENC upper module to be tested, upper and lower hybrids have noise of ~380 ENC
Bear modules for petalet in embedded (straight bonding due to double metal layer on sensor) configuration
lower modules have noise of ~660 ENC upper module to be tested, upper and lower hybrids have noise of ~380ENC
Bear modules for petalet in standard (wire-bonds with different angles) configuration have lower noise of about 560ENC.
ATLAS Phase II Pixels : Planar sensors

Sensor Inefficiency vs. Fluence and Voltage

Hit inefficiency for n-in-n sensors (IBL) as a function of bias voltage for different fluences.
ATLAS Phase II Pixels

• **Electronics Technologies & Challenges**
  
  – **Specifications and Challenges.**
    
    • Radiation tolerance, Low power consumption per channel, Low noise
    
    • High density of channels -> interconnects (TSV, bump-bonding=cost)
    
    • Move towards deep(er) sub-micron technologies 65nm. CERN - RD53 now established and operational.
    
    • On detector power conversion (DC-DC (baseline) and Serial Power under consideration)
  
  – **FEI4**
    
    • *Currently being used for IBL, requirement well matched to outer layers of ITk pixel detector. To limit cooling requirements chip power should not exceed 450mW/cm².*
    
    • *RD65 to develop the next generation of chips*

  – **Choices**
    
    • *Extensive R&D in progress, wait for appropriate time to make decisions*
ATLAS Phase II Pixels: Modules and Structures

A prototype of a Quad Module
This has 4 FEI4 chips
Core and bus tape

- Core:
  - Designed and production ongoing
  - Results:
    - Planarity: still low (~250 um flatness).
    - Ti-pipes resistance: more than 200 bar.

- Bustape:
  - First designed and produced.

---

Core: Designed and production ongoing

Results:

- Planarity: still low (~250 um flatness).
- Ti-pipes resistance: more than 200 bar.

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ATLAS Phase II Strips
ATLAS Phase II Strips: Staves/Petals

Fig. 1. Sketch of a barrel short strip stave and its cross-section (top); sketch of an end-cap petal (bottom).
ATLAS Phase II Strips : End-Caps

Figure 6.37: Turbofan arrangement of petals.
ATLAS Phase II : Track Trigger

• L1 Track Trigger
  ✓ Aim to keep $p_T$ thresholds and trigger rates low at L1
  ✓ Part of High Level Trigger reconstruction moved to L1

• Triggering sequence
  • Based on Regions of Interest (RoI)
    ✓ L0 trigger (Calorimeter/Muons) reduces rate within 6 $\mu$s to $\geq$ 500 kHz and defines RoIs
    ✓ L1 track trigger extracts tracking info inside RoIs from detector FEs

Alternate self seeded (a la CMS) approach also being studied.
ATLAS Phase II: Changes to trigger architecture

- New design in time for Phase II
  - 2-level system at Phase II
  - Phase-I L1 becomes Phase-II L0, new L1 includes tracking
  - Make use of improvements made in Phase 1 (NSW, L1Calo) in L0
  - Introduce precision muon and inner tracking information in L1
- Better muon pT resolution
- Track matching for electrons...
  - Requires changes to detector FE electronics feeding trigger system

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Fully populated DC-DC powered 250nm stave in December 2013

FE electronics
ABCN is an evolution of the binary chip used for the SCT (binary readout)

Prototypes based on 250nm CMOS already in use
New 130nm currently under evaluation