ATLAS LAr Calorimeter Upgrade for HL-LHC

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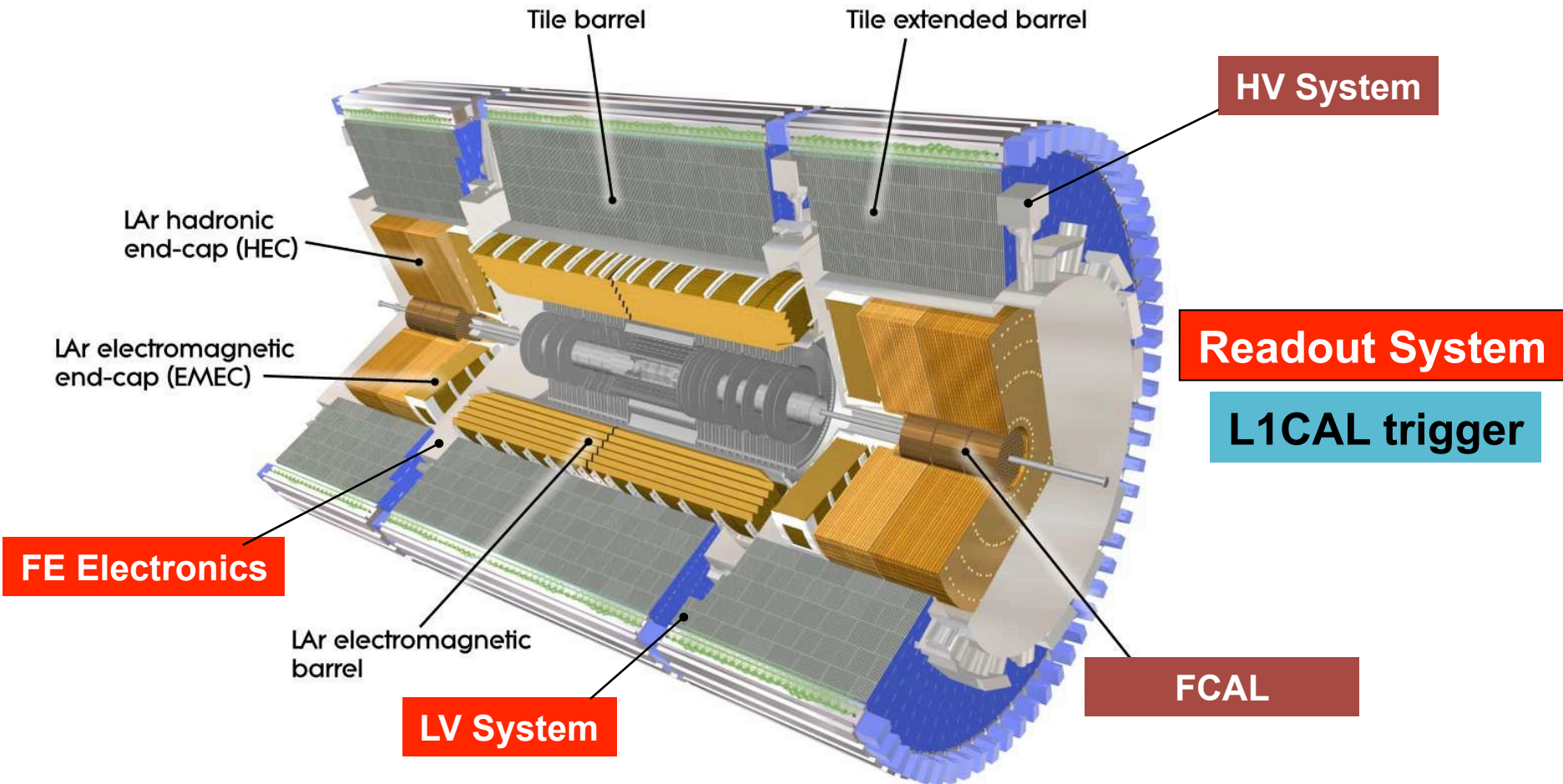
For ATLAS Liquid Argon Calorimeter Group

ATLAS LAr Upgrades for HL-LHC

Phase-I: Changes to L1 trigger

Phase-II: New readout and optionally a new forward calorimetry and the HEC cold electronics replacement

Contents of This Presentation

1. Concepts of LAr Readout Upgrade*
2. System Level Studies
3. Current R&Ds for the Front-end
    a. Preamplifier and Shaper ASICs
    b. ADC ASIC developments
    c. The Optical Link
4. Conclusions

* LAr upgrades consist of phase-I trigger upgrade and phase-II readout and detector upgrades. Reported here is only the phase-II readout upgrade.
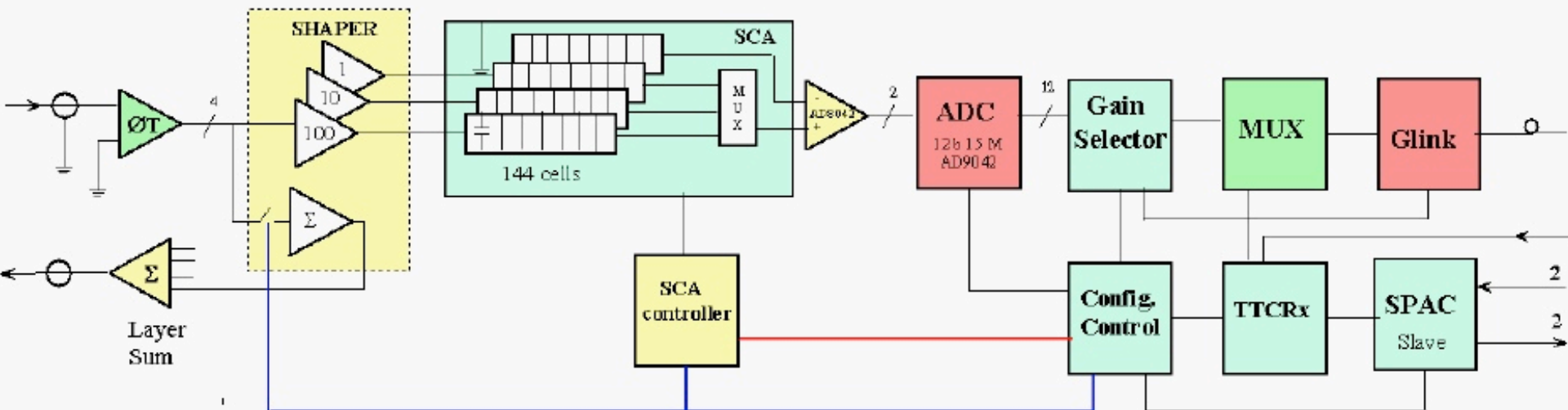
Concepts of LAr Readout Upgrade
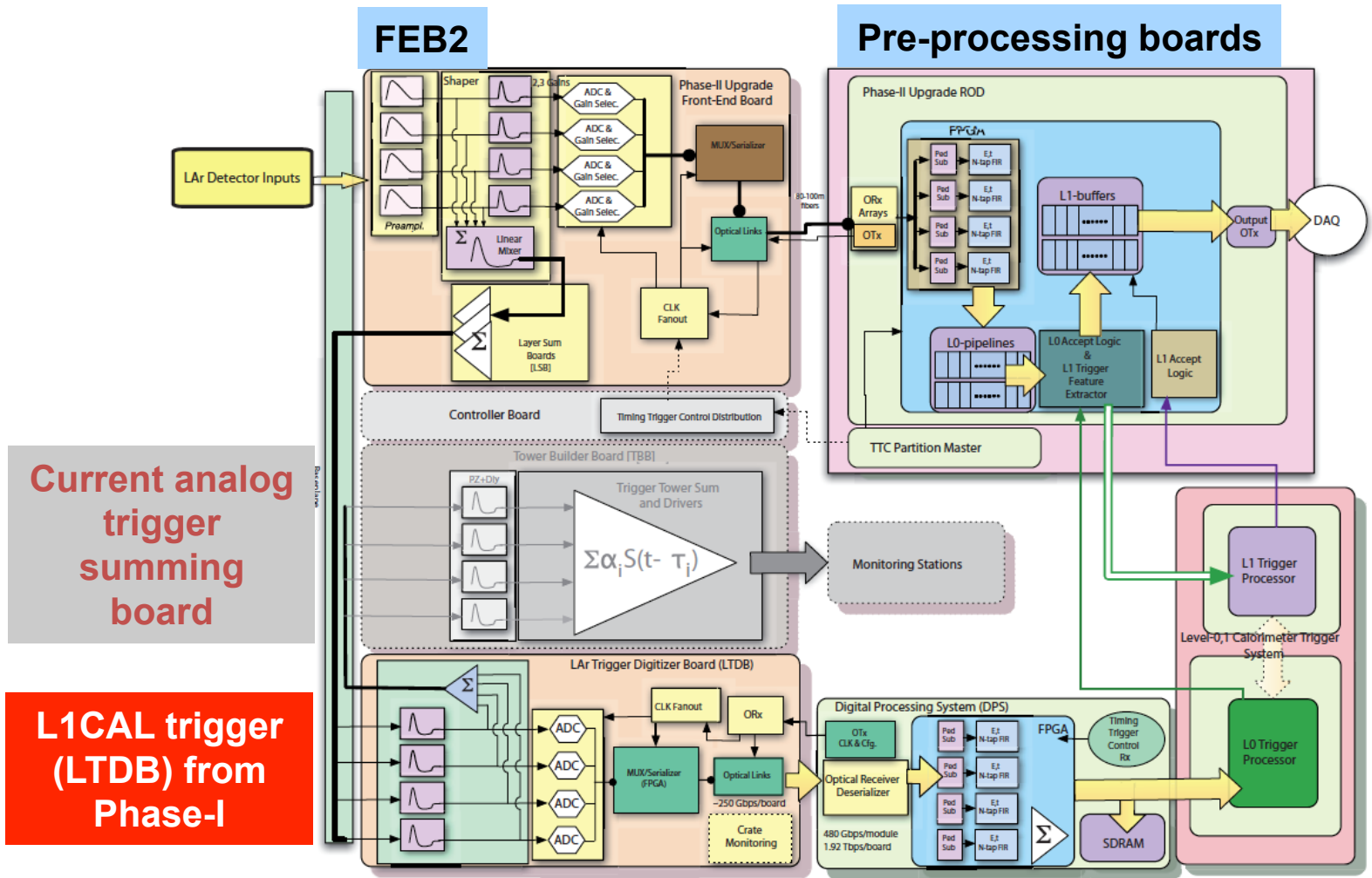
LAr readout upgrade to eliminate current limits on L1 rate and latency, to avoid operation of electronics beyond design lifetime and qualified radiation tolerance.
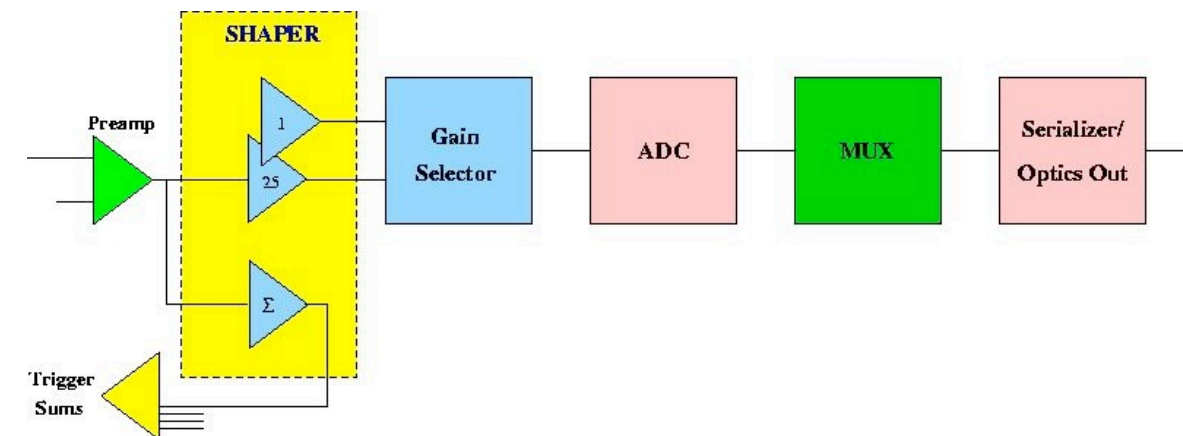
Concepts of LAr Readout Upgrade

Current detector readout scheme on the FEB

Proposed readout upgrade (FEB2)

Critical R&D:
1. **Pre-amp + Shaper**
2. **ADC (12 to 16 bit)**
3. **Optical Link (10 G)**

System Level Studies

Questions (for example):

○ Analog v.s. digital shaping?

Digital shaping adds the flexibility of adjusting shaping time according to operation conditions.
For the analog shaper, keep bipolar or can we move to unipolar?

○ Sampling rate and digital filtering algorithms for high pileup operation conditions

• What is the optimum waveform sampling rate to distinguish pileup events within the digitizing rate and data bandwidth achievable in ADC and the optical link?

• With data streamed to the back-end, should we still treat pileup as noise or we can find a better digital signal processing algorithm to separate piled-up events?
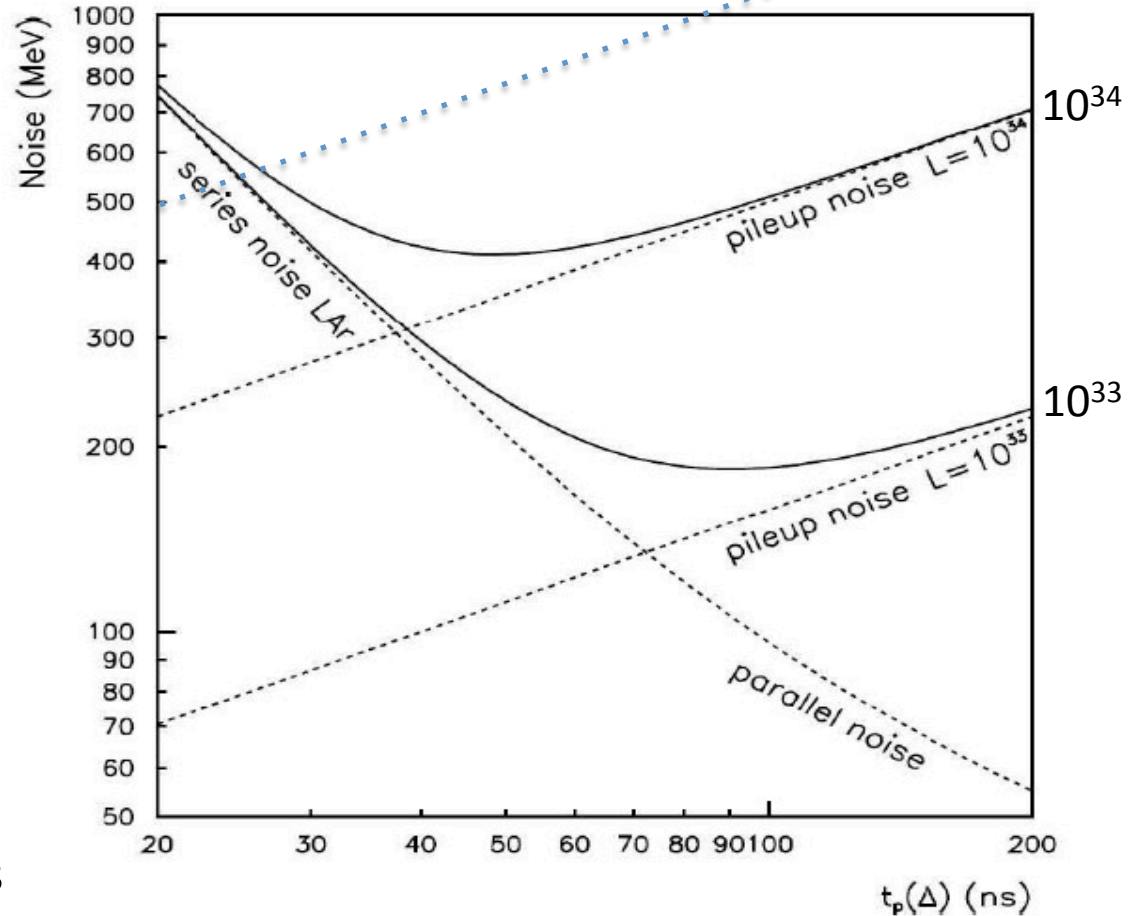
Current Component Level R&Ds

R&Ds are concentrated for the front-end:

(back-end can usually start later, and it will benefit greatly from developments for phase-I)

a. **Preamplifier and Shaper ASICs**

Two prototypes, one based on IBM 8WL, the other IHP, both are SiGe. Plan to investigate IBM 7WL as well.

b. **ADC ASIC developments**

Two architectures for phase-I: pipeline+SAR, a full SAR. R&D will be needed for phase-II, including technology and architecture changes.

c. **The Optical Link**

Currently based on Silicon-on-Sapphire 0.25 µm CMOS and reached 8 Gbps. Plan to migrate to 65 nm CMOS for phase-II.

d. **Studies on GaAs preamplifiers in cold (LAr) under irradiation (not covered in this talk)**
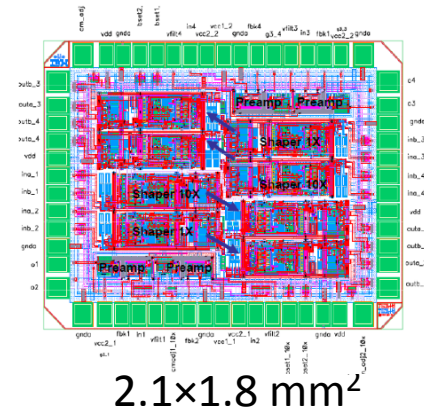
LAr Preamplifier and Shaper

Key requirements:

Preamp: 16-bit dynamic range, $e_{n,equiv}$ = 0.26 nV/√Hz, P = 42 mW
Shaper CR-(RC)^2: 16-bit (2 or 3 gain ranges), INL < 0.1%, Noise < 2.2 nV/√Hz, P ~ 150 mW

Two ASIC prototypes in Silicon Germanium.

1. **LAPAS**, 2 preamps, 2-1x and 2-10x shapers Fabricated in IBM 8WL process in 2008. Tested and reported at TWEPP 2008
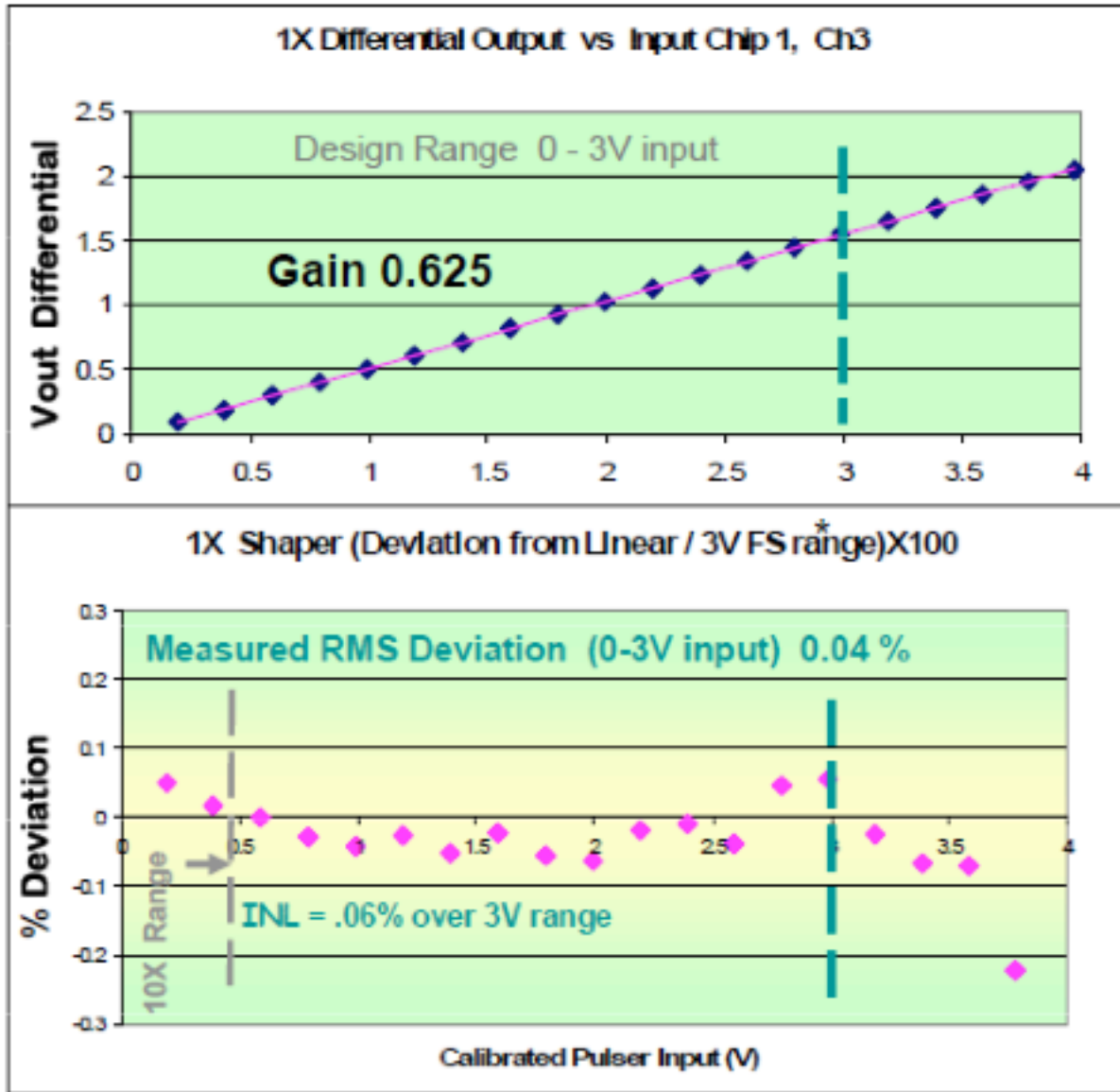

2.1×1.8 mm^2

2. **IHPPSD**, 2 preamps, 1x and 10x shapers Fabricated in IHP SG25H3P process in 2011 Tests interrupted by phase-I activities, resume in 2014.
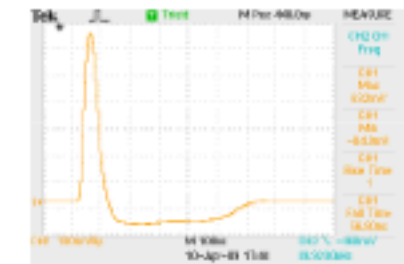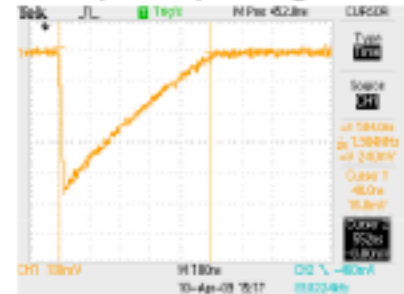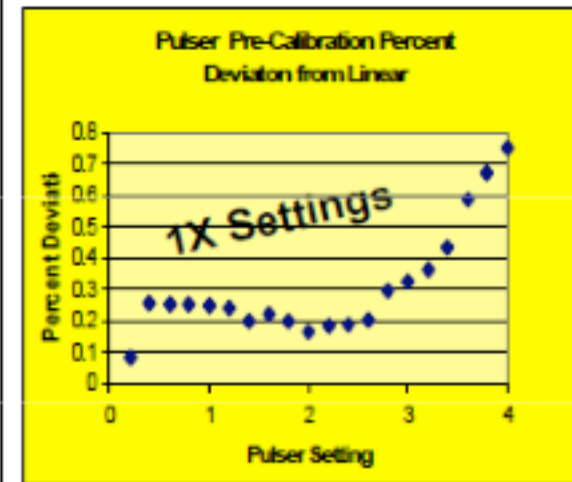

2.6×1.5 mm^2

LAPAS Test Results

1X Differential Output vs Input Chip 1, Ch3

Design Range 0 - 3V input

Gain 0.625

1X Shaper (Deviation from Linear / 3V FS range)X100

Measured RMS Deviation (0-3V input) 0.04 %

INL = .06% over 3V range

10X Range

Calibrated Pulser Input (V)
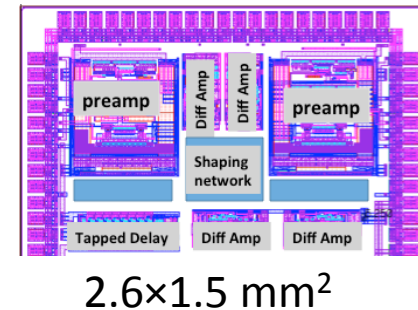
Shaper Input Signal

LAPAS Shaper Output

Pulser Pre-Calibration Percent Deviation from Linear

1X Settings

Pulser Setting

IHPPSD Preliminary Test Results
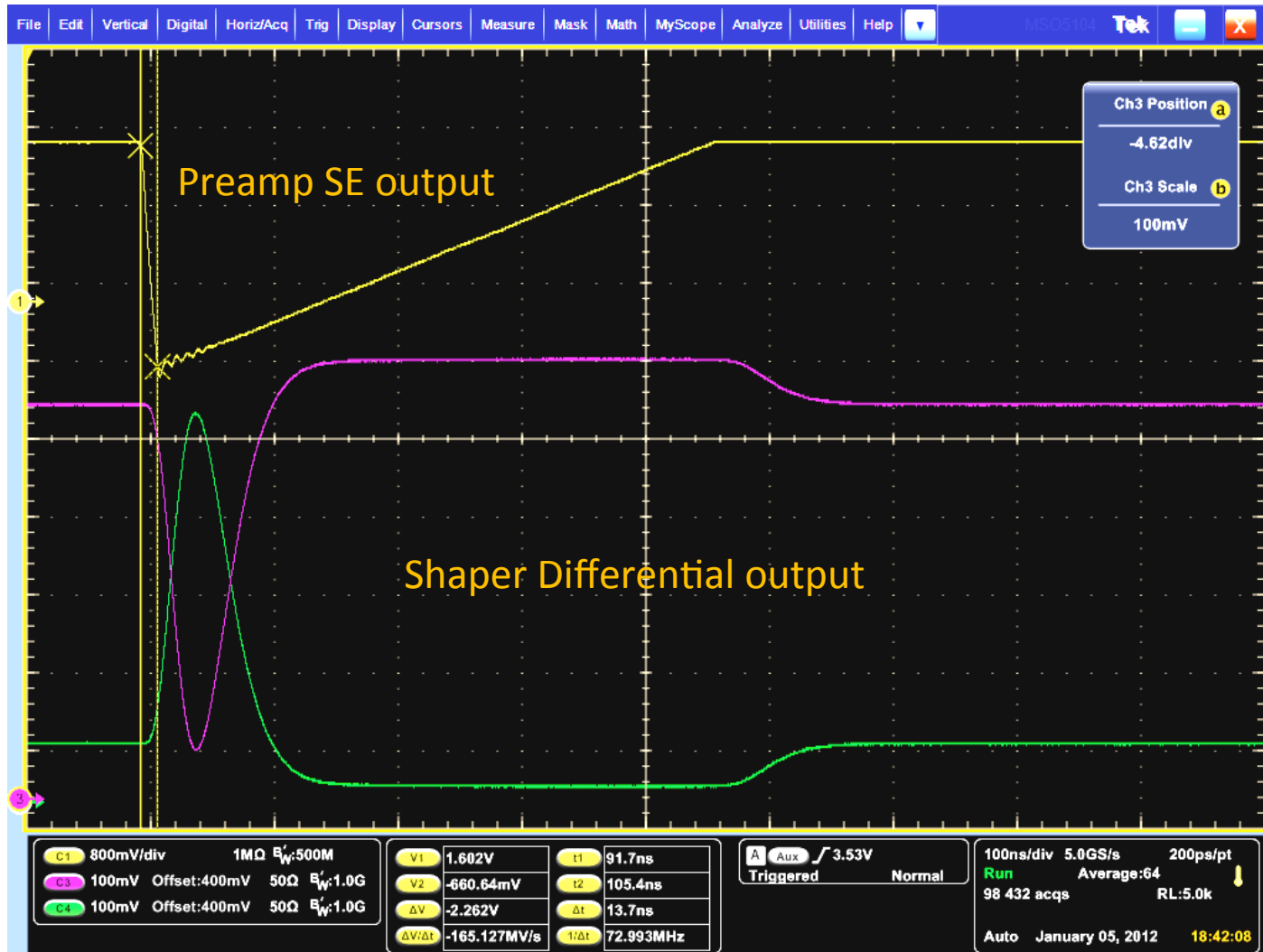
Preamplifier and Shaper Plan

2014 - Complete measurements of IHPPSD. Review Signal Processing approach in light of the present HL-LHC requirements.

2015 - Design/simulate/layout multi-channel prototype circuit.
- Investigate a 180 nm SiGe bi-CMOS process.
- Step through a circuit simulation and layout of the same circuit. Understand tradeoffs in noise, power and cost.

2016 - Submit Multi-channel design in the process of choice.
- Measure and plan for production version ASIC.

The ADC ASICs

Key requirements

16-bit dynamic range (matching w/ shaper gain ranges). 40 or 80 Msps (matching w/ optical link bandwidth). Power fits the current FEB cooling capacity.

Two approaches for phase-I, both with IBM 8RF 0.13 μm CMOS process. R&D needed beyond phase-I for phase-II.

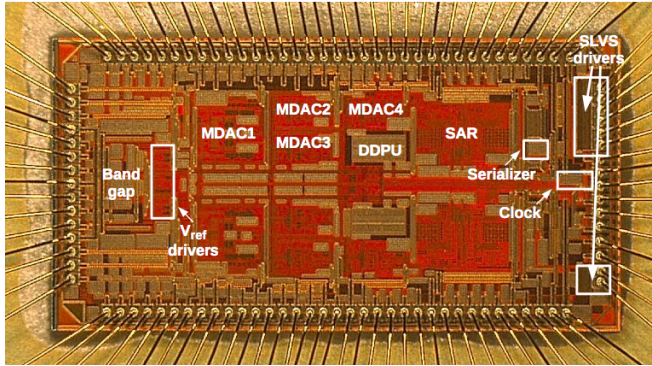**Nevis ADC**: pipeline (4-bit) + SAR (8-bit)

Two prototypes (10 and 12) tested. Nevis13, a quad 12-bit ADC prototype with I^2C interface, is in fabrication. Future plan driven by technology choice. May change architecture.

LPSC PEALL: SAR (12-bit)

Also two design iterations with preliminary test results. Future plan includes architecture change to Flash-SAR with redundancy and digital correction to reach 14-bit dynamic range.

Nevis12 ADC Test Results

- 4-bit pipeline + 8-bit SAR
- Effective number of bits 11
- Power < 50 mW/ADC channel
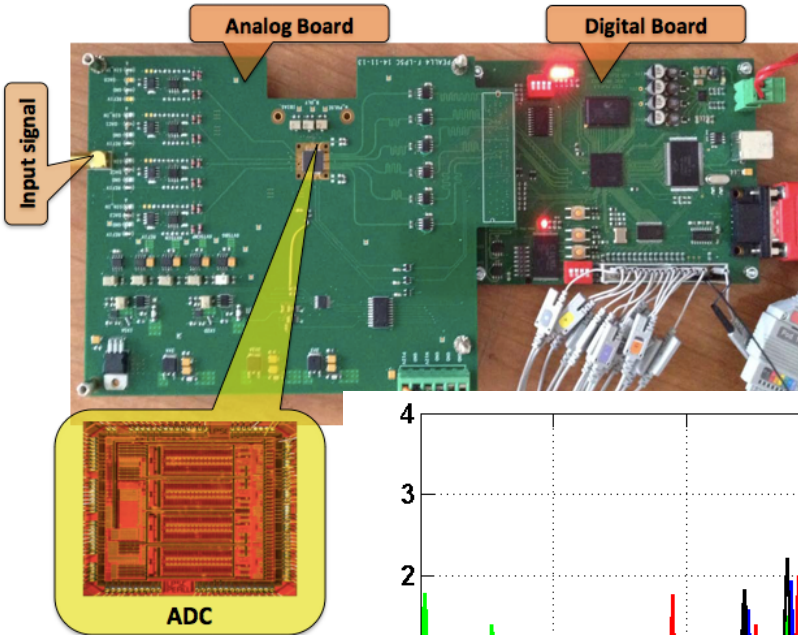- Serial output
- Finalizing SEE measurement

ATLAS Upgrade

SFDR: -79.37

SINAD: -67.90

SNR: -69.27

ENOB: 10.99

Spur Freq. [MHz]:

19.93   -79.37

10.36   -81.52

9.84   -81.62

19.80   -85.21

10.03   -87.92
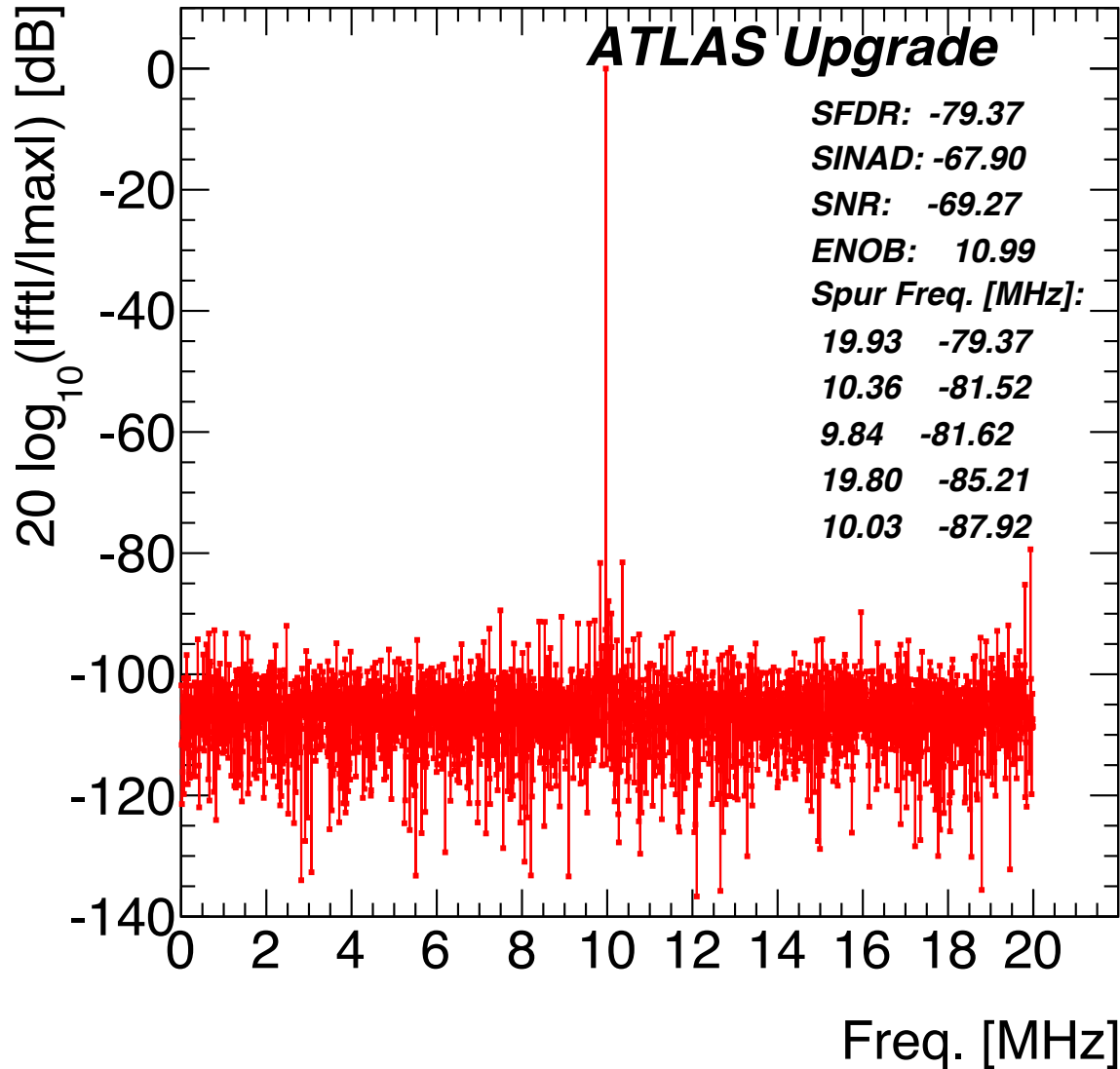
Nevis ADC Towards Phase-II

❖ **Still with IBM 8RF 0.13 μm CMOS:**
  - ❖ Use 3 gains and make a 12-channel chip (little R&D needed)
  - ❖ Add four more 1.5-bit stages in front (+ ~35 mW/channel) (little R&D needed)
  - ❖ Change pipeline stages from 1.5 bits/stage to 2.5 bits/stage. Can probably maintain 12-bit precision (limited R&D needed; new MDAC probably ~1 year of engineering)
  - ❖ Will we still have IBM CMOS 8RF for production?

❖ **Change technologies:**
  - ❖ 65 nm: "hybrid" pipeline+SAR still possible (but maybe not a good choice)
  - ❖ 65 nm or lower: full SAR, "fully digital ADC", i.e. digital error correction does everything
  - ❖ In either case, much lower power (~10 mW/channel?), but technology change implies substantial R&D needed

LPSC PEALL (2nd) Test Results

4 Channel 12-bit 40 Msps ADC with serial output
Die size: 2.8 x 3.4 mm^2

Total power (with Vref buffer): 27 mW/channel
Effective number of bits (ENOB) is from 8.8 to 9.2

Ongoing work on jitter improvement and on testing set-up

No SEE test yet.
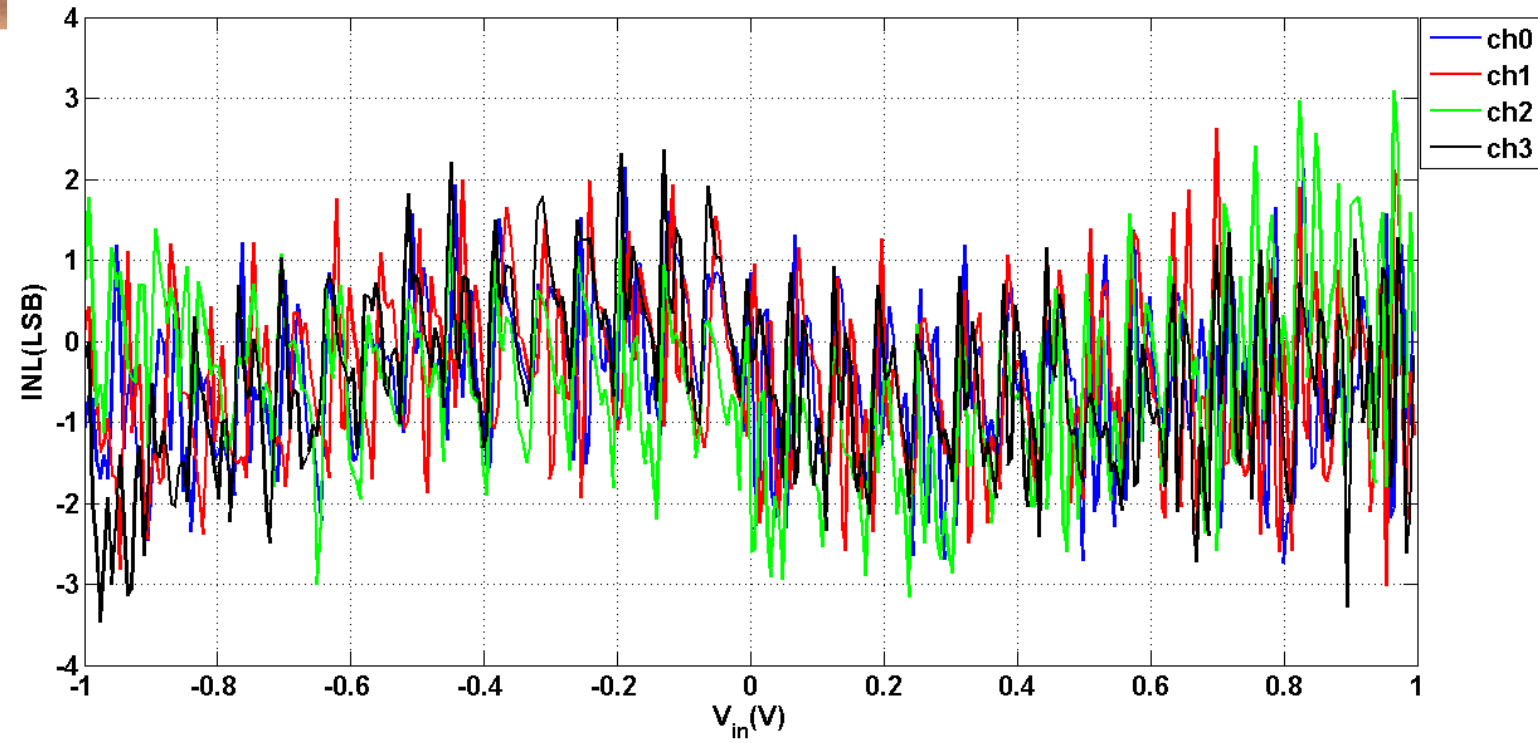
LPSC ADC Towards Phase-II

➢ Flash-SAR to reach 14-bit with redundancy and digital correction to go beyond the capacitors matching limitations. Current Simulations indicate that even 10% mismatch will be compensated and have up to 11.6 bits of ENOB with a 12 bit design.

10% mismatch effect in binary SAR
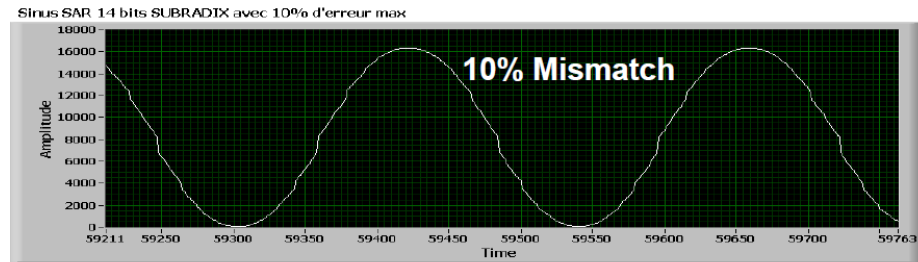
10% mismatch effect in redundant SAR + Digital correction
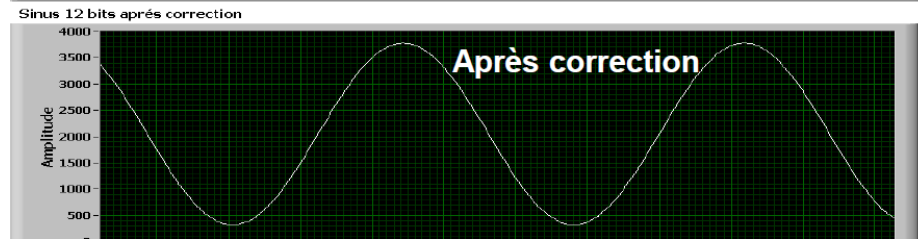
Output spectrum For the corrected redundant SAR codes
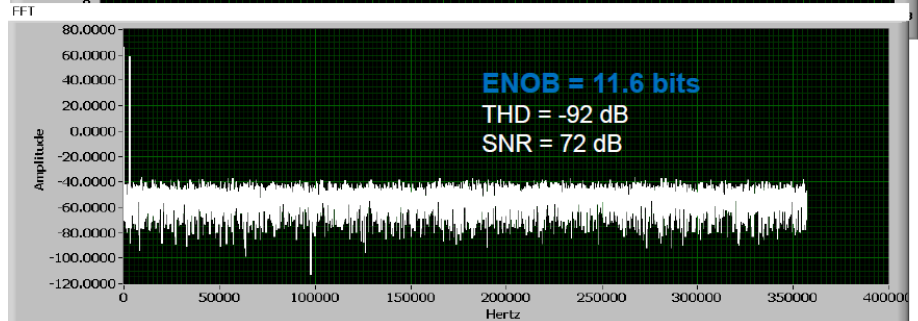
The Optical Link

1. Current efforts are for phase-I upgrade. The ASIC development is based on SOS 0.25 μm CMOS technology. The LOC ASICs reach 8 Gb/s transmission rate and is radiation tolerant for operations in LAr front-end.
2. For phase-II (HL-LHC), higher data rate (10 Gb/s) and lower power dissipation call for a change of technology (65 nm CMOS?) and taking full advantage of ASIC development, such as integrating the serial output of the ADC with the serializer of the optical link, sharing high speed clock synthesizers.

The LOC Serializer and VCSEL driver

LOCs2 prototype QFN-100 package
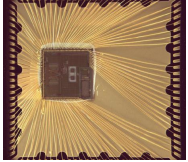
- LOCs2 is a 2-channel, 8 Gb/s per channel, serializer
- Its LCPLL tunes from 3.3 to 4.25 GHz with RJ ~ 1 ps.
- Power consumption 1.25 W for the chip with both channels run at 8 Gb/s.

LOCs2 eye diagram at 8 Gb/s
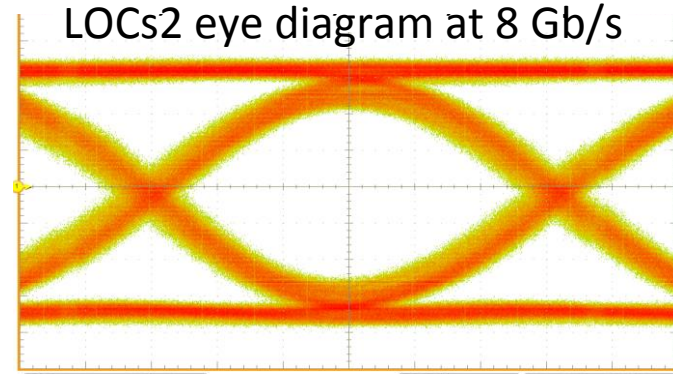
QFN-24 packaged LOCld1 with I^{2}C, two of them on MTx

Die, 8Gbps

MTX QFN, 8Gbps
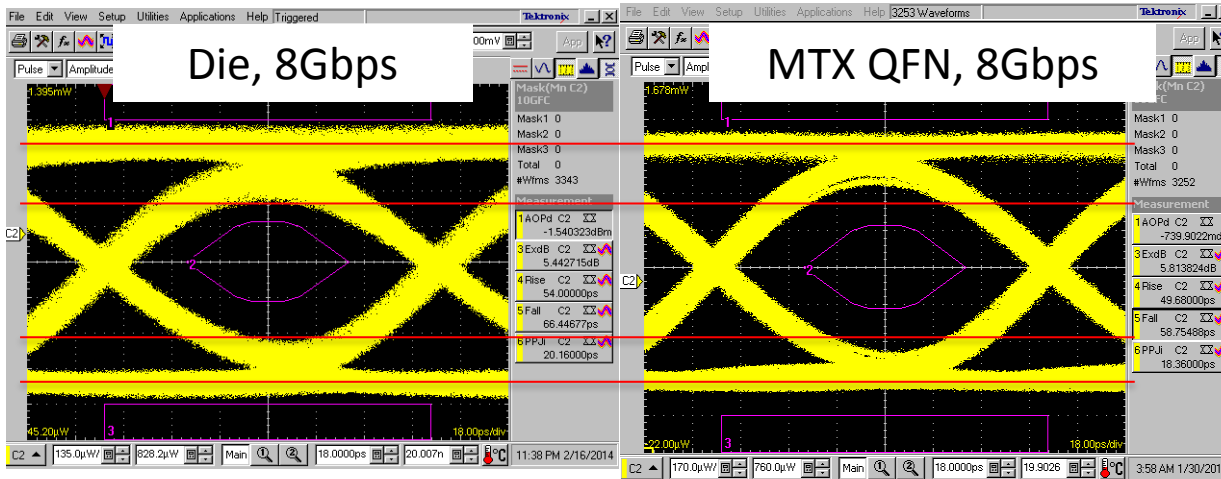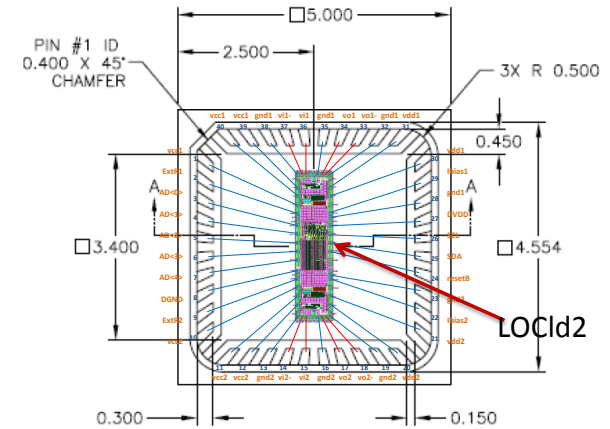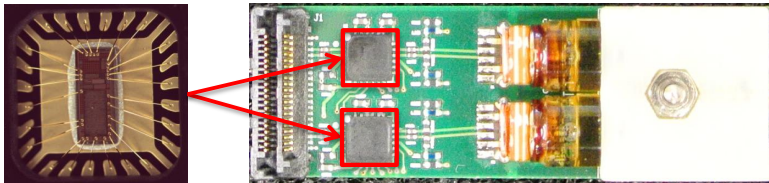
LOCld2

A dual channel version, LOCld2, to match the dual channel serializer, is in fabrication, will be tested in April to May.

The MTx (Miniature Optical Transmitter)

Idea from CERN SF-VTRx, the Versatile Link common project.
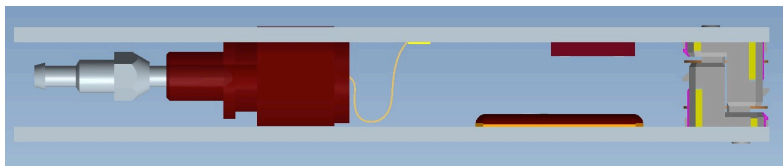
Comparison with SFP+

14 mm

6 mm
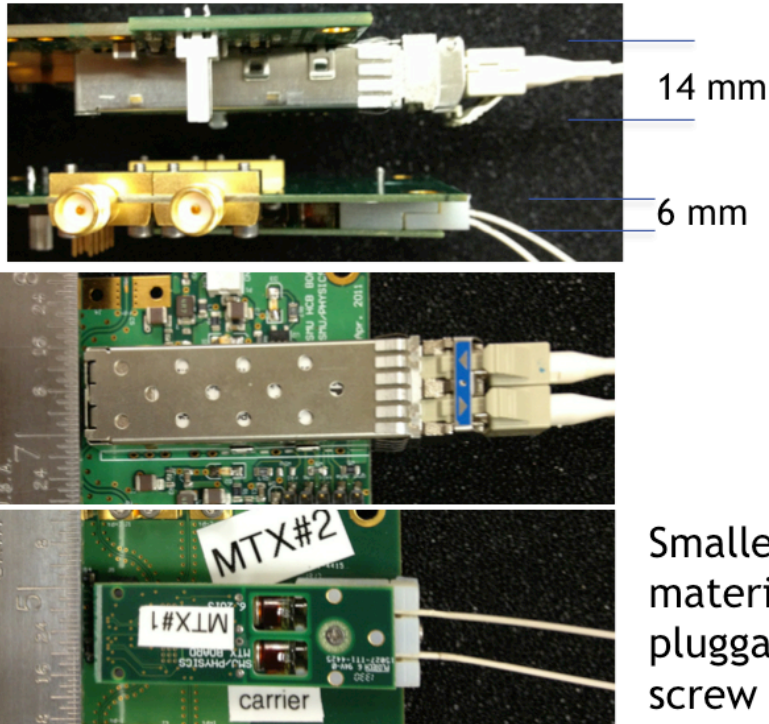
Optical coupling is guaranteed by the TOSA. Custom latch engages fiber with LC ferrule, spring and flange
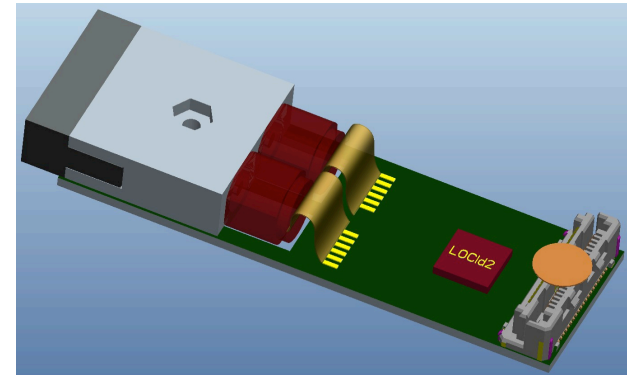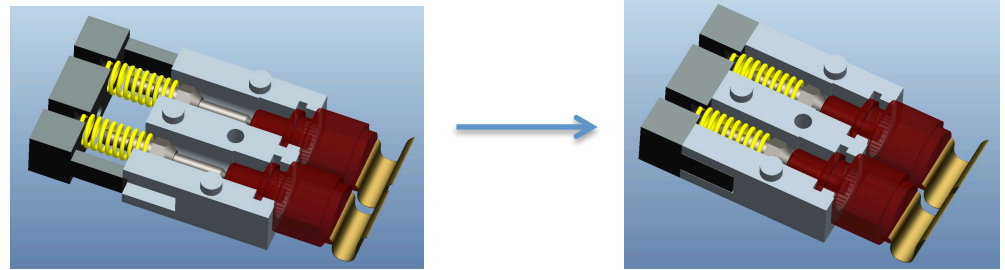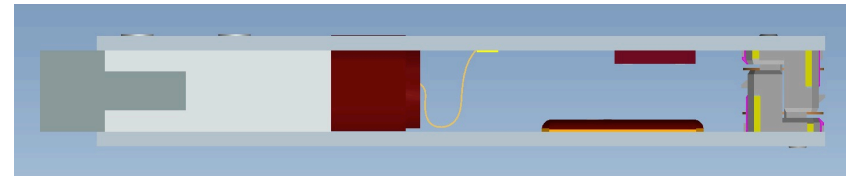

Smaller and less material. Fiber pluggable with a screw
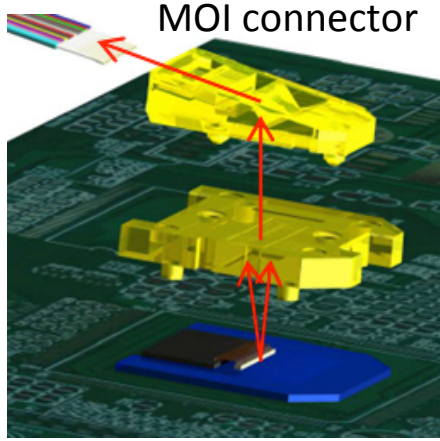
6 mm MTx

Mother board w/ serializer
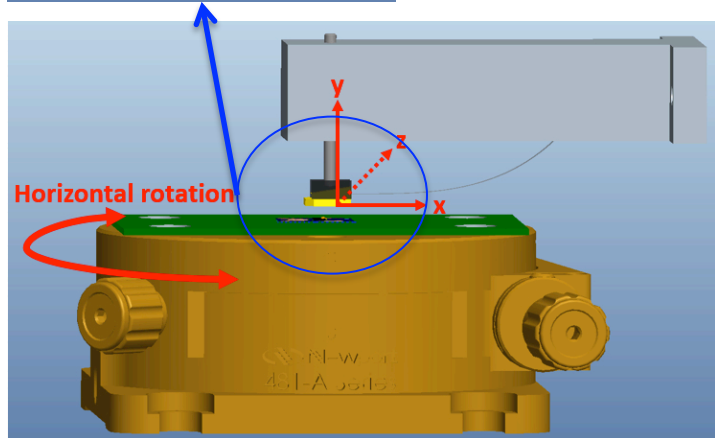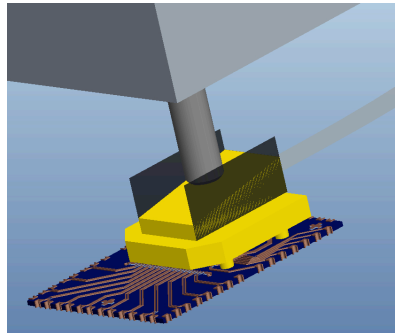Side view without the latch

Side view with the latch

An Attempt in Array Optics

MOI connector
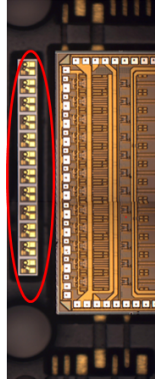
VCSEL array

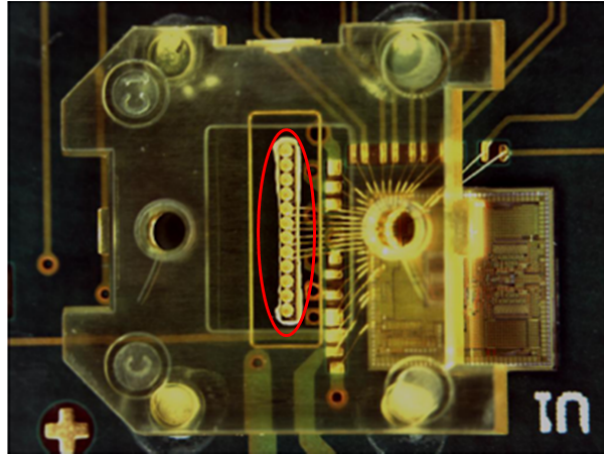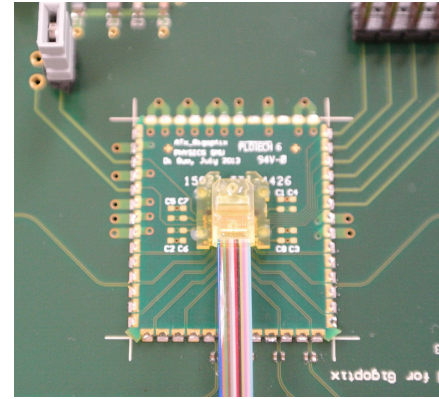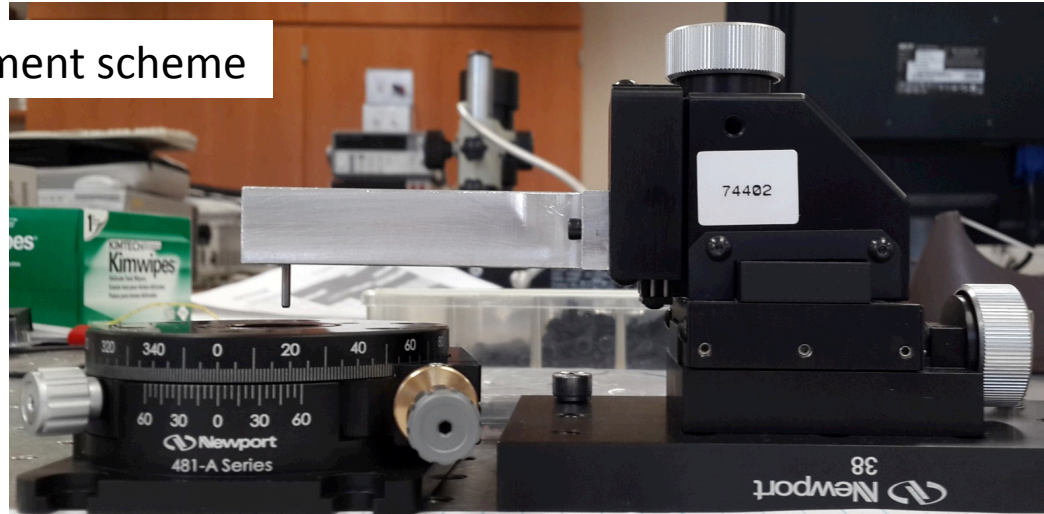Driver chip

Top view, VCSEL array, driver under MOI

Test PCB

One active alignment scheme

Horizontal rotation

Conclusions

1. ATLAS LAr Calorimeter readout needs upgrade for HL-LHC.
2. Component developments for the front-end are reported.
3. Some R&D work benefits from projects in phase-I (e.g., the ADC, the optical link).
4. Still a lot of work, but phase-II is fewer than 10 years away, leaving not much time for R&D, as the construction, installation and commissioning will take years.