The AMC13XG: A New Generation Clock/Timing/DAQ Module for (CMS) MicroTCA

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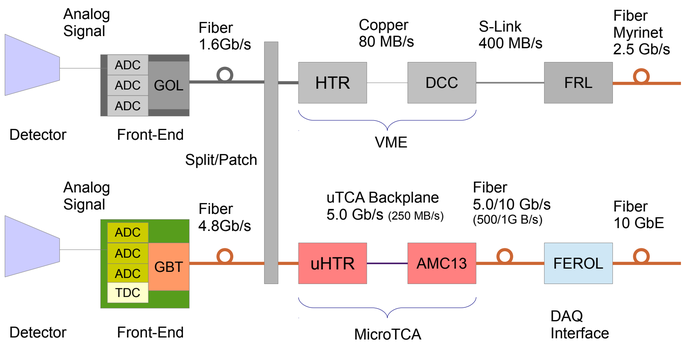
Detailed documentation at:
www.amc13.info

Motivation: HCAL Upgrade



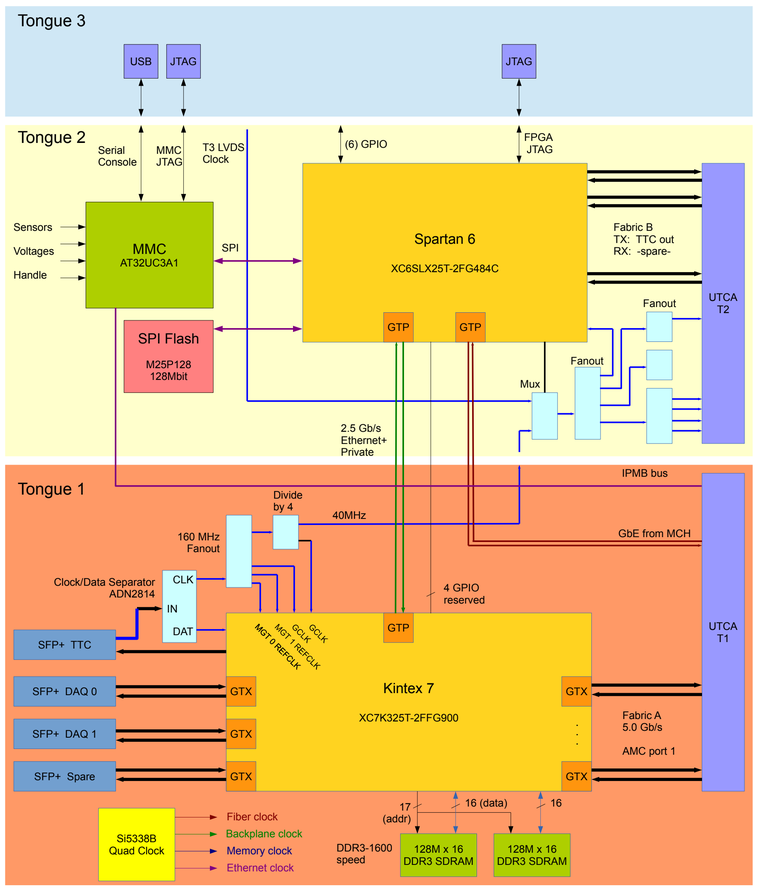
Observation: ***All subsystems need timing / DAQ services, So why not develop a common module?***

AMC13 Logic

The AMC13 provides clock, timing and DAQ service for many subdetectors and central systems in the upgraded CMS detector. This year we have developed an upgraded module, the AMC13XG, which supports 10 Gigabit optical fiber and backplane interfaces. Many of these modules are now being installed in the CMS experiment during the current LHC shutdown.

The AMC13XG mounts in the MCH2 site of a "dual-star" MicroTCA crate, and thus has point-to-point connections for clock and data fabrics to each of 12 AMC slots. The module is constructed as a stack of 3 PC boards (Tongues 1, 2, 3).

AMC13 Block Diagram



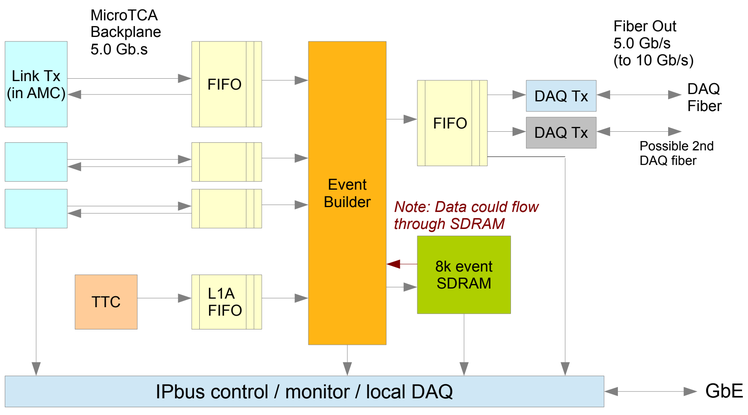
The AMC13 **Machine clock recovery** begins on tongue 1 with an optical receiver feeding an Analog Devices ADN2814 Clock and Data Recovery IC. This device process *i.e.* an LHC Trigger, Timing and Control (TTC) encoded stream and recovers clock and data. The clock (160MHz for the TTC case) is fanned out and delivered to several alternative clock inputs on the Kintex 7 FPGA on tongue 1 as well as to Tongue 2. The recovered data is sent to the Kintex 7 for further processing.

The AMC13 **clock fanout** is located on tongue 2. It can take input from either a front-panel input on tongue 3, or from the TTC receiver on tongue 1. The clock is fanned out to 12 AMC modules via the MicroTCA backplane as well as to the Spartan FPGA. From there it can be returned to the Kintex FPGA on tongue one for special applications.

The AMC13 **local clock** subsystem is quite flexible. A SiLabs Si5338B quad programmable "fractional-N" type clock synthesizer is used to generate four independent clocks. These can be used in addition to the TTC recovered clock to drive the backplane links, front-panel fiber links, Gigabit Ethernet and DDR3 memory.

The AMC13 **Module Management Controller** (MMC) is implemented with an Atmel 32 bit AVR microcontroller, with firmware developed by colleagues at the University of Wisconsin. In addition to required MicroTCA MMC functions, our MMC provides several extended features, allowing for fine-grained control over fault conditions, remote setting of module IP addresses and other parameters.

AMC13 DAQ Path

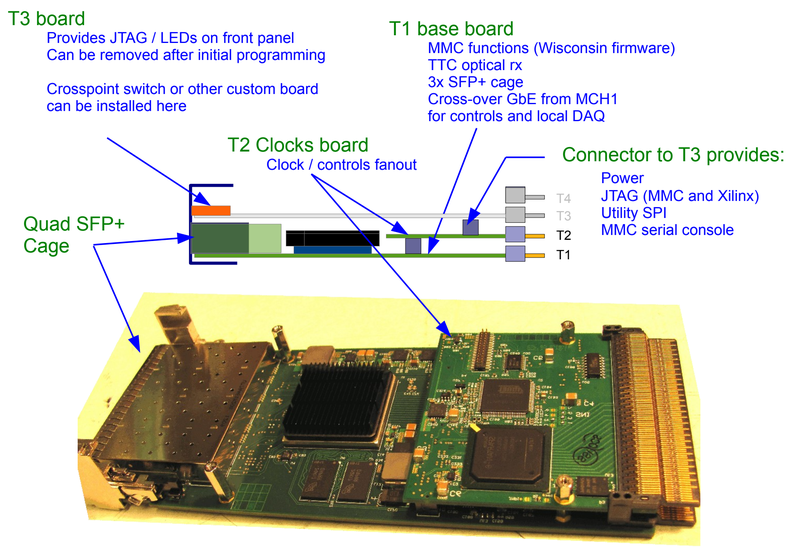


The **AMC13 DAQ Path** is detailed above. In response to each Level 1 trigger (L1A), each AMC card in the MicroTCA crate sends a CRC-protected packet over the backplane to the AMC13 at 5.0Gb/s. The packet has a header with event number, bunch crossing number and orbit number along with an optional subsystem-specific payload. The AMC13 event builder collects these packets and builds event fragments. The event builder output can be sent to one, two or three 5/10Gb fiber links to CMS CDAQ, and additionally to an SDRAM buffer which can hold several thousand events.

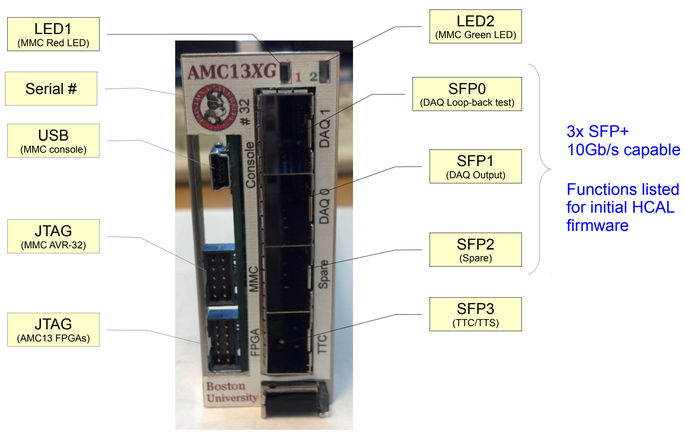
The SDRAM buffer may be prescaled, and may capture "windows" around events which exhibit specific error conditions. The buffer may be read out to a host PC over the 1GbE backplane link via the MicroTCA Carrier Hub

The AMC13 also supports **10GbE TCP/IP** readout on up to 3 links. A simplified subset of the TCP/IP protocol allows transfer at close to 1GB/s to a standard PC..

AMC13 Construction



AMC13XG Front Panel



AMC13 T1 Board

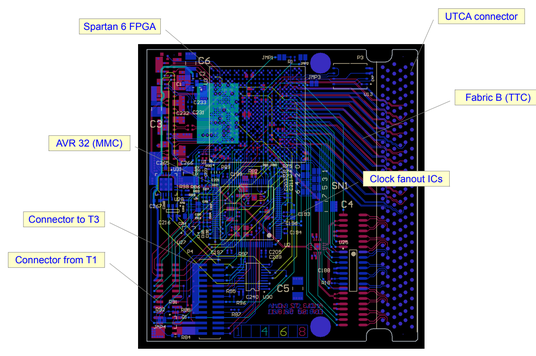
PCB Stackup

Nelco 4000SI-13

Thickness
Overall: 1.6mm
Signal: 18µm
Power: 36µm

1	GTL	Prepreg 2.7	Z0 ctrl (10G, SDRAM)
2	GP1	Core 5.0	GND
3	GP2	Prepreg 5.4	Split power
4	G1	Core 5.0	Z0 ctrl (SDRAM)
5	GP3	Prepreg 2.7	Split power
6	GP4	Core 5.0	GND
7	GP5	Prepreg 5.4	Split power
8	G2	Core 5.0	Z0 ctrl (SDRAM)
9	GP6	Prepreg 5.4	GND
10	G3	Core 5.0	Z0 ctrl (10G, SDRAM)
11	GP7	Prepreg 2.7	GND
12	GBL		Z0 ctrl (10G, SDRAM)

AMC13 T2 Board



PCB Stackup

FR-4

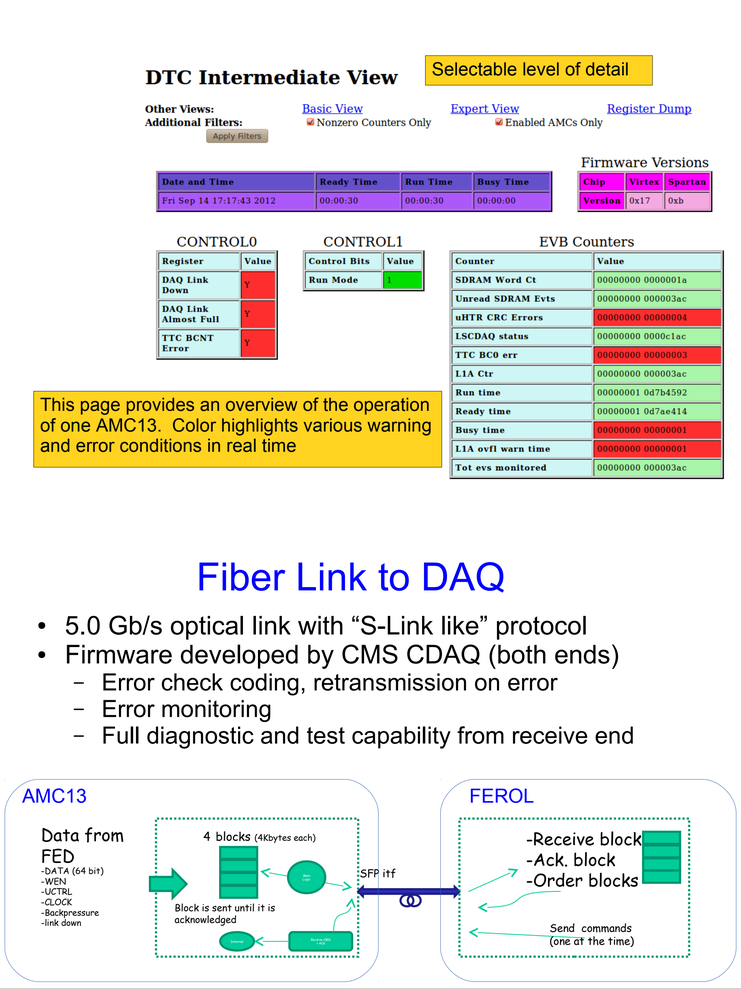
Thickness
Overall: 1.6mm
Signal: 18µm
Power: 36µm

1	GTL	5 mil dielectric	Z0 ctrl (TTC)
2	GP1	3 mil dielectric	GND
3	GP2	9 mil dielectric	Split power
4	G1	9 mil dielectric	Inner signal
5	GP3	9 mil dielectric	Split power
6	G2	9 mil dielectric	Inner Signal
7	GP4	5 mil dielectric	GND
8	GBL		Z0 ctrl (TTC)

AMC13 Software

A set of C++ classes is provided for full control of the AMC13. Command-line tools support testing and diagnostics. CMS xDAQ applications support operation and monitoring for CMS HCAL (currently) and generic CMS operation (soon).

A **HyperDAQ** web display provides real-time status during data taking.



Fiber Link to DAQ

- 5.0 Gb/s optical link with "S-Link like" protocol
- Firmware developed by CMS CDAQ (both ends)
  - Error check coding, retransmission on error
  - Error monitoring
  - Full diagnostic and test capability from receive end

AMC13 Test and Production

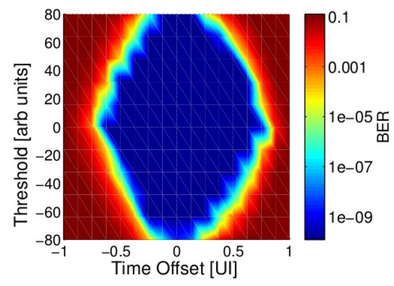
Estimated AMC13 Use through 2014

Experiment / Subsystem	No. AMC13	Special Requirements
CMS / HCAL	30	May require 2-3 x 10Gb/s DAQ outputs
CMS / Level 1 Trigger	36	Calo trigger: 6 EMU Track Finder: 3 Overlap region TF: 3 Barrel TF: 3 Global Trigger: 1 Spares, Test stands: 20
CMS / Pixels	6	TTC only, readout direct from FEDs?
CMS / TCDS	10	Custom T3 for front-panel clock and control inputs
G-2 (FNAL) / Tracker	3	Custom firmware
Total (est)	110	

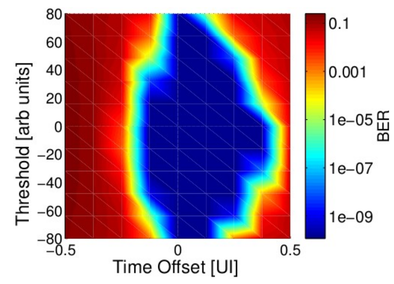
Serial Link Tests

These tests establish the reliability of the high-speed serial interconnections. In each plot, the horizontal axis represents the time of sampling of the serial data, with 0 representing the ideal time (middle of bit period). The vertical axis represents the threshold voltage used to characterize a bit as '1' or '0'.

Backplane Loop-Back @ 5.0 Gb/s
AMC Slot 1 (farthest from AMC13)



Fiber Optic Loop-Back @ 10.0Gb/s



Backplane Loop-Back Test – In this test a pseudo-random bit stream (PRBS) is sent down the backplane to an AMC slot, and electrically looped-back to the AMC13. This corresponds to **double the trace length** of a normal point-to-point connection.

Fiber Optic Loop-Back Test – In this test a 30m optical fiber is connected between an SFP transmitter and receiver, and a PRBS is sent through the fiber.

HCAL Slice Test

As a validation test of the MicroTCA readout system, the front-end data for the HCAL subdetector of CMS was split using optical splitters on the fibers from the on-detector electronics. Collider runs were taken in CMS and the data was compared byte-wise between the legacy VME electronics and the new MicroTCA system. An exact match was found in all data.

MicroTCA Crate at P5

Splitters installed on GOL links

Parallel readout in VME and uTCA

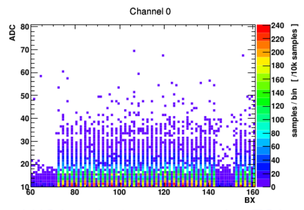
Events "tagged" by specific L1A ID (programmed HLT to save events)

xDAQ software to control uTCA

Results:

All data match perfectly!

HCAL uTCA Data!



LHC bunch structure seen in uTCA

AMC13 in CMS MicroTCA Crate