

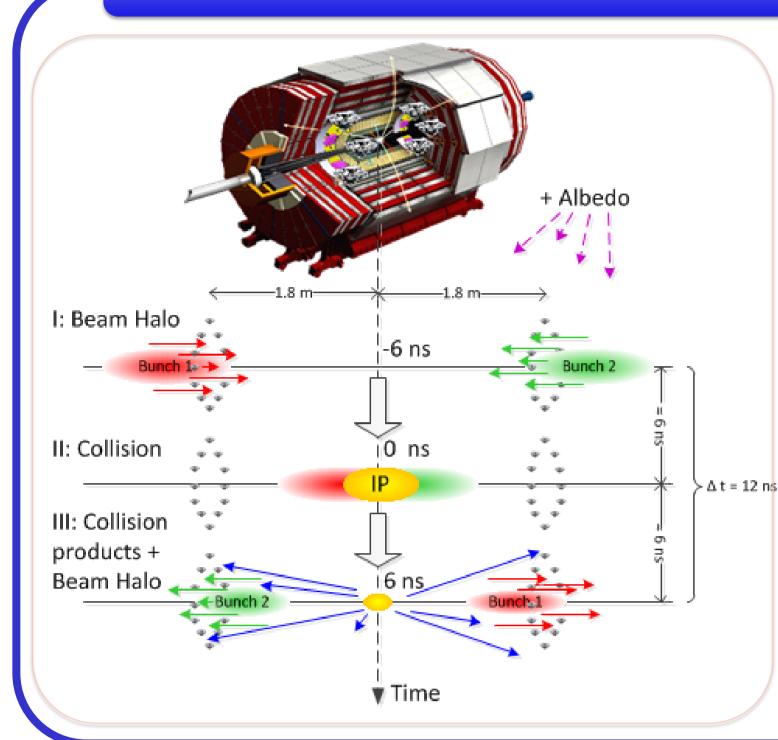
# **BCM1F Backend Electronics Phase 1 Upgrade for Beam Conditions and Luminosity measurement**

A.A.Zagoździńska, on behalf of the CMS Beam Radiation, Instrumentation and Luminosity Project (BRIL) CERN, Geneva, Switzerland



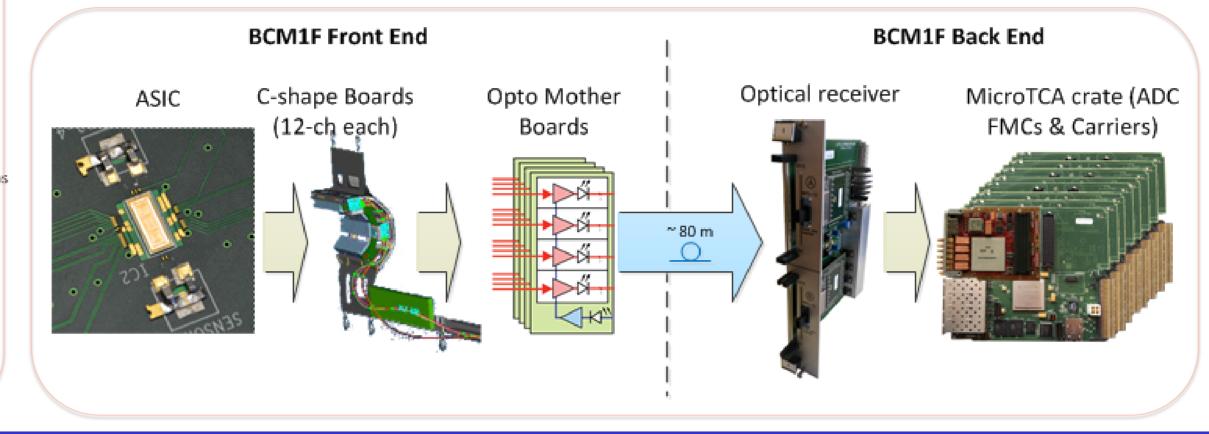
The Beam Condition Monitoring (BCM1F) system is a part of the CMS Beam Condition Radiation and Luminosity Project (BRIL). The BCM1F is designed to monitor the flux and timing of charged particles originating from beam halo and collision products using 12 single crystal CVD diamond sensors positioned at a distance of  $\pm 1.8$  m from the interaction point. Signals from the detectors are shaped and amplified by a custom designed ASIC and transmitted through optical fibers. The BCM1F Backend Electronics are designed to receive signals from the Front-end Electronics via 48 optical channels at very high input rates (e.g. for 50 pile-up collisions the expected rate is about 270 MHz) from the Front-end Electronics. The online and offline data analysis will provide information about collision, beam halo and albedo rates. The system will be based on AMC modules with a microTCA chassis. Two architectures are considered. Both are using 4 channel ADC FMC mezzanines for signal digitizing at a sampling speed up to 1.25 GSps per channel. Samples will be processed in FPGAs on AMC carrier boards, of which there are two types available: GLIB designed by the CMS collaboration, and AFC AMC available as an Open Hardware Project supported by the Warsaw University of Technology. Both carrier candidates are compatible with AMC13, which is a CMS specific microTCA Carrier Hub (MCH) and can drive the FMC ADC. The data will be processed, put into histograms and sent to the BRIL data acquisition system. The data processing speed is limited by the FPGA capabilities, hence data buffering will be required. Some amount of raw data will also be stored for offline analysis. One branch of the system is designed to collect the BPTX signals with the highest possible sampling rate of 5GS/s provided by the ADC in a single-channel mode. In this case, only one channel of the ADC FMC can be used. The data flow in the system is crucial and can be designed in different ways. Depending on the final architecture, the most capable and stable configuration will be chosen. The performance of the system, its architecture and the algorithms under consideration for data analysis, are presented.

## **Overview of the CMS BCM1F System**



- Sensor type: single crystal CVD diamonds
- Position z: ±1.8 m from interaction point
- Number of sensors: 12 double-pad per end (48 channels in total)

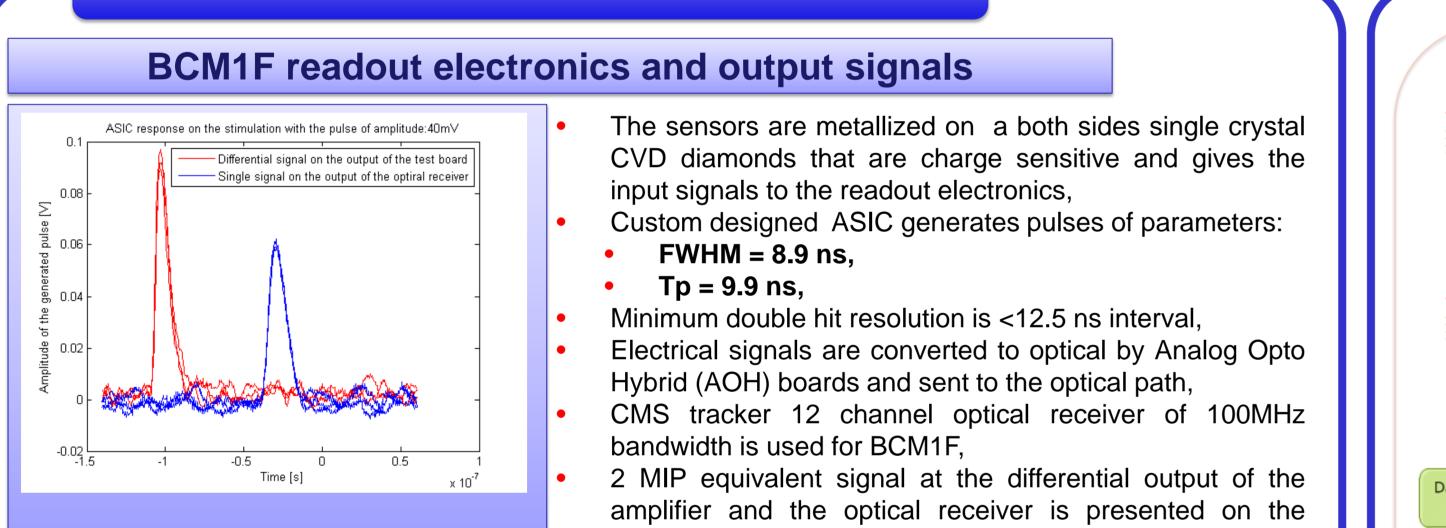
**ABC hits:** Diamonds installed around the beam pipe detect particles of that can be Beam Halo, Collision products or Albedo hits. Distinguish between them is essiential to get the high precision of luminosity measurement.



channels

Diamonds and custom design ASICs<sup>(1)</sup> will be installed on 4 C-shape boards. Analog signals will be transmitted to 4 Opto Mother Boards and converted to the optical signals. Fibers will lead signals from experimental cavern to the counting room where two 24-channels optical receivers will convert them back to analog. Signals will be sampled by high-speed ADCs mounted on the FMC mezzanines. 8-bit, 5GSps/4-channel FMC125(4DSP) or 10-bit, 5GSps/4-channel FMC126(4DSP) are being considered. AFC FMC carriers will collect data, process and histogram it. Two types of histograms will be collected: total number of counts (hits) in time and total number of counts in amplitude. Hits will be assigned to the orbit, bunch crossing number and will get a time. High resolution of distinguish between bunch and albedo hits is crucial. The algotithm cannot introduce the dead time. Collected data will be and sent to **BRIL DAQ**. Additional task for the Back End is BPTX signals measurement and integration. The system will be also in charge of Front End configuration.

# **BCM1F Hardware**

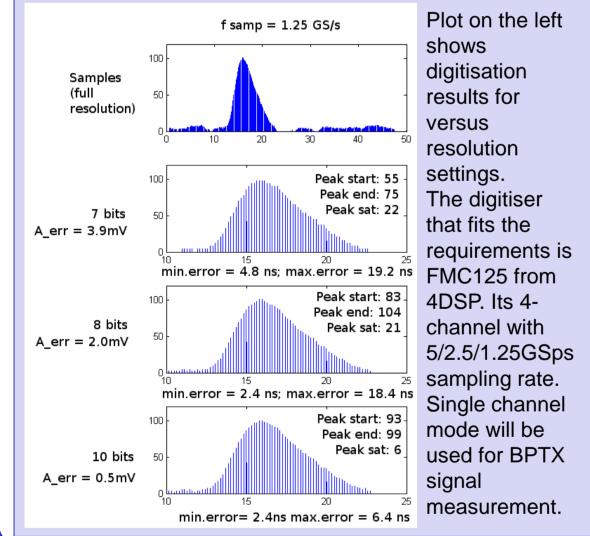


#### MicroTCA crate no.2 MicroTCA crate no.1 **Data rate estimation** LHC Clock ADC LHC Clock— Input Data: • 8 bits @1.25 Gsps (f<sub>s</sub>) with 1:2 DMux AMC FMC carrier AMC FMC carrier Received with DDR @625 MHz • 8 samples in parallel @156.3 MHz • Single orbit is 110-120 kS Raw Data One orbit takes ~1 Mbit/ch -LHC Clock- ADC Possible to store 4 channels at the

# **Backend Electronics architecture**

- picture on the left side.

### **Analog to Digital**



**FMC AMC carriers** 

Two architectures of the system are considered: based on CMS recommended components and based on Open Hardware Repository (OHWR) Components. There is a set of requirements for AFC FMC carriers:

- Minimum 1 FMC slot in HPC version
- Backplane connection: port 3 available for TTC signals distribution
- Ability to process 20GBps of incoming data
- Drivers for peripherials available, high speed comunication via backplane



GLIB board is easly accesible in CMS and communication with TTC distribution module (AMC13 MCH2) was tested. It offers complex software and firmware libraries with IP bus communication integrated. Its resources are more limited and only one FMC slot is possibe to use for ADC FMC mounting, but it fits BCM1F requirements. The second option will be used if GLIB will be insufficient.

# **Software / Firmware**

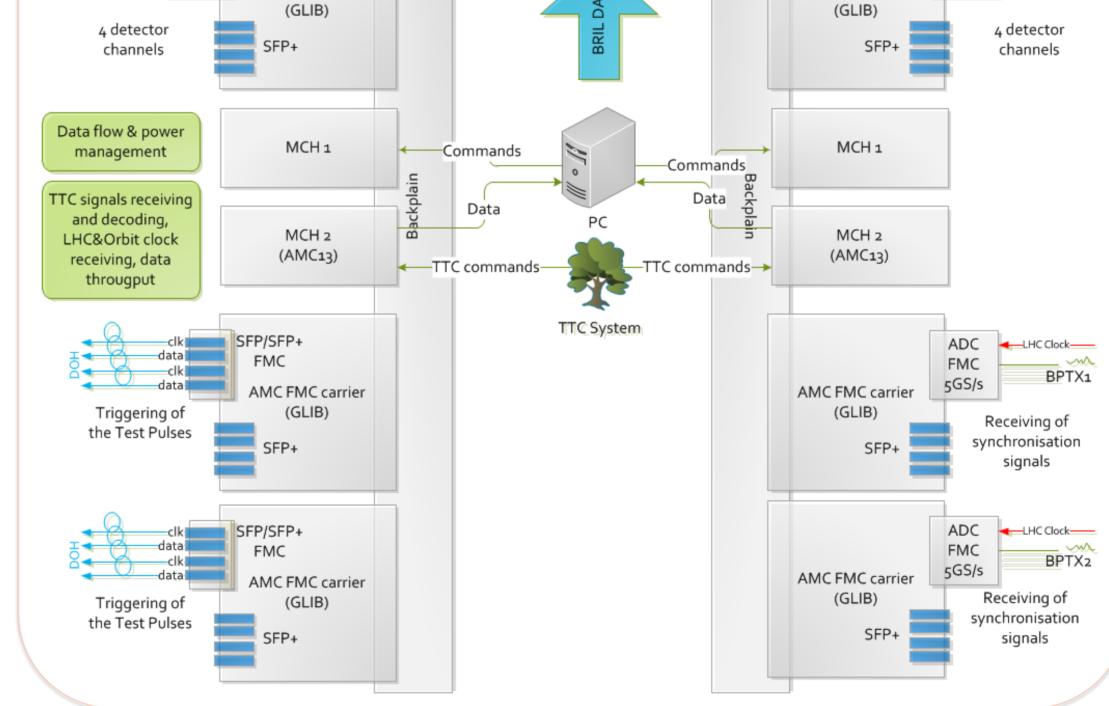
SW/FW of the Back End electronics is based on CACTUS repository that is provided with a GLIB board. Software is developed in C++ and allows programming, managment and communication with boards via IPbus. It will provide the local data presenting as well as efficiency estimation. Separate FW modules are beeing developed for BCM1F, BPTX measurement as well as slow control of the Front End.

#### Types of the histogramming modules:

✓ **BRIL DAQ:** Total number of hits vs amplitude

#### Slow control architecture

Designed to manage remotely the Front End. Data and 40MHz



same time (50% of FPGA resources) Average data production speed 480 Gbps • Data readout speed - IPbus limit over 1 GbE: 500 Mbps • Possible to read out 1 orbit every 1000 Amplitude Histograms: 256 bins (at full ADC resolution) 120 kS/orbit. 2^12 orbits/nibble. fits in 32 bits/bin • 8 kb/channel, 32 kb/board, 384 kb/crate. Storage on FPGA requires twice as much memory due to double buffering (64kb/FPGA) • Readout every nibble ~1 Mbps Time domain Histograms: • Optimized, with 8 bins/bx (30k bins) • 2^12 orbits/nibble, fits in 16 bits/bin • 500 kb/channel, 2 Mb/board, 24 Mb/crate Storage on FPGA requires twice as much

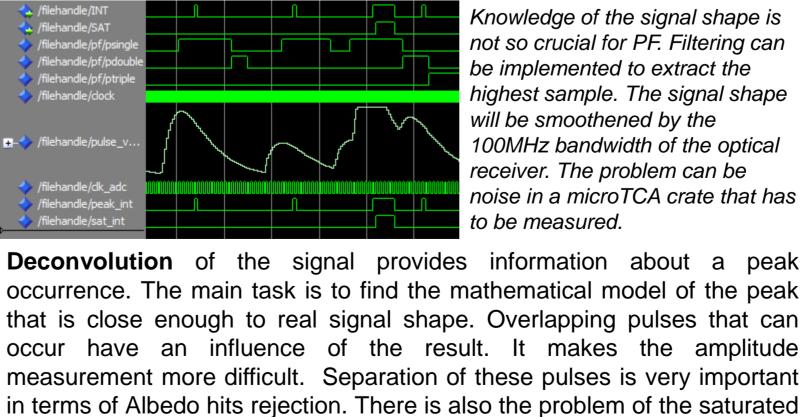
- memory due to double buffering (4Mb/FPGA)
- Readout every nibble ~70 Mbps

Collected data will be transmitted to the local PC and LumiDAQ via the backplane of the crate and optical links from AMC13 (MCH2) board. Transmision protocol is IPBus.

# Peak measurement algorithm

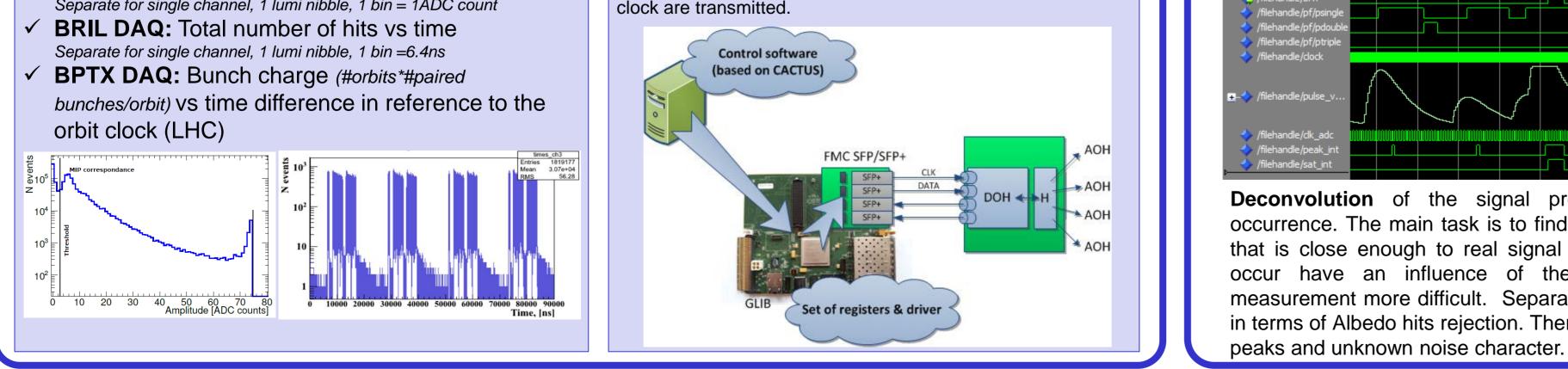
Limited resources and a very high volume of data producing will limit possibility of the complex algorithm implementation. The algorithm has to provide realiable amplitude and time measurement. Results will be collected in histograms and sent to the local BRIL DAQ. Small amount of RAW data (called spy data) will be transmitted for algorithm efficiency measurement. Two simple algorithms are taken into account: peak finding and deconvolution. They are tested with data measured in different conditions. Peak finding (PF) is the naive algorithm that can be

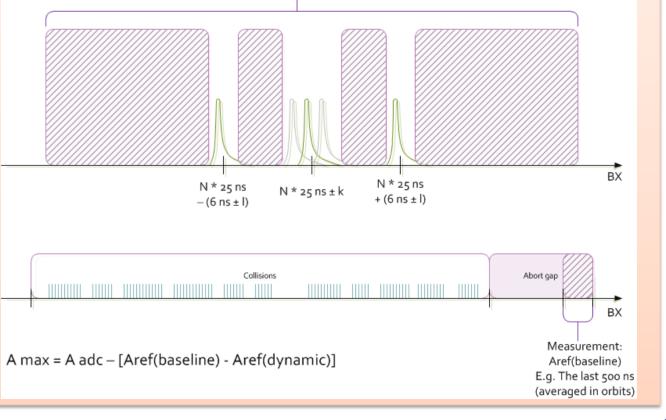
easly implemented. It can provide fast peak recognising on the basis of several consecutive samples. The problem is definition of the saturation and its high sensivity to noise. Distinguish between the overlaping samples with 6ns spacing is possible. The algorithm is very sensitive to the noise and pulse saturation.



Baseline measurement will be done during the last 50 ns of the abort gap and repeated every orbit. Averaged value Aref(baseline) will be taken into account. There is a possibility of Aref(dynamic) measurement during collisions. Amplitude of pulses Aadc will be corrected with the value of baseline Aref(baseline)- Aref(dynamic).

- Aref(dynamic)





- BCM1F is a part of the CMS BRIL project for beam monitoring and luminosity measurement, it will provide information about Albedo, Beam Halo and Collision hits,
- Architecture of the system follows CMS recommendation and introduces some custom solutions that will allow fast signals measurement and accurate luminosity measurement. The system elements are being tested for system compatibility and possibility of usage in the real system,
- Algorithm for peak recognition is developed on basis of previous BCM1F experience and current Front-End measurements,
- The basic functionality will be provided before 2015, system firmware and software will be developed according to the first commisionning results.

<sup>(1)</sup>See poster of D.Przyborowski "Design of a Front–end ASIC for Single Crystal Diamond Sensors" in this workshop