First Test Beam measurements of BCM1F back-end phase 1 upgrade, using the FMC125 Fast Digitizer

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Introduction

- Upgrade of the CMS **Fast Beam Condition Monitor (BCM1F)** for luminosity and beam background measurements during CMS phase 1 upgrade, in the context of the **Beam Radiation Instrumentation and Luminosity (BRIL)** project.

- Increase the number of diamond sensors to 24 with split metalization, placed 1.8 m from the interaction point in CMS, around the beam pipe and about 7 cm from the beam line.

- Tests performed in January 2014 at DESY Hamburg of the full measurement chain with new front-end ASICs having improved timing parameters: a peaking time and FWHM of less than 10 ns, allowing identification of two MIPs with 12ns of separation.

- Test beam was supported by AIDA project.

Goals of measurements

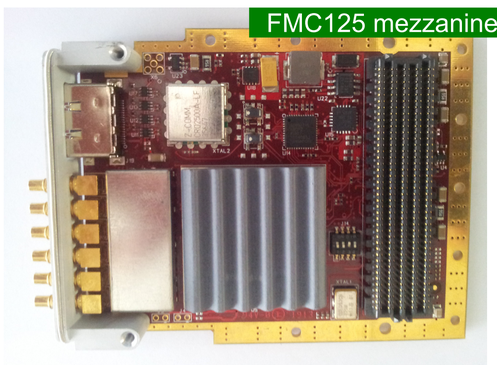
- Check fast FMC125 – ADC mezzanine card in terms of meeting the timing criteria of the system.

- Test front-end ASIC.

- Compare data from split (2-pad) and single pad diamonds.

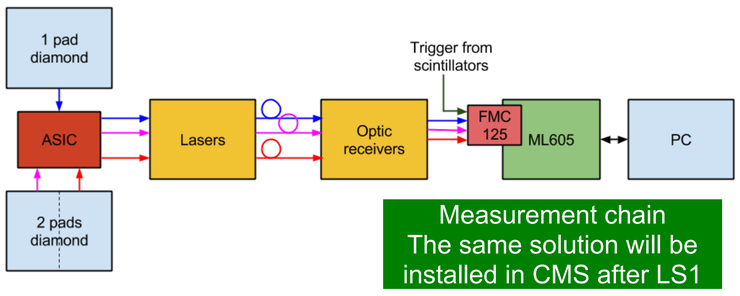
FMC125: ADC

The digitizer under consideration is provided by a 4DSP mezzanine FMC card with an 8-bit, 4-channel ADC, with sampling 1.25 GS/s per channel and AC coupled input. Recorded ADC values are transferred into 1:2 demultiplexed mode to the FPGA on the carrier board. For these measurements a ML605 Xilinx Development Board with Virtex6 was used.

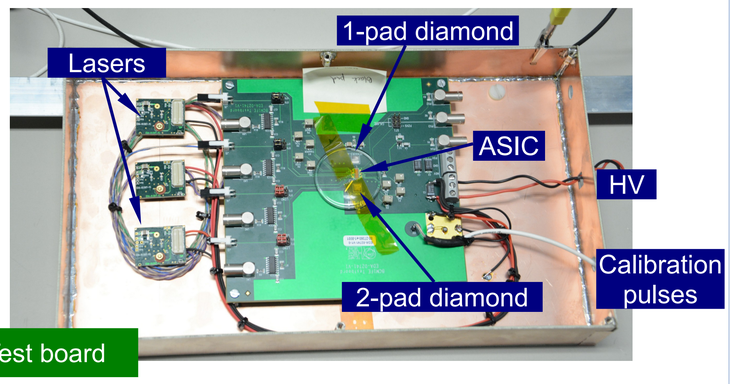


FMC125 mezzanine board from 4DSP

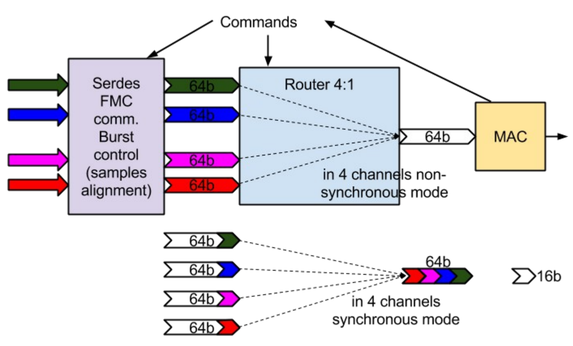
Measurement setup



Measurement chain
The same solution will be installed in CMS after LS1

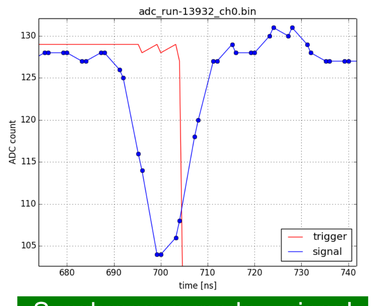


Test board



FPGA firmware:
- 4 channels non synchronous mode: 1.25GSps (0.8ns)
- 4 channels synchronous mode: effective 312.5 Msps (3.2ns)

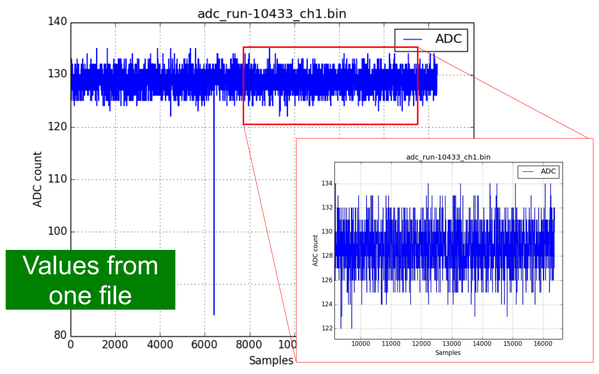
First step was to collect data in synchronous mode: ADC channel A of ADC was connected to a trigger, the other channels were connected to signals from 1-pad and 2-pad diamonds. It caused slower effective sampling speed of the signals than using 4 channel non-synchronous mode, where all data from one channel were registered.



Synchronous mode – signal registered with respect to the trigger

All of the signals collected in synchronous mode were with respect to a trigger. Based on that, we made an assumption that signals registered in 4 channel non-synchronous mode were also in respect to the trigger.

Baseline and Noise distribution



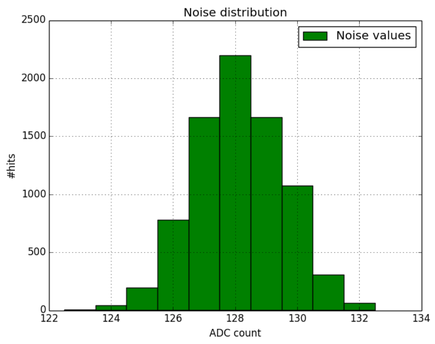
Values from one file

Results

Baseline was calculated for each file as a mean of 8000 samples. Signal peaks were excluded from the baseline calculation.

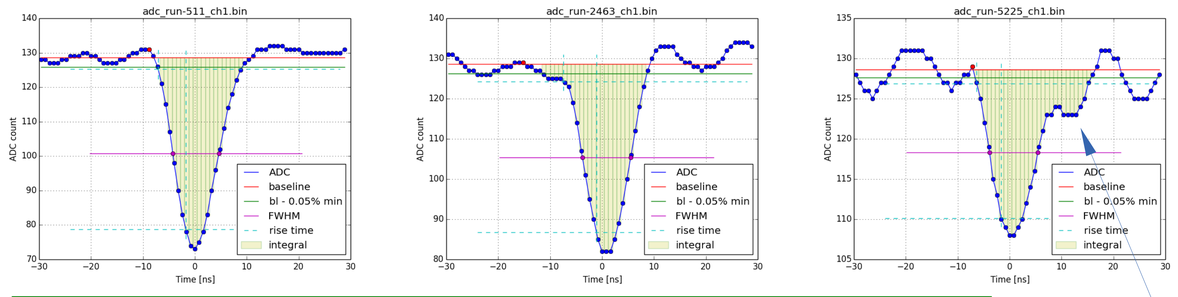
Baseline value was 128.4±2.5 ADC counts (0±4.88mV), close to the middle of 8-bit resolution range.

In the plot to the right we show the noise distribution for all channels. It is narrow (±2.5 ADC counts), symmetric and with a dominant middle value.



Noise distribution for all channels

Pulse shape



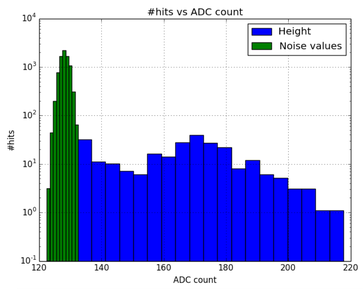
Pulses shapes with indication of calculated parameters registered during test beam

In these plots example signal pulses with maximum time resolution (0.8ns sampling period) are shown.

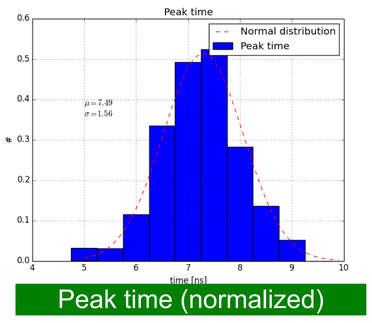
A postprocessing software trigger was set to 120 ADC to select signal pulses. We calculated the height of a pulse, a rise time, peak time, FWHM and integral under a peak.

Some of the peaks have smaller pulses, just after main one.

Pulse parameters



Height of pulses in log y scale

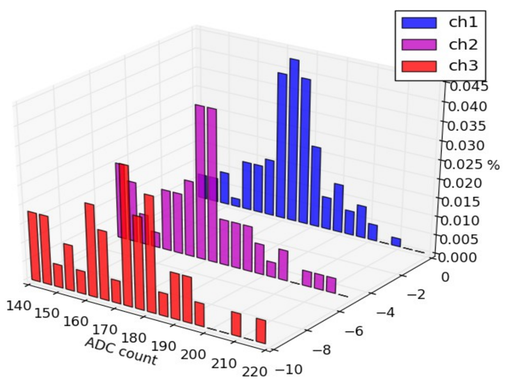


Peak time (normalized)

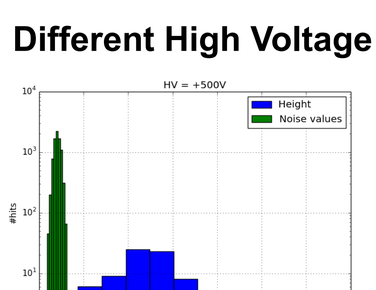
Height was calculated as a difference between minimum and baseline.

The plot on right presents height distribution for 3 channels:
- ch1 – 1-pad diamond
- ch2 – 1st pad of 2-pad
- ch3 – 2nd pad of 2-pad

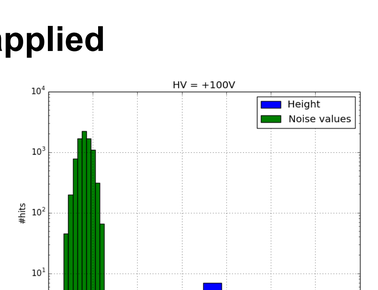
The average peak time, the time difference between maximum before a pulse and minimum of a pulse, was 7.49±1.56ns.



Height distributions for 3 channels



Rise time (normalized)

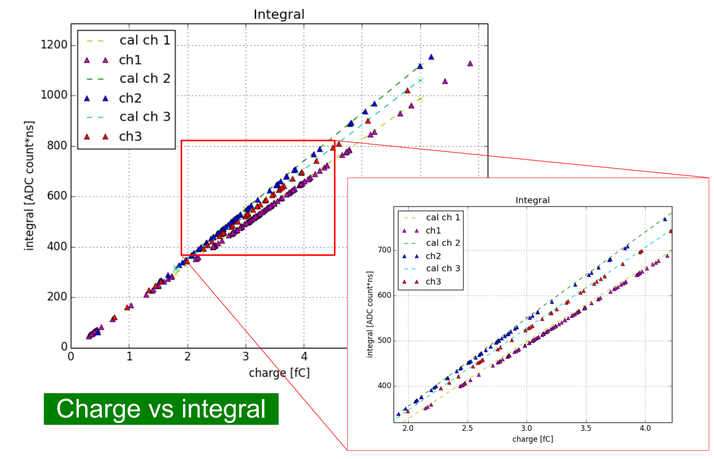


FWHM (normalized)

The rise time is the time required for the response to rise from 10% to 90% of its final value[1]. Measured value is 5.46±1.40ns.

FWHM – Full Width at Half Maximum describes the width of a pulse. Small values of this parameter give better sensitivity to overlapping pulses. This value was 9.26±1.90ns.

Calibration

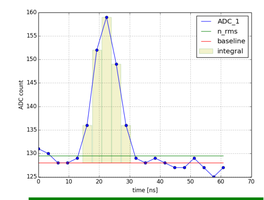


Charge vs integral

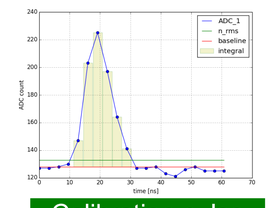
Calibration was performed to determine the dependency between input step test pulse amplitude (and in consequence test charge) and the ADC count value:

Ampl [mV]	Charge [fC]	ADC count
30	1.8	34
50	3.0	62
100	6.0	114

Also between input step test pulse amplitude (test charge) and integral under pulse, which is presented on a plot to the left.



Calibration pulse 30mV, ch A



Calibration pulse 100mV, ch A

Different High Voltage applied

Height distributions for different HV applied: +500V, +100V and -500V

During measurement different High Voltages were applied: +500V[1)], +100V, -350V, -500V[1)].

[1)] Only for 1-pad diamond

Conclusions

- These measurements show good separation between signal and noise.

- The low intensity beam (around ~= 100-300Hz) and free trigger running firmware, resulted in an extremely low data gathering efficiency = 0.1%.

- Data collected with 4 channels in non-synchronous mode were the most accurate in terms of timing.

- Pulse parameters recorded in 2-ch and 4-ch synchronous mode are in range of values recorded in 4-ch non synchronous mode.

Achievements:

- Sensor and front end characterization.

- FMC – ADC works.

- Solid base to develop firmware for the CMS installed system.

Literature:

[1] Levine, William: *The control handbook*, Boca Raton 1996

Thank you Erik Van Der Bij for lending ML605!

PB @ 2014