Design of a Front–end ASIC for Single Crystal Diamond Sensors

Application as Beam Condition Monitors in CMS and LHC

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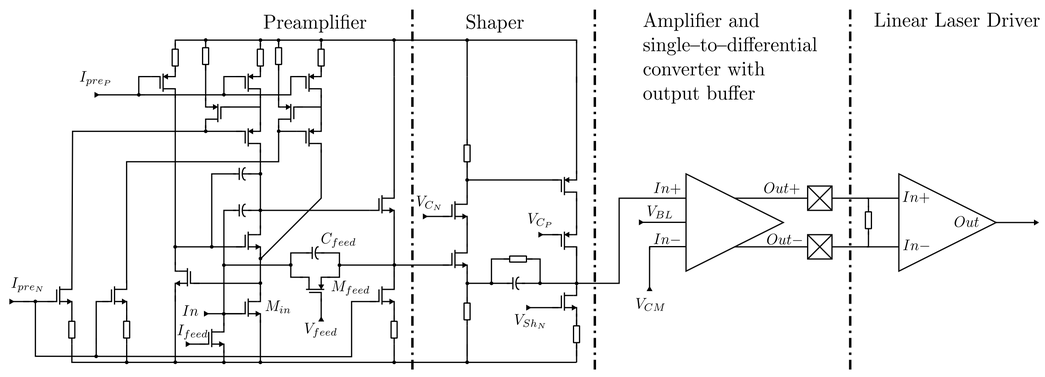
Design goals

- 2 – 5 pF detector capacitance range
- $\sim$ 10 fC linearity range
- $\sim$ 50 mV/fC of charge gain
- Equivallent Noise Charge $<$ 1000e$^-$
- Quasi–Gaussian shaping with T_P and FWHM $<$ 10 ns
- Fast baseline recovery after overdrive signal
- Hi–performance output buffer (100Ω & 10 pF load)

Architecture

- IBM CMOS8RF 130nm technology,
- number of safety diodes added to protect against transient overvoltage (to reach the amplifier bandwidth, circuit is built with thin oxide devices supplied with 2.5V instead of nominal 1.2V) – high voltage enabled design[1]

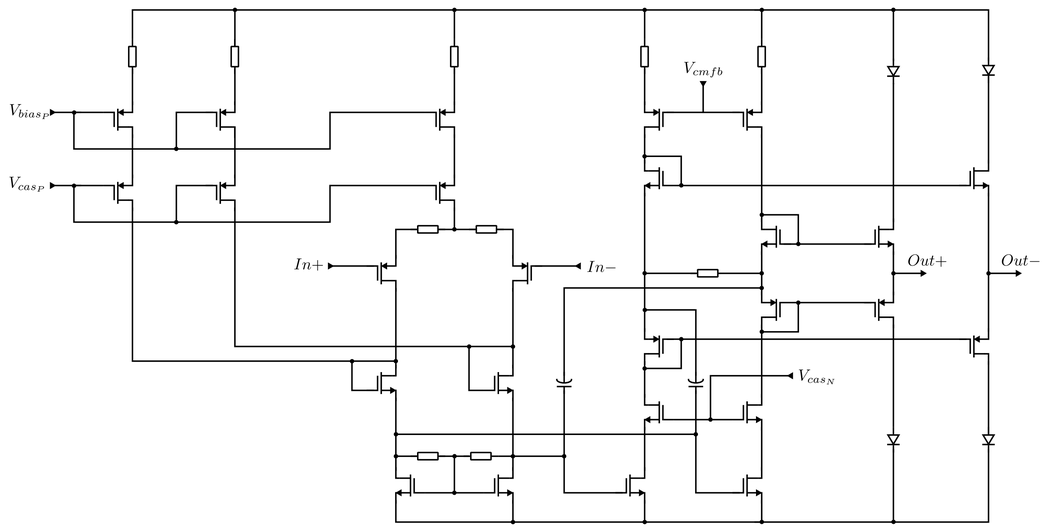


The front–end channel contains:

- Fast transimpendance preamplifier with active feedback[2]
- Cherry–Hooper shaper amplifier[2]
- Single–to–Differential converter with output buffer

Input transistor current $\sim$ 300μA, $g_m \sim$ 7.5 mS

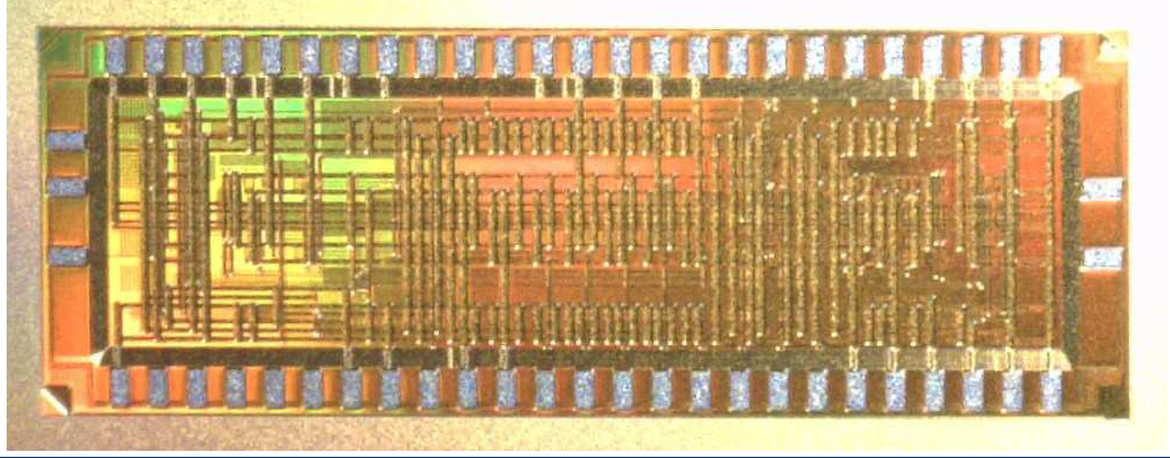
Output stage



- Class AB Push–Pull operation
- $\sim$ 9 mA output current capability (limited by safety diodes)
- $\sim$ 10 mW of power consumption

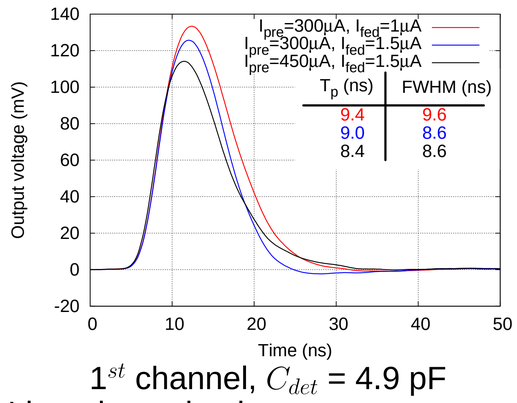
Fabricated prototypes

Die size: 5.6 $\times$ 2 mm^2, 4 channels per ASIC
Channel size: 860 $\times$ 80 μm^2
220 $\times$ 60 μm^2 (preamp + shaper) & 490 $\times$ 80 μm^2 (output stage)

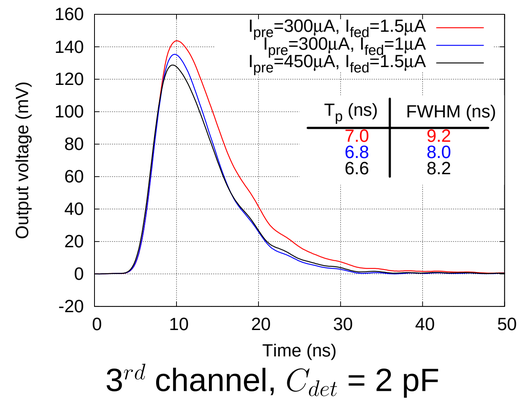


Performance measurements

1. Pulse Shapes for MIP response

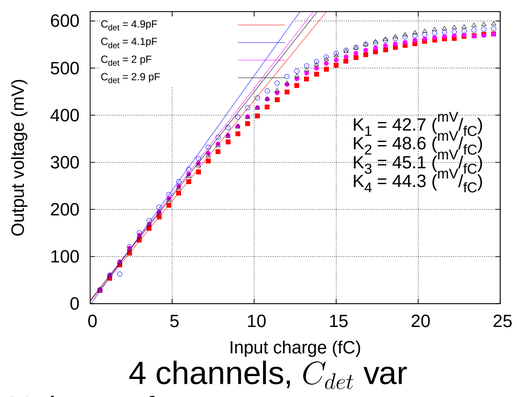


1^{st} channel, C_{det} = 4.9 pF

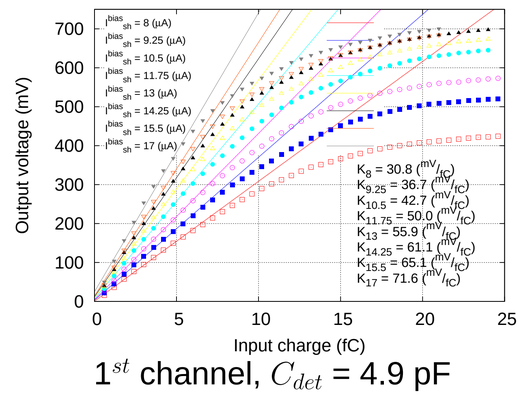


3^{rd} channel, C_{det} = 2 pF

2. Linearity and gain

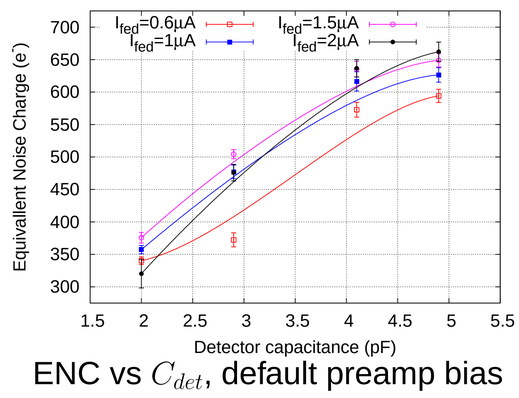


4 channels, C_{det} var

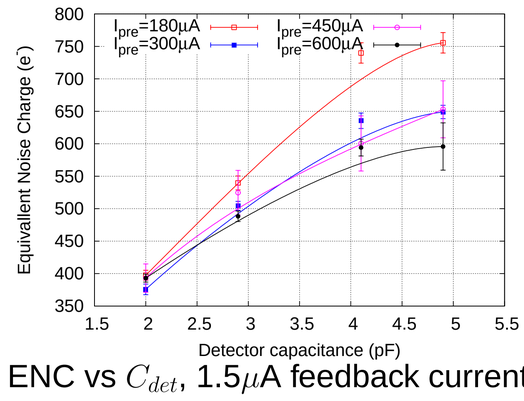


1^{st} channel, C_{det} = 4.9 pF

3. Noise performance

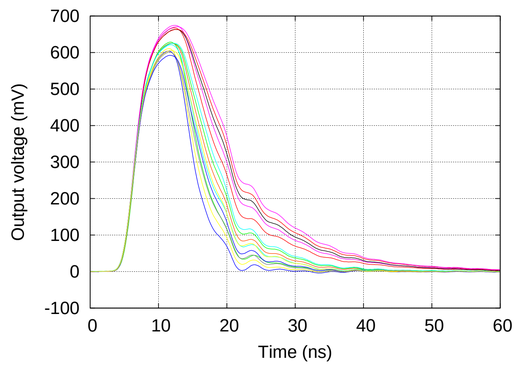


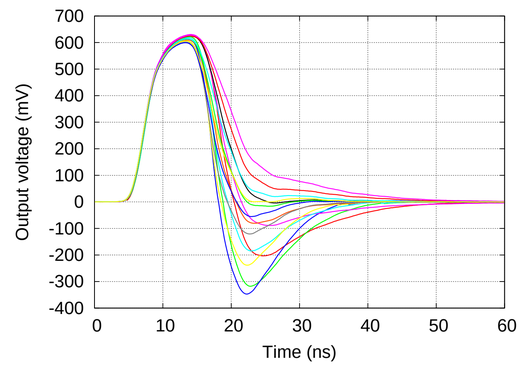
ENC vs C_{det}, default preamp bias (300μA), feedback current varied

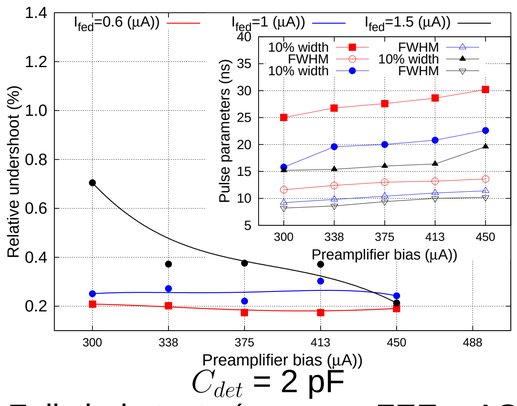


ENC vs C_{det}, 1.5μA feedback current, preamp current varied

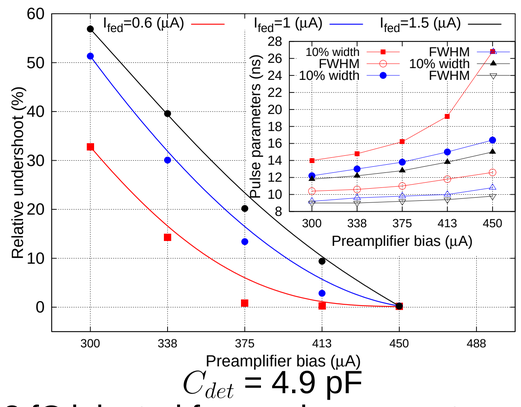
4. Large signal response for various FEE settings – Q_{in} 60 fC





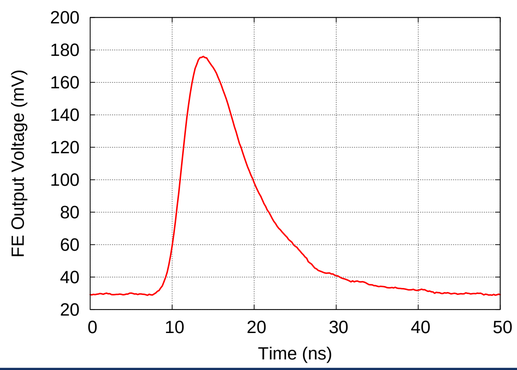


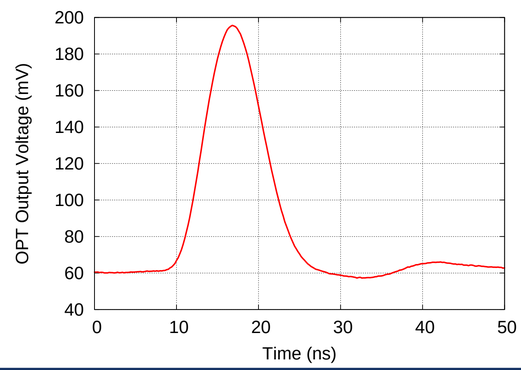
C_{det} = 2 pF



C_{det} = 4.9 pF

5. Full chain tests (sensor + FEE + AOH) – 3 fC injected from pulse generator





Summary

- Fabricated prototype is fully functional
- Power consumptions $\sim$ 11 mW
- Regulated charge gain – 50 mV/fC default
- Both T_p and FWHM are below 10 ns for various settings and C_{det}
- Equivallent Noise Charge below 800 e$^-$
- Return to baseline below 25ns without undershoot is possible

[1] Pui–In Mak, R. P. Martins: *High-/Mixed-Voltage RF and Analog CMOS Circuits Come of Age.* IEEE Cir. and Sys. Mag., vol. 10, no 4, pp. 27–39, 2010.

[2] J. Kaplon, M. Noy: *FEE for SLHC Semicon. Trackers in CMOS 90 nm and 130 nm Proc.* IEEE Tran. on Nuc. Sci., vol. 59, no 4, pp. 1611–1620, 2012.