Proton irradiation test of an SRAM FPGA for the possible usage in the readout electronics of the LHCb experiment.

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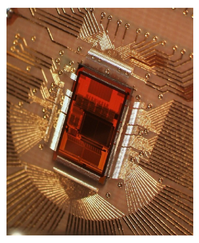
FPGA irradiation test board

The LHCb upgrade

- 2018 LHCb will upgrade its detector to a 40 MHz readout and a much more flexible software-based trigger system and increase the luminosity to 2×10^{33} $cm^{-2}s^{-1}$
- Current readout chips like the OTIS have a maximum readout rate of 1.1 MHz → Need upgrade!



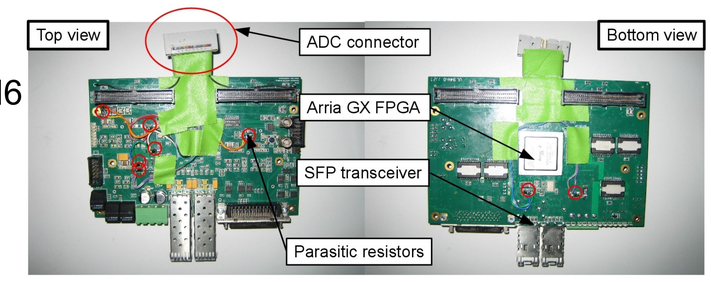
OTIS chip

Possible solution for regions with lower radiation levels

- Modern SRAM based FPGAs with high bandwidth transceivers provide a large number of logic elements to realize even multi-channel TDCs.
- Using FPGAs reduces costs of time and money.
- The radiation hardness of these devices increases with the down-scaling of the CMOS process.

Test board

- Arria GX EP1AGX35DF780I6
- FPGA used as TDC and Gbit/s transceiver
- 2 x 3.125 GBit transceivers



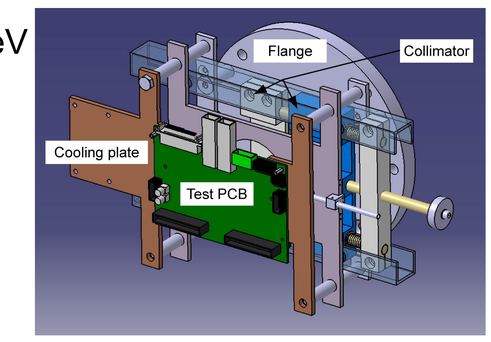
Total expected dose for LHCb OT readout

	Current situation	Upgrade situation
Total dose	3 krad	29 krad
1MeV neutron	4×10^{11}	4×10^{12}

Irradiation environment

Irradiation

- Two test boards were irradiated with 20 MeV protons up to 7 and 31 Mrad(Si)
- Proton flux : 2×10^{7} protons*Hz/cm^2 - 6×10^{9} protons*Hz/cm^2
- Dose per irradiation cycle between : 4.5 krad(Si) – 5 Mrad(Si)

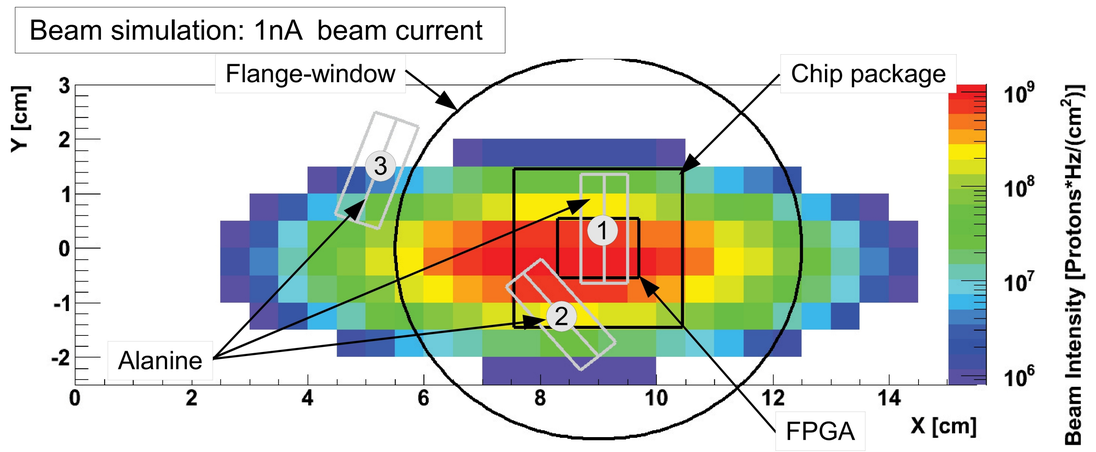


Dose determination

- Measured beam profile with straw-tube detector and collimator.
- Beam current monitored with Faraday cup.
- Simulation of dose
- Cross-check: passive dosimeters (alanine) show very good agreement

	Meas. Dose [Mrad] Probe 1/ Probe 2	Calc. Dose Alanine [Mrad] Probe 1/ Probe 2
Position 1*	~0 / 0.070	0.06 / 0.06
Position 2	0.15 / 0.25	0.12 / 0.32
Position 3	8.2 / 12.2(max)	7.9 / 14.0

*Position 1 was only place for one irradiation period

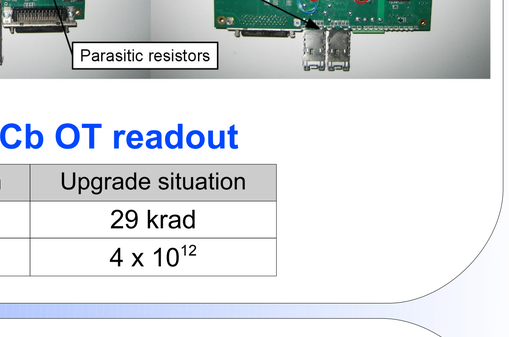


Proton flux over chip variates by +40% / -50%
but 70% of the chip area got at least the average flux.

Total ionization results

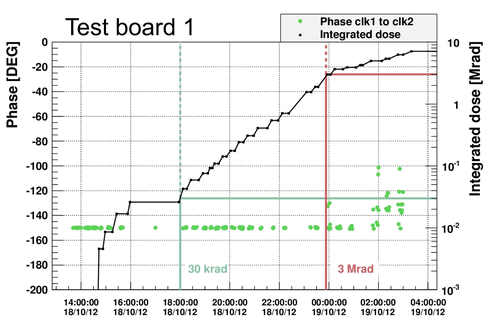
FPGA currents

- The electric currents of different voltages of the FPGA were monitored with resistors and ADCs.
  - The core current for the logic elements rises after 150 krad(Si) and reaches 107% for 7 Mrad(Si).
  - High irradiation intensities cause a drop followed by a linear rise. Power cycles of the FPGA bring the current back to the default value before the irradiation cycle.
  - The I/O current starts to drop after 400 krad(Si) and reaches 94% at 7Mrad(Si)
- All permanent current changes are between 5% - 20% and begin after 150 krad(Si).



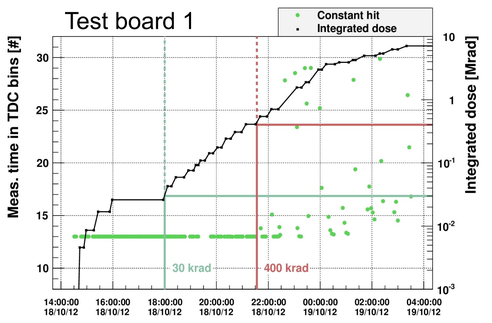
PLL stability

- 3 PLL clock signals monitored with a 1 GHz oscilloscope
  - The 3 frequencies (312.25MHz; 39MHz; 156.12MHz) are stable throughout the whole irradiation.
  - The phase between clk1 and clk2 shows a shift from -150° to larger values after 3 Mrad(Si).

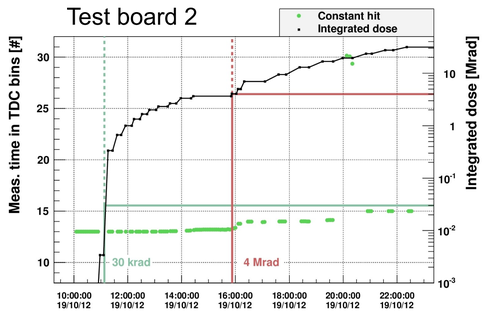


TDC stability

- 32 channel FPGA based TDC was tested.
  - TDC bin size: 790 ps
- The TDC design uses fast counters + fine timing with phase shifted clocks to determine the time.



- The stability of the time measurement for 4 channels was monitored.
  - Test board 1 shows a wrong time measurement after a total dose of 400 krad(Si).
  - Test board 2 shows a shifted time measurement after 4 Mrad(Si)

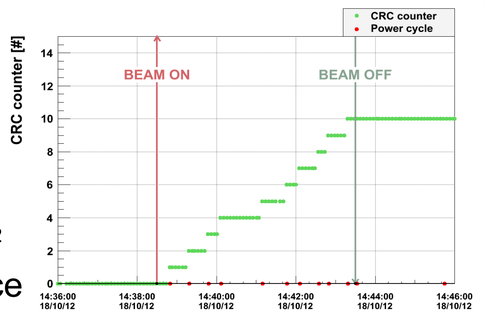


The FPGA sustained the expected TID of 30 krad for the upgrade of the LHCb OT readout without measurable degradation.

Soft-error results

FPGA configuration registers

- Used cyclic redundancy checker tool from Altera.
- For an irradiation intensity 54000 times the expected one, one error every 27.9 ± 3.2 seconds was found.
  - Proton flux : 2.3×10^{7} protons*Hz*cm^{-2}
  - Cross section: $1.6 \pm 0.2 \times 10^{-9}$cm^2 / device



Single event upset of user flip flops

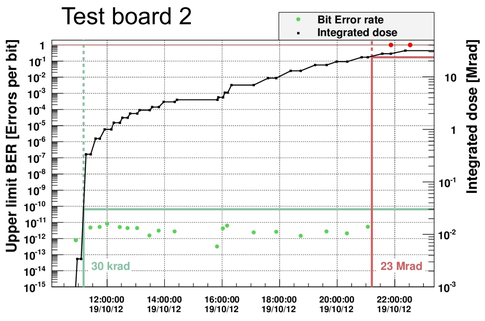
- 4608 flip flops, grouped into triples, were used to measure SEUs
- Error injector was used to test the functionality of the SEU block.
- No SEU was detected during the whole campaign.
  - Cross section: < 2×10^{-14}cm^{-2} / flip flop

GBit/s transceiver tests

- 1. Gbit link: Loop back → BERT
- 2. Gbit link: TDC data transmission to a second FPGA.

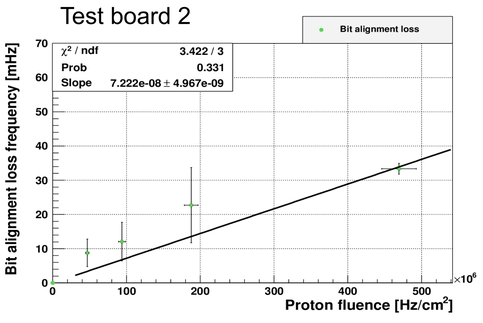
Between the irradiation periods

- No bit errors found
- BER upper limit: 10^{-11} – 10^{-12} errors per bit due to measurement time
- Both Gbit transceivers of second FPGA stopped working after 23 Mrad(Si)



During the irradiation periods

- Loss of bit alignment found, which the transceiver control block recovered automatically.
- Complete de-synchronization found, which needed a firmware reset.
  Cross section: $8 \pm 4 \times 10^{-11}$cm^2 / Gbit trans.



Scaling the results to the LHCb upgrade intensity

- FPGA configuration error expected every: 1.5×10^{6} s / FPGA
- Gbit transceiver resets needed every 3×10^{7} s / transceiver
- Further tests with higher energetic protons are foreseen (50MeV-200MeV)

The expected rate of FPGA firmware errors and resets for the Gbit transceivers seem to be manageable for the LHCb Outer Tracker upgrade.

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