Proton irradiation test of an SRAM FPGA for the possible usage in the readout electronics of the LHCb experiment.

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FPGA irradiation test board

The LHCb upgrade:
- 2018 LHCb will upgrade its detector to a 40 MHz readout and a much more flexible software-based trigger system and increase the luminosity to 2 x 10^{34} cm⁻²s⁻¹
- Current readout chips like the OTIS have a maximum readout rate of 1.1 MHz → Need upgrade!

Possible solution for regions with lower radiation levels:
- Modern SRAM based FPGAs with high bandwidth transceivers provide a large number of logic elements to realize even multi-channel TDCs.
- Using FPGAs reduces costs of time and money.
- The radiation hardness of these devices increases with the down-scaling of the CMOS process.

Test board:
- Arria GX EP1AGX35DF780I6
- FPGA used as TDC and Gbit/s transceiver
- 2 x 3.125 GBit transceivers

Total expected dose for LHCb OT readout

<table>
<thead>
<tr>
<th>Total dose (krad)</th>
<th>Current situation</th>
<th>Upgrade situation</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 krad</td>
<td>29 krad</td>
<td></td>
</tr>
<tr>
<td>1 MeV neutron</td>
<td>4 x 10^10</td>
<td>4 x 10^11</td>
</tr>
</tbody>
</table>

FPGA currents
- The electric currents of different voltages of the FPGA were monitored with resistors and ADCs.
  - The core current for the logic elements rises after 150 krad(Si) and reaches 107% for 7 Mrad(Si).
  - High irradiation intensities cause a drop followed by a linear rise. Power cycles of the FPGA bring the current back to the default value before the irradiation cycle.
  - The I/O current starts to drop after 400 krad(Si) and reaches 94% at 7 Mrad(Si).
- All permanent current changes are between 5% - 20% and begin after 150 krad(Si).

PLL stability
- 3 PLL clock signals monitored with a 1 GHz oscilloscope
  - The 3 frequencies (312.25MHz; 39MHz; 156.12MHz) are stable throughout the whole irradiation.
  - The phase between clk1 and clk2 shows a shift from -150° to larger values after 3 Mrad(Si).

TDC stability
- 32 channel FPGA based TDC was tested.
  - TDC bin size: 790 ps
  - The design uses fast counters + fine timing with phase shifted clocks to determine the time.
  - The stability of the time measurement for 4 channels was monitored.
    - Test board 1 shows a wrong time measurement after a total dose of 400 krad(Si).
    - Test board 2 shows a shifted time measurement after 4 Mrad(Si)

The FPGA sustained the expected TID of 30 krad for the upgrade of the LHCb OT readout without measurable degradation.

Irradiation environment

Irradiation:
- Two test boards were irradiated with 20 MeV protons up to 7 and 31 Mrad(Si)
- Proton flux: 2 x 10^{10} protons*Hz/cm² - 6 x 10^{10} protons*Hz/cm²
- Dose per irradiation cycle between: 4.5 krad(Si) – 5 Mrad(Si)

Dose determination:
- Measured beam profile with straw-tube detector and collimator.
- Beam current monitored with Faraday cup.
- Simulation of dose Cross-check: passive dosimeters (alanine) show very good agreement

<table>
<thead>
<tr>
<th>Beam: Mrad Probe 1/ Probe 2</th>
<th>Calc. Dose: Alamine Probe 1/ Probe 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Position 1</td>
<td>0.1 / 0.570</td>
</tr>
<tr>
<td>Position 2</td>
<td>0.06 / 0.505</td>
</tr>
<tr>
<td>Position 3</td>
<td>0.12 / 0.322</td>
</tr>
</tbody>
</table>

Soft-error results

FPGA configuration registers
- Used cyclic redundancy checker tool from Altera.
- For an irradiation intensity 54000 times the expected one, one error every 27.9 ± 3.2 seconds was found.
  - Proton flux: 2.3 x 10^{10} protons*Hz/cm²
  - Cross section: 1.6 ± 0.2 x 10^{14} cm² / device

Single event upset of user flip flops
- 4608 flip flops, grouped into triples, were used to measure SEUs
- Error injector was used to test the functionality of the SEU block.
- No SEU was detected during the whole campaign.
  - Cross section: < 2 x 10^{16} cm² / flip flop

Gbit/s transceiver tests
1. Gbit link: Loop back → BERT
2. Gbit link: TDC data transmission to a second FPGA.

Between the irradiation periods
- No bit errors found
  - BER upper limit: 10^{−14} < 10^{−12} errors per bit due to measurement time
- Both Gbit transceivers of second FPGA stopped working after 23 Mrad(Si)

During the irradiation periods
- Loss of bit alignment found, which the transceiver control block recovered automatically.
  - Complete de-synchronization found, which needed a firmware reset.
  - Cross section: 8 ± 4 x 10^{15} cm² / Gbit trans.

Scaling the results to the LHCb upgrade intensity
- FPGA configuration error expected every: 1.5 x 10^{14} / FPGA
- Gbit transceiver resets needed every 3 x 10^{19} / transceiver
- Further tests with higher energetic protons are foreseen (50MeV-200MeV)

The expected rate of FPGA firmware errors and resets for the Gbit transceivers seem to be manageable for the LHCb Outer Tracker upgrade.

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