ATLAS Phase II Strip Tracker: Electronic Developments

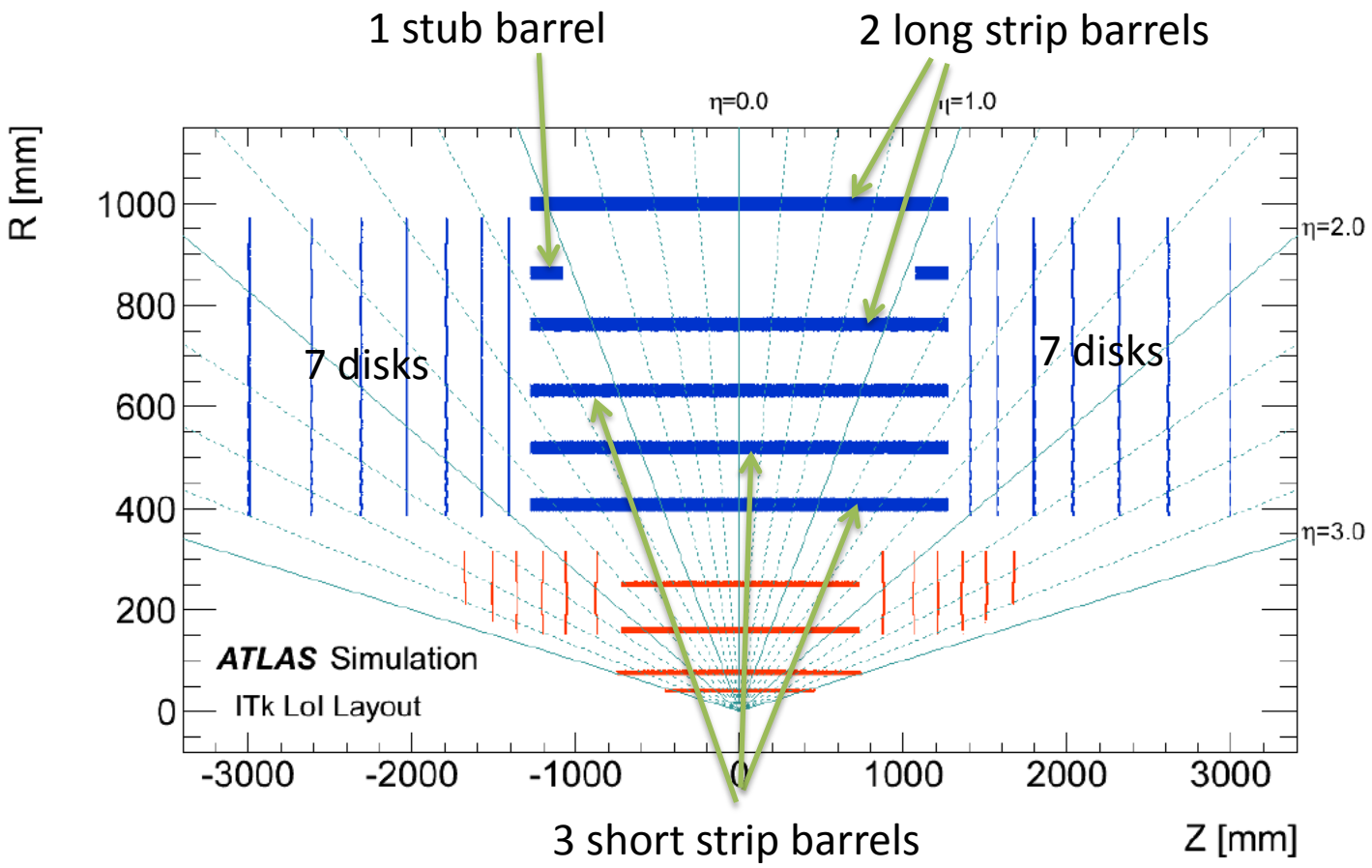
ACES, CERN, 19/03/2014

Peter W Phillips
On behalf of
The ATLAS ITK Strip Community

Outline

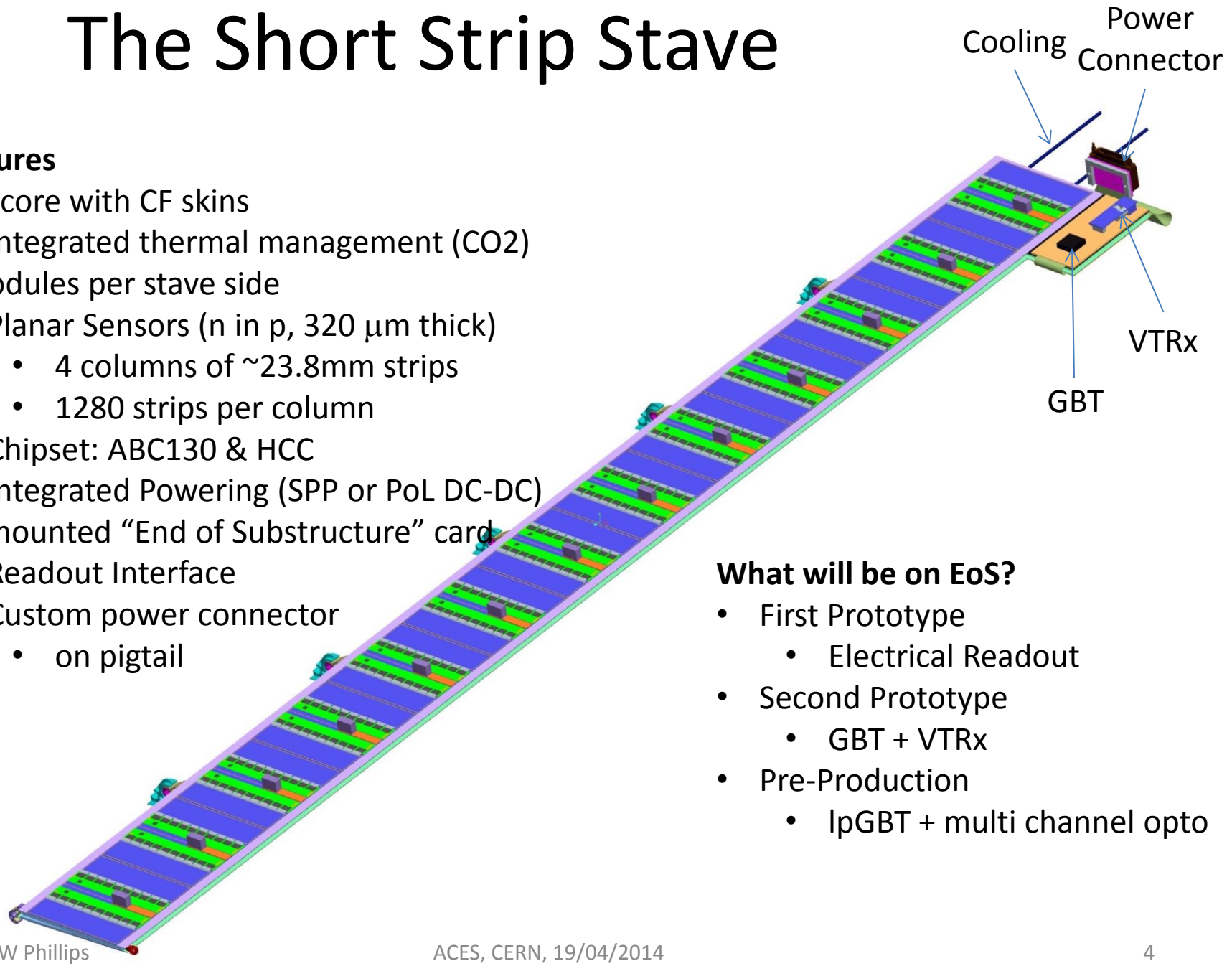
- **Conceptual Layout**
  - **Barrels and Disks, Staves and Petals**
- **Architecture**
  - **ASICs**
    - **HCC**
    - **ABC130**
  - **Trigger Scheme**
  - **First ABC130 Results !!!**
  - **ABC130 Module with Integrated Powering**
  - **HV Multiplexing and Bias Current Measurement**
- **Status of Petal and Stave Prototypes**
  - **With 250nm chipset**

Provisional ITk Layout



Strip system: 193 m^2 sensor area, 74M channels

The Short Strip Stave



Key Features

- Stave core with CF skins
  - Integrated thermal management (CO2)
- 13 modules per stave side
  - Planar Sensors (n in p, 320 μm thick)
    - 4 columns of ~23.8mm strips
    - 1280 strips per column
  - Chipset: ABC130 & HCC
  - Integrated Powering (SPP or PoL DC-DC)
- Side mounted “End of Substructure” card
  - Readout Interface
  - Custom power connector
    - on pigtail

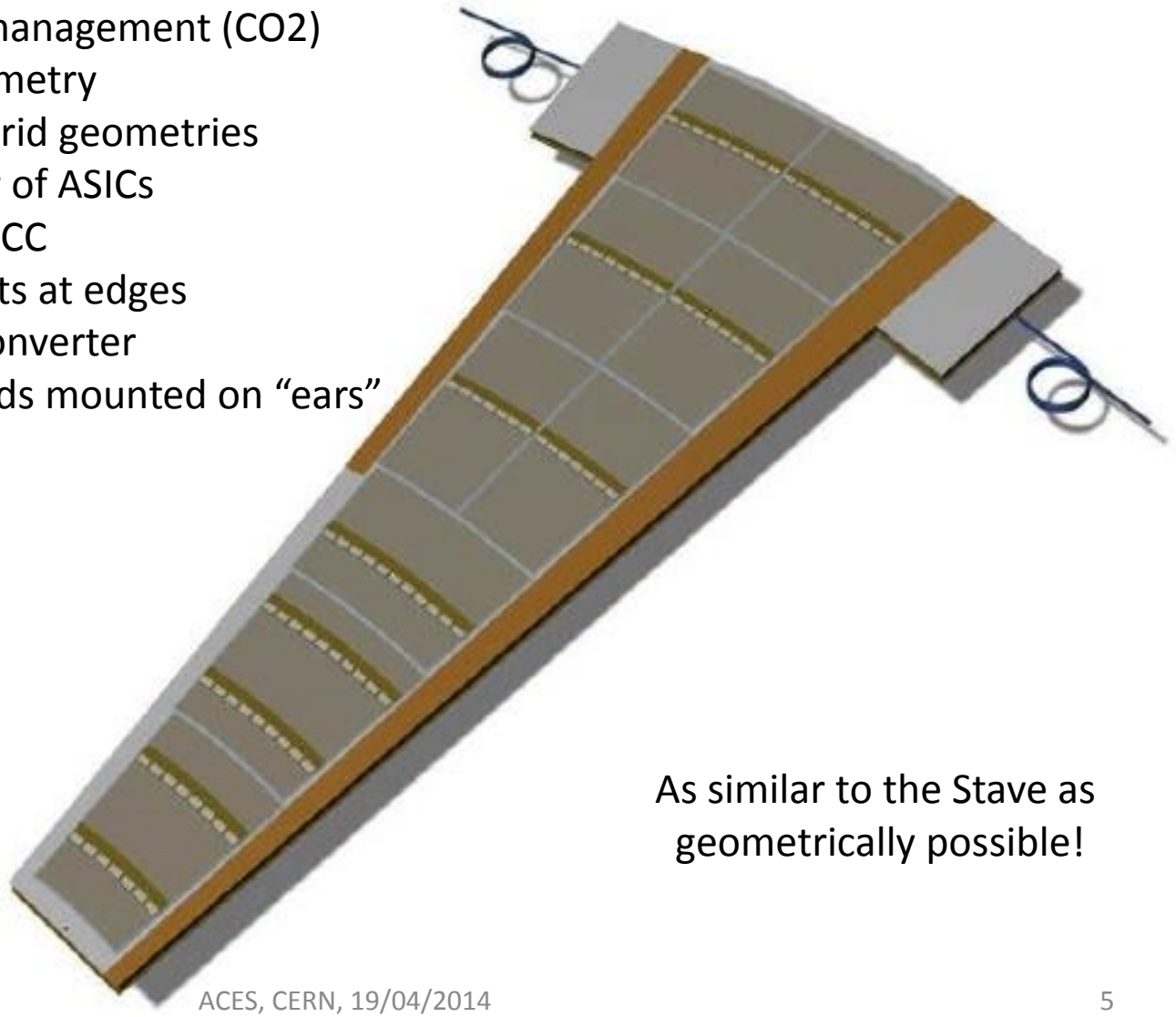
What will be on EoS?

- First Prototype
  - Electrical Readout
- Second Prototype
  - GBT + VTRx
- Pre-Production
  - lpGBT + multi channel opto

The Petal

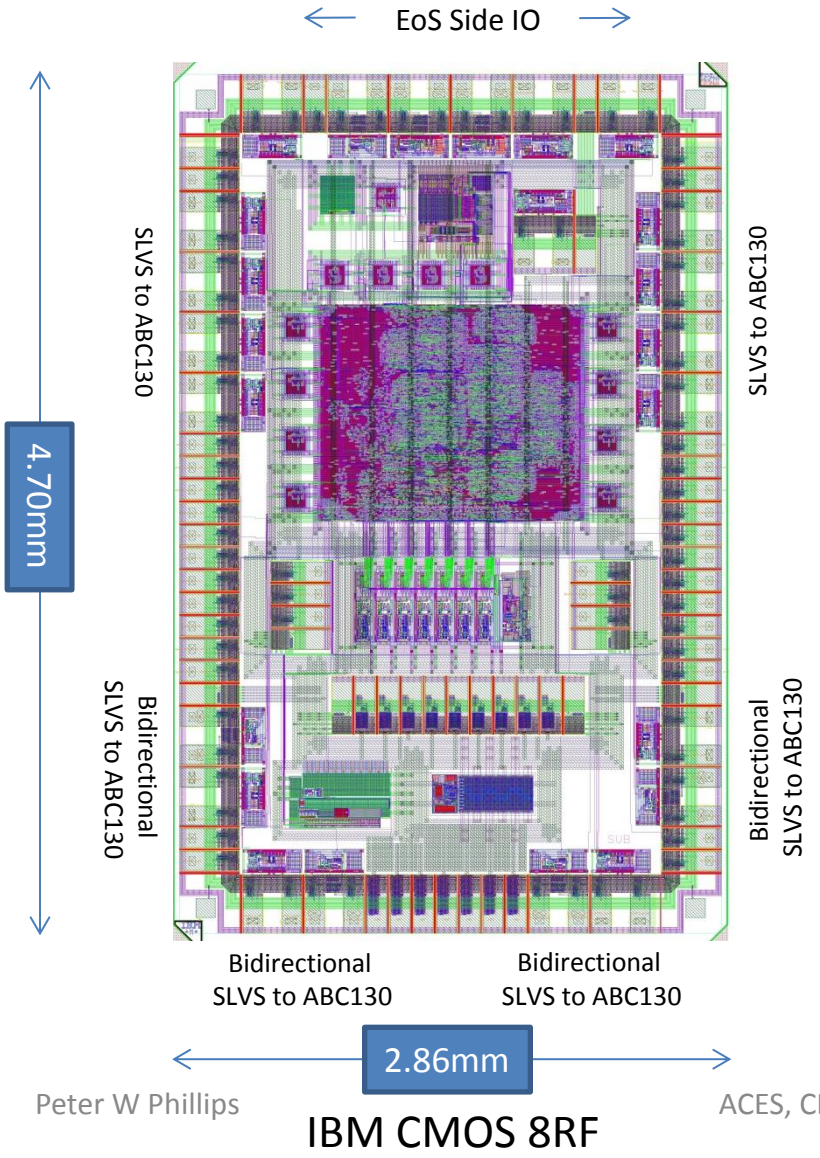
Key Features

- Petal core with CF skins
  - Integrated thermal management (CO2)
- Modules with wedge geometry
  - Several sensor & hybrid geometries
    - Varying number of ASICs
  - Chipset: ABC130 & HCC
  - Powering components at edges
    - SPP or DC-DC converter
- “End of Substructure” cards mounted on “ears”
  - Readout Interface



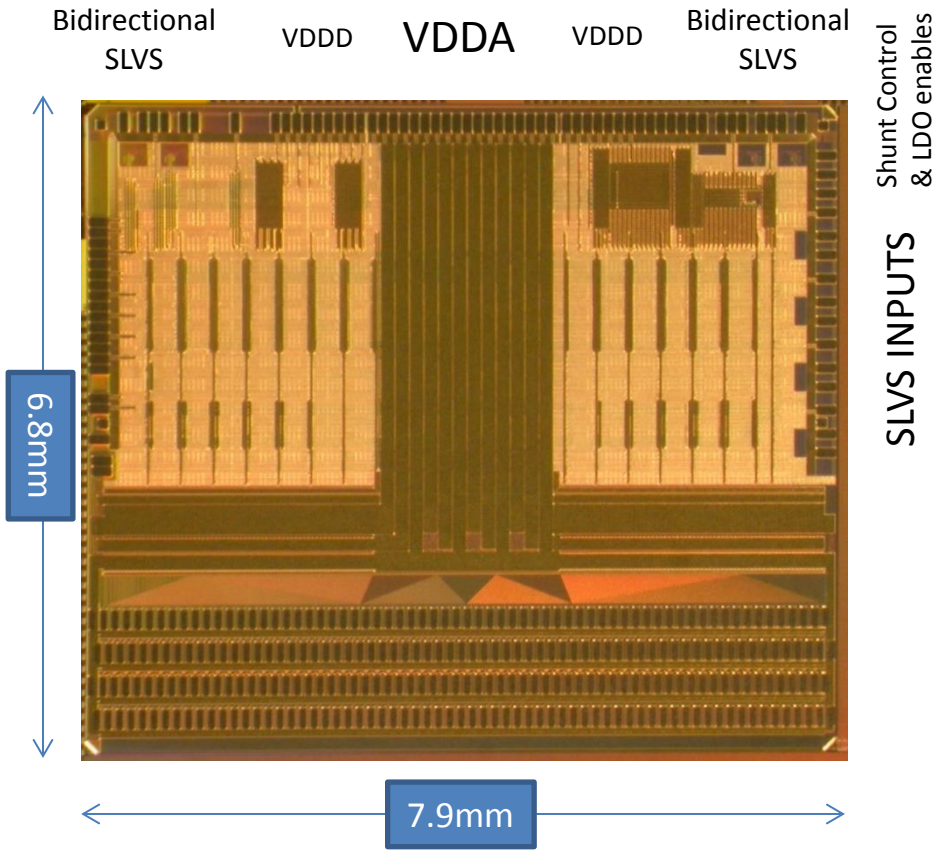
As similar to the Stave as geometrically possible!

Hybrid Controller Chip (HCC)



- Pad Frame optimized for hybrid mass reduction
  - Smaller footprint => Smaller hybrid
  - Hybrid side SLVS buses copied to both sides to suit left and right “handed” hybrids
- Key Features:
  - SLVS IO
    - Data back to EoS at up to 320Mbits
    - with optional 8b10b
  - PLL to generate 40, 80, 160, 320, 640MHz synchronous to BCO
    - Modified GBT ePLL
  - Delays
  - DCS Monitoring & General Purpose IO
    - Temperature, Voltage, …
    - Output ABC130 compatible fixed length packets
- Status
  - P&R and verification well advanced
  - Probable submission in May

ABC130 Front End Chip

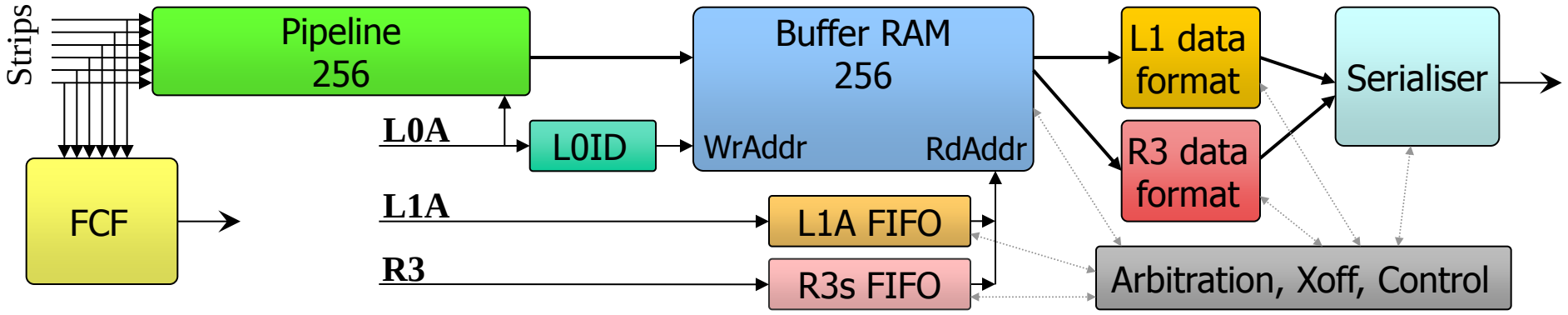


IBM CMOS 8RF

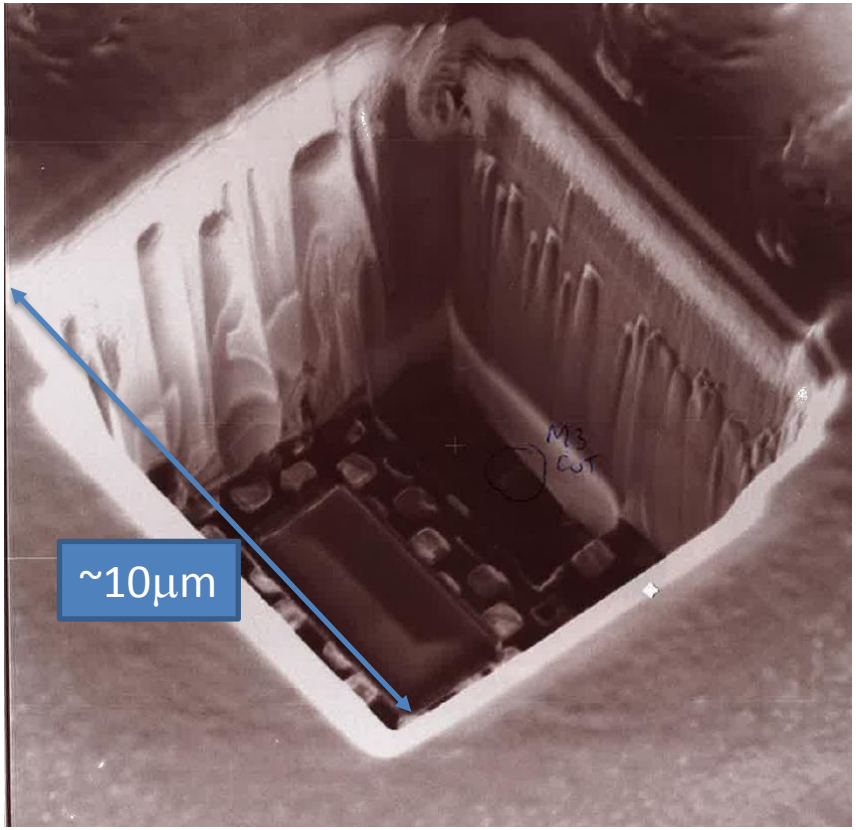
- Pad Frame optimized for hybrid mass reduction
  - 256 channels -> reduce part count
  - FE geometry suits direct sensor bonding
  - All power bonds at back edge
- New 2 level trigger architecture
  - Level-0 - synchronous 500kHz-1MHz
    - Moves event data from a pipeline to buffer in FEs, no readout
    - Event data tagged with L0ID
  - Level-1 - asynchronous ~200kHz
    - Data retrieved from buffer using L0ID tag
- Other key features
  - Fixed length data packets
  - Programmable LDOs for Analogue / Digital power
  - Shunt to support Serial Powering
- Two variants made
  - One includes additional “Fast Cluster Finder” block for self-seeded trigger
- First wafers back Q4 2013
  - Testing in progress

ABC130 Trigger Architecture

- Additional track-trigger function
  - Regional Readout (R3)
    - A special trigger sent only to modules inside a Region of Interest
    - L0-trigger identified regions of interest
- L0A copies data from pipeline to RAM
  - L0ID counter used as address
- L1A and R3 requests have independent FIFOs
  - Stores L0IDs - locates event in buffer
  - Arbiter ensures ordered data handling - R3 has priority
  - Effective as a de-randomiser
- Data is formatted by dedicated blocks and serialised to HCC



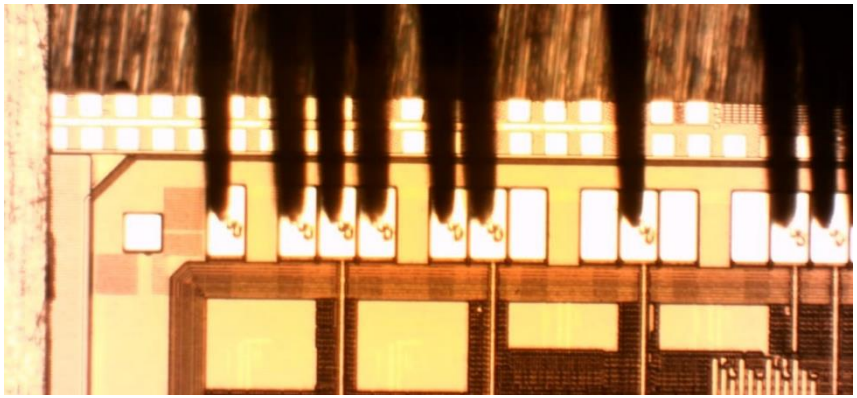
ABC130 Early Test Issue



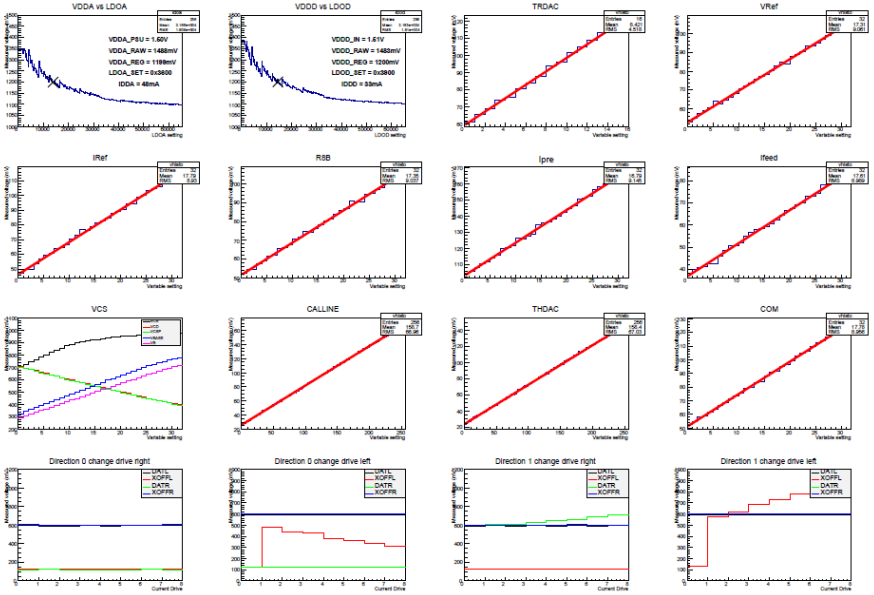
FIB edit by NanoScope Ltd., Bristol

- No data output
- Problem traced to custom transceiver block
  - Discrepancy between reality and functional model for polarity of “direction” signal
- Corrected for a small number of die by FIB edit
  - Cut direction line
  - Strap to VDD or 0V as required
- Resubmission being prepared
  - New M3 layer only
  - Others unchanged

ABC130 Preliminary Results (1)



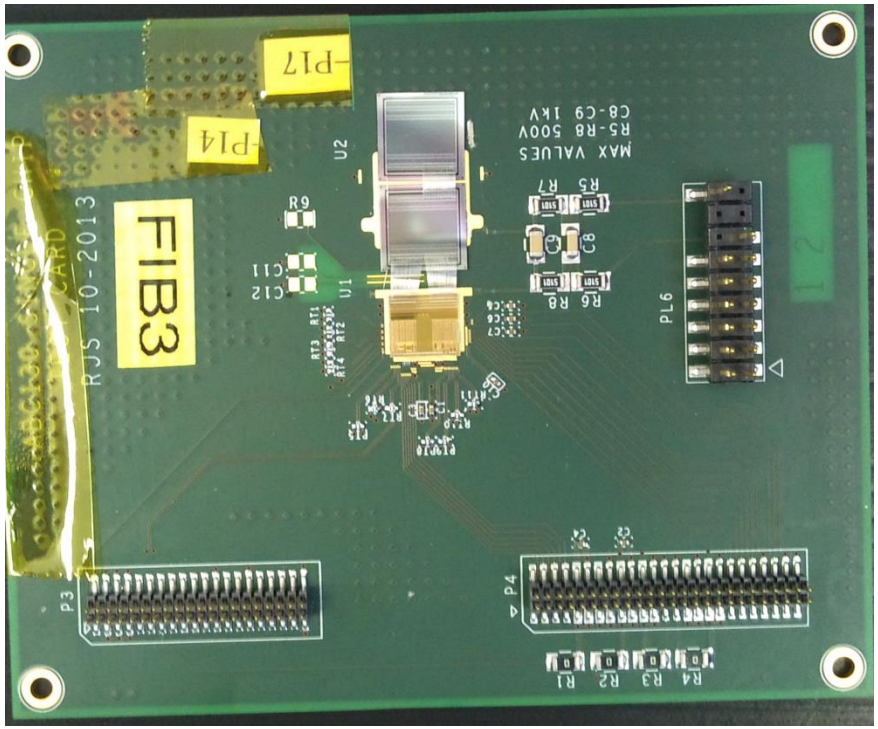
ABC130 under Probe Test



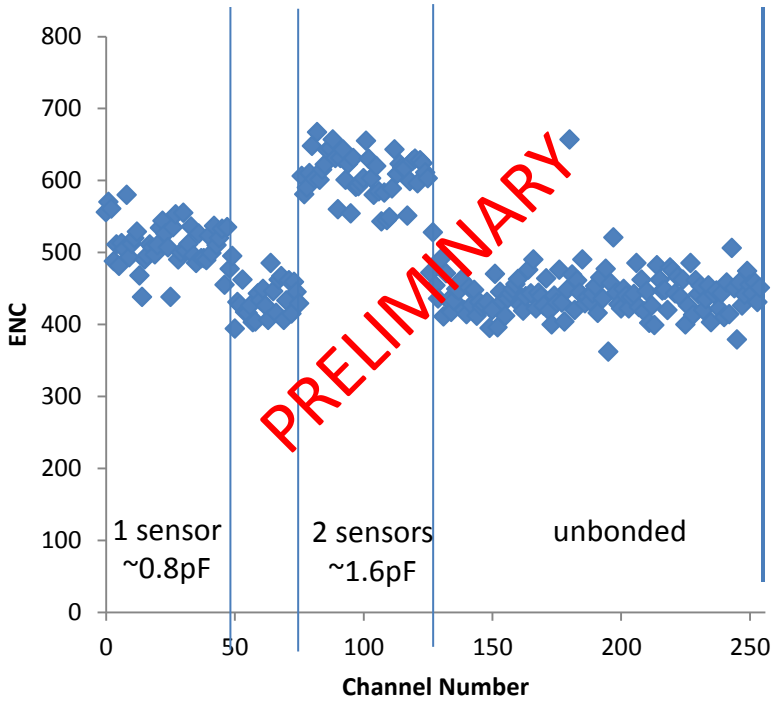
ABC130 DAC & LDO Characteristics

- Evaluation of single FIB die continues
  - Test PCB
  - Probe Card
- Test coverage to date:
  - Register write/read
  - DACs & LDOs
  - 40, 80, 160 MHz DCLK
  - Noise with mini sensors
  - Mean Power vs trigger rate
- Pending
  - Clock margin (higher BCO)
  - Power vs time
  - Gain calibration
    - beam, laser, source…
  - SEU studies
  - Irradiation
  - …

ABC130 Preliminary Results (2)



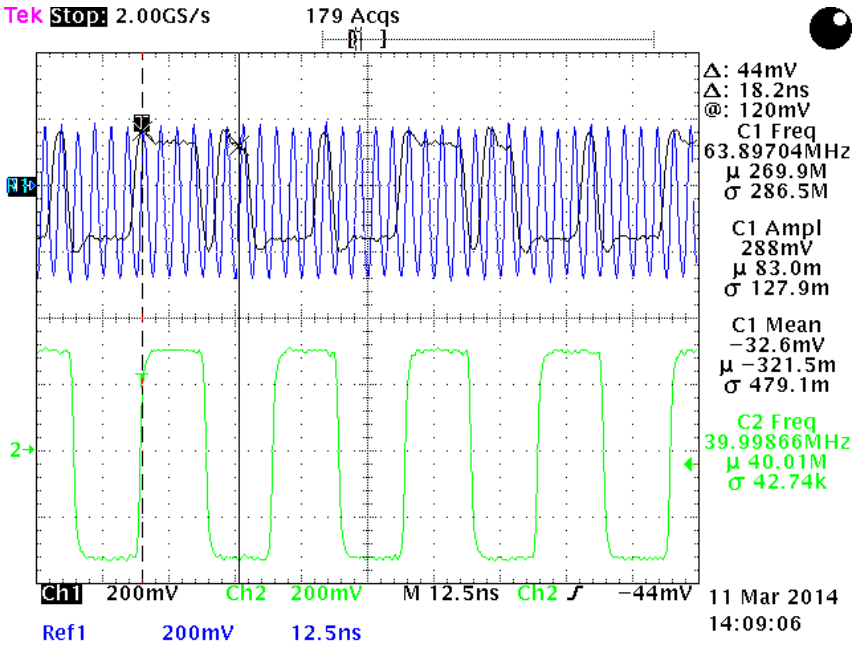
ABC130 with two ATLAS07 mini sensors



Preliminary noise data at 150V bias

Noise is as expected. To date - apart from the known "feature" - ABC130 is working well.

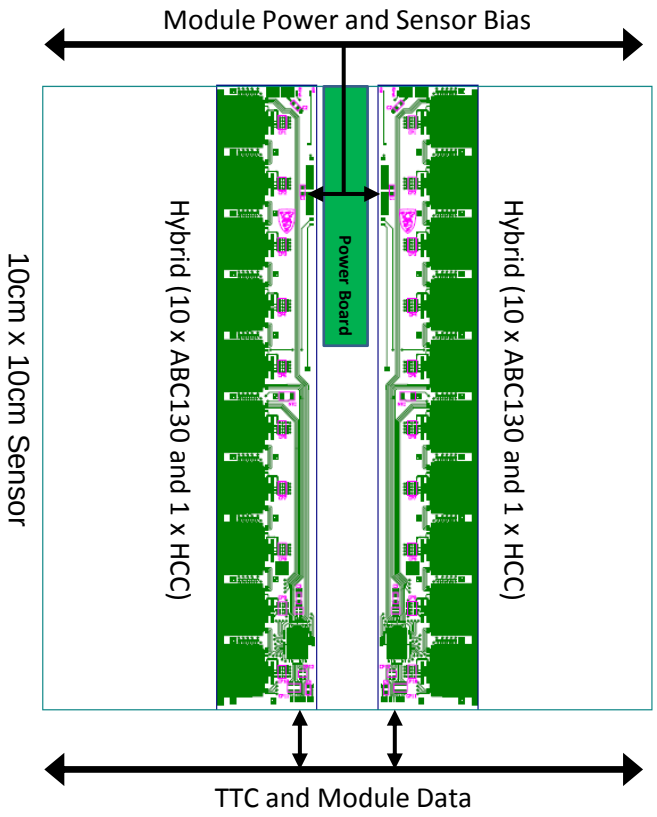
Testing The Fast Cluster Finder



FCF Output (black) at 320 MHz (blue)

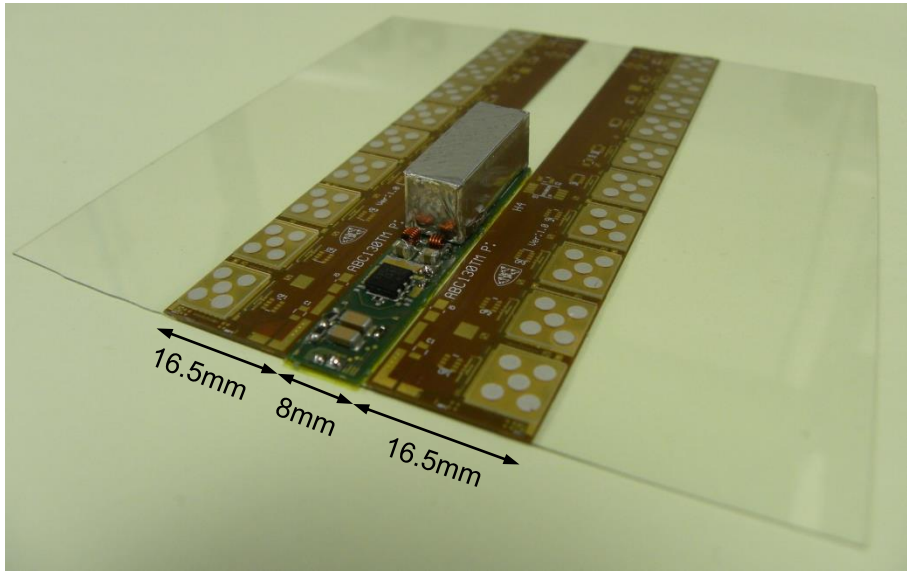
- Fast-Cluster-Finder is a proof-of-principle block for self-seeded triggering
  - Autonomous – no interaction with other chip functions
  - Outputs cluster lists at up to 640Mbits for correlation with hits from other side of stave/petal
- Parallel effort to verify function of this block on uncorrected die
  - Plot shows FCF output at 320 MHz
  - Half speed for now, but basically working
- This effort will continue
  - Work is directed toward a self-seeded trigger demonstrator module

ABC130 Barrel Module



- Module is made up of 3 main parts:
  - Sensor
  - Flex circuits (carrier for readout asics and I/O buffer)
  - Power Board (SPP or PoL DC-DC) with sensor filtering
- Moving towards an integrated module
  - Flex circuits and powering attached within sensor area
  - Sensor provides mechanical support and thermal management

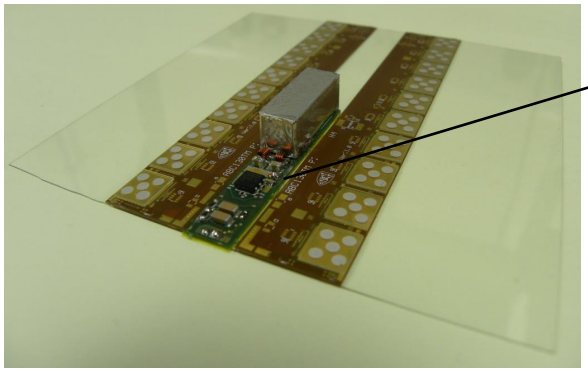
Assembly of "half module" with 5 FIB corrected ABC130 and 5 uncorrected ABC130 pending

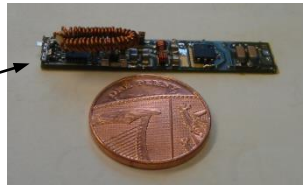


Thermo-Mechanical Module with Prototype DCDC converter

Prototype DC-DC Converters

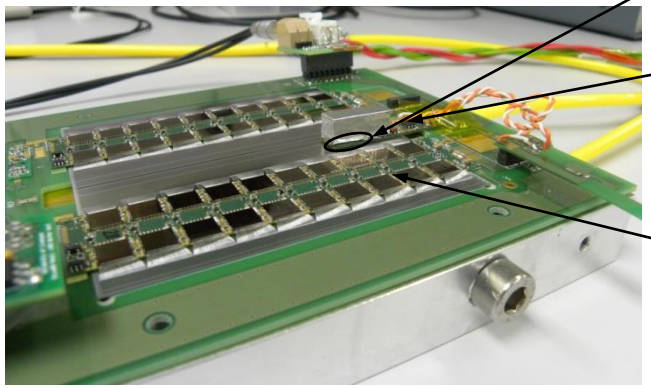
ABC130 Prototype Converter



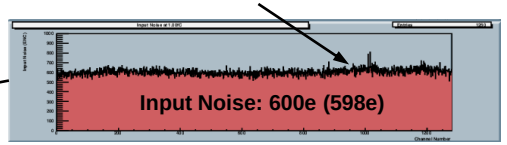


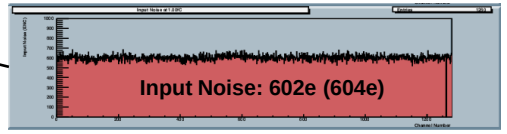
- Converter Dimensions (L x W x H): 44 x 8 x 6.5 mm
  - 4 Layer build using 1oz Cu
  - Hand wound elliptical inductor (200nH/26mΩ)
  - Converter circuit based on CERN STV10
    - With reduced sized SMDs (0805 instead of 1210)
    - Plus 1-wire control and HV filtering

Test on ABCN-25 module



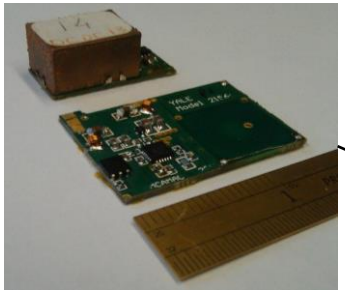
Leakage from shield box (~15e increase)





Reference measurement shown in brackets (CERN SM01C converter)

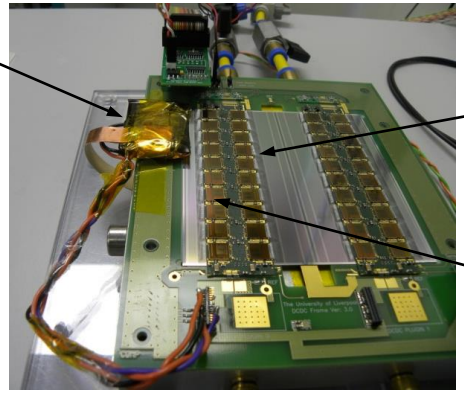
Planar Coil Prototype Converter



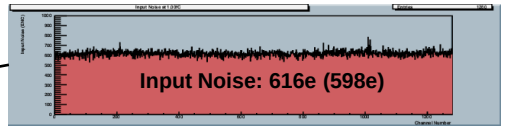
- Involves embedding coil within PCB
  - Significant reduction in height compared to toroidal coil
    - **Target height <4mm with shield**
  - Making integration and cooling of coil easier

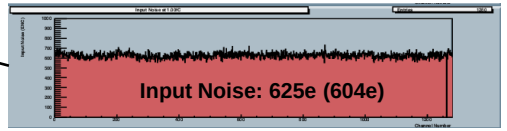
- Based on commercial LTC3605 buck regulator
  - As per CERN type
  - Wrap-around shield added to encompass noisy circuitry
  - Efficiency comes in at 77% at 3A

Test on ABCN-25 module



Converter placed <3mm from bond wires

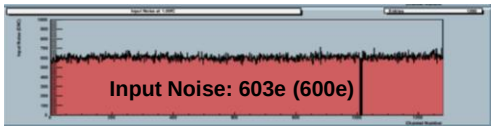


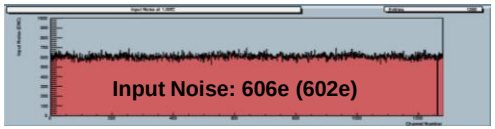


Converter at 4MHz

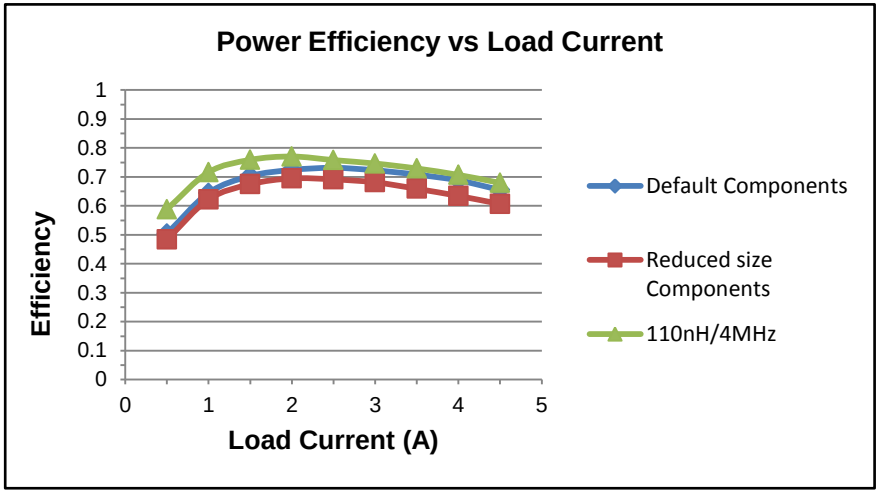
- Switching frequency of Buck regulator increased from 2MHz to 4MHz
  - Should allow smaller sized components to be used, making integration/packaging easier
  - Inductor now ~110nH (was originally ~220nH) and DC resistance now ~14mΩ (was ~26mΩ)

- Tests done with converter on sensor, largest sized component is 0805
  - Input noise is more or less identical to previous measurements using ~200nH coil at 2MHz
  - Efficiency is coming in at ~77% at 2A (predicted ABC130 module current consumption)
    - Was originally 70-72% operating at 2MHz

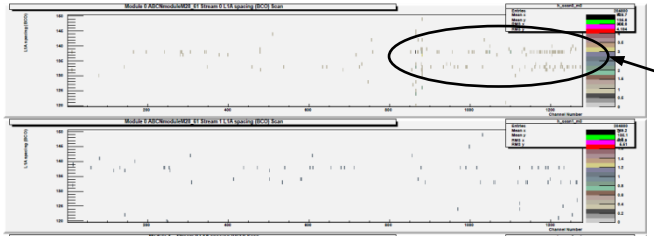




Value in brackets is original noise measurement at 2MHz using 0805 components



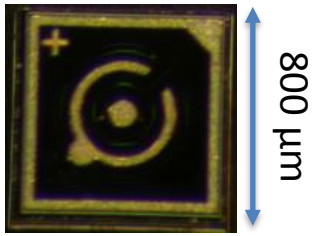
DTN at 0.4fC



Only see evidence of converter at 0.4fC, all other threshold settings show approx zero occupancy

Sensor Bias (HV) Multiplexing

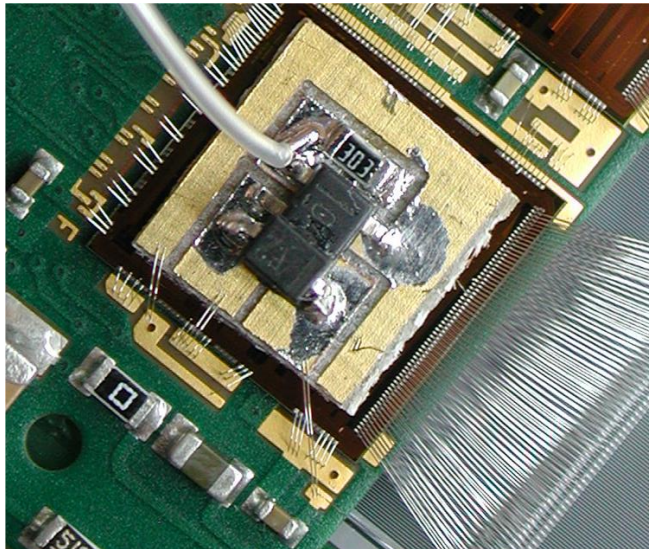
- Propose use of rad-hard HV switches
  - To be able to disconnect any failed sensors from common bias line
- Present phase: Device Identification
  - Study of commercial HV transistors: GaN, Silicon, Silicon Carbide
  - before and after irradiation
  - Devices with BV < 500V would need to be “stacked”

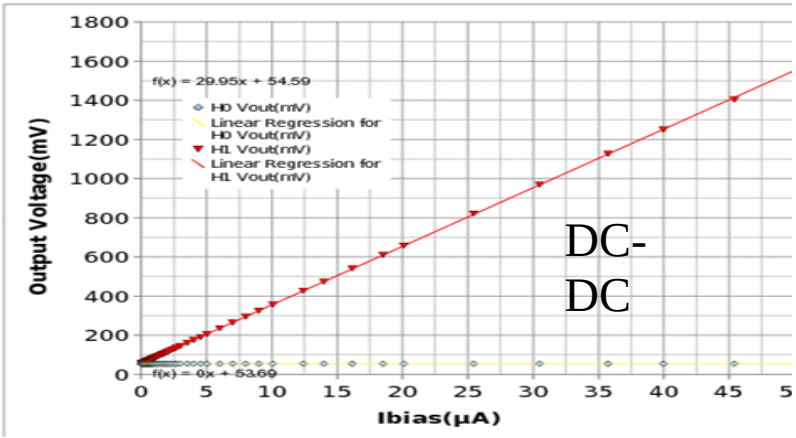


Crystalonic 2N6449

Transistor	Type	Other data	Status	
Crystalonic 2N6449	Si JFET	BV = 300V, Idmax = 5 mA , Idss = 1 nA, die 0.8 x 0.8 mm²	TESTED	
Interfet 2N6449	Si JFET	Similar to Crystalonic	IRRADIATED	
IXYS CPC5603	Si MOSFET	BV = 410V, Idmax = 0.3 A, Idss = 0.02µA, packaged	IRRADIATED	
ROHM R6006ANX	Si MOSFET	BV = 600V, Idmax = 6A, Idss <1nA@500V, packaged	TESTED	
Infineon IPA50R950CE	Si MOSFET	BV = 500V, Idmax = 4 A, Idss <1nA, packaged	TESTED	
Semisouth SJEP170	**SiC JFET**	**BV = 1700V, Idmax = 8 A, Idss = 10 µA**	**TESTED**	**GOOD but unavailable**
USCi UJN1205	SiC JFET	BV = 1200V, Idmax = 23 A, Idss = 250 µA, die 3.1 x 3.1 mm²	TESTED	
CREE CPMF-1200	**SiC MOSFET**	**BV = 1200V, Idmax = 28 A, Idss = 50 µA, die 3.1 x 3.1 mm²**	**IRRADIATED**	**PROMISING**
ROHM S2403	SiC MOSFET	BV = 1700V, die 4 x 3mm²	IRRADIATED	
ROHM SCT2080K	SiC MOSFET	BV = 1200V, die 2 x 2 mm²	IRRADIATED	
GeneSiC GA04JT17	SiC BJT	BV = 1700V, Idmax = 4 A, Idss = 0.5 µA, die 1.45 x1.45 mm²	TESTED	
TranSiC FSICBH057A120	SiC BJT	BV = 1200V, Idmax = 20 A, Idss = 100 µA, die 2.5 x 2.5 mm²	TESTED	
Transphorm TPH2006C	GaN JFET	BV = 600V, die and packaged		
EPC2012	**GaN JFET**	**BV = 200V, die and packaged**	**TESTED**	**GOOD**

On-Hybrid Sensor Current Measurement



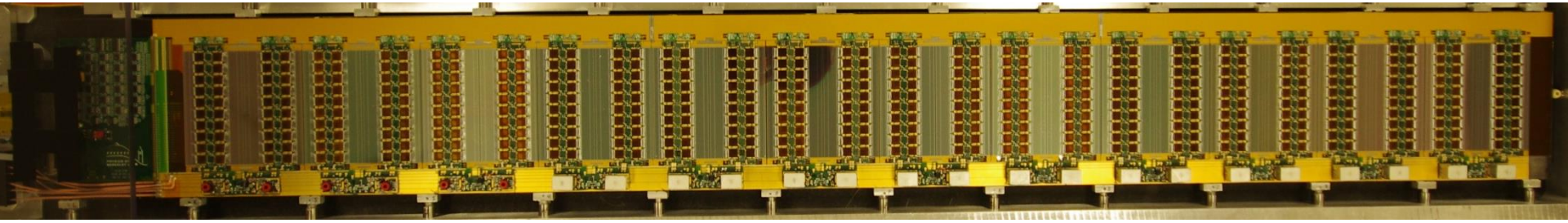


- Signal Return on Hybrid
  - Strip Bias AC coupled at every corner
- DC return
  - One corner has diode/op-amp combination
    - Normal DC path through op-amp (later HCC or other ASIC)
    - Backup DC path through diode (accommodates amplifier offset)
- Proof of Principle test using commercial parts
  - OPA365, 1N4148
- **No additional noise for test module using DC-DC converter**

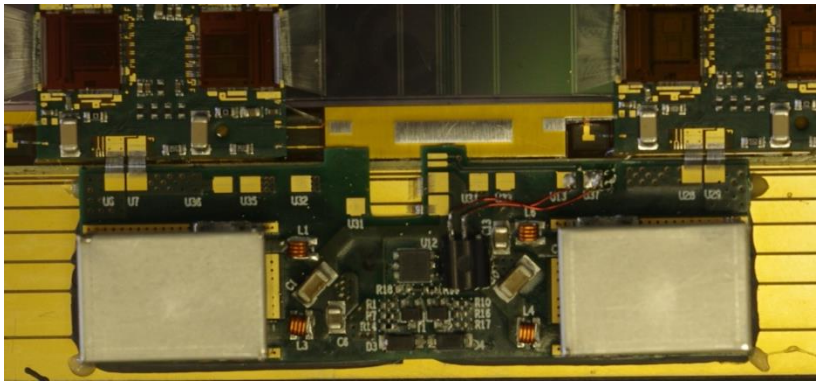
Status of Petal & Stave Prototypes

With 250nm Chipset

Stave 250 DC-DC

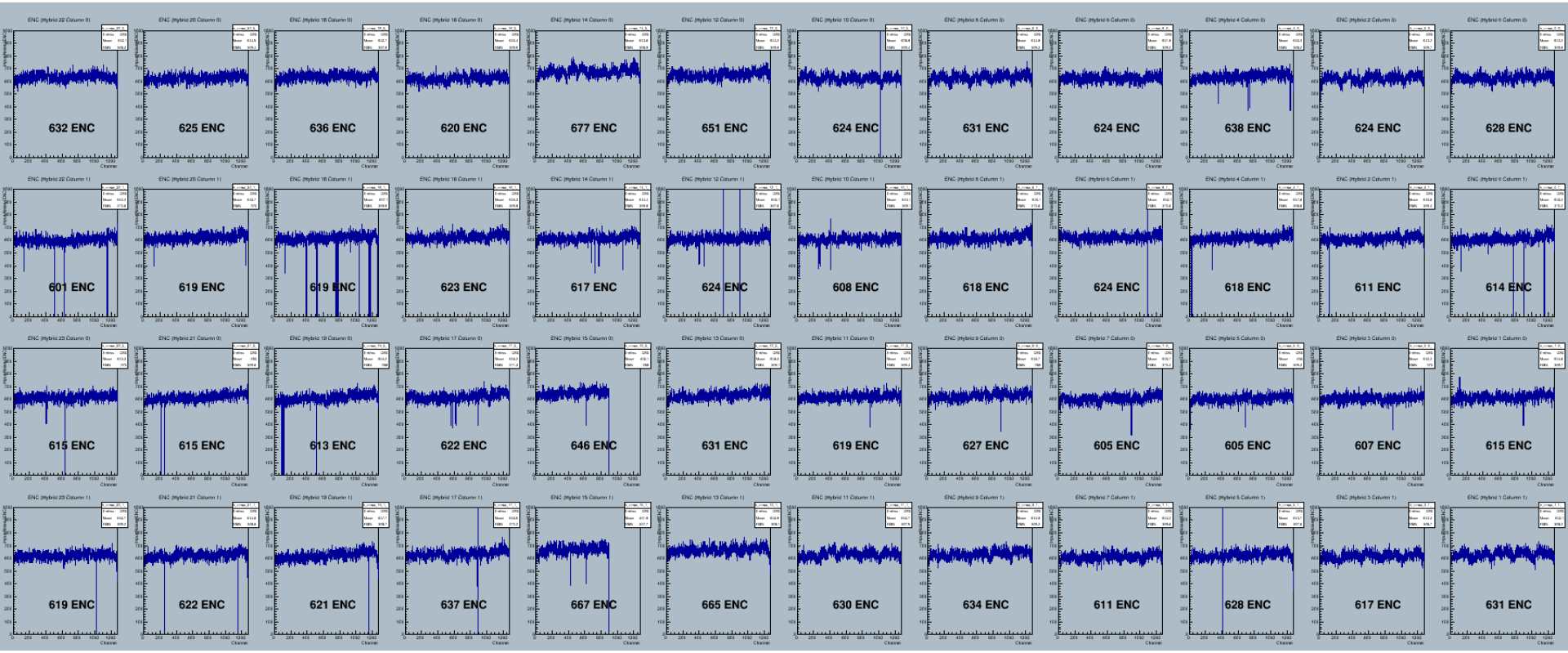


- 12 module stave side
  - Fully loaded and working
- “Tandem” DC-DC converter
  - Design by CERN group
  - Two converters in one PCB
    - Necessary due to current demand of 250nm chipset
  - LTC3605 chip
- “one wire” control
  - DS2413 chip
- Power bus split into 4 segments
  - Each drives 4 modules



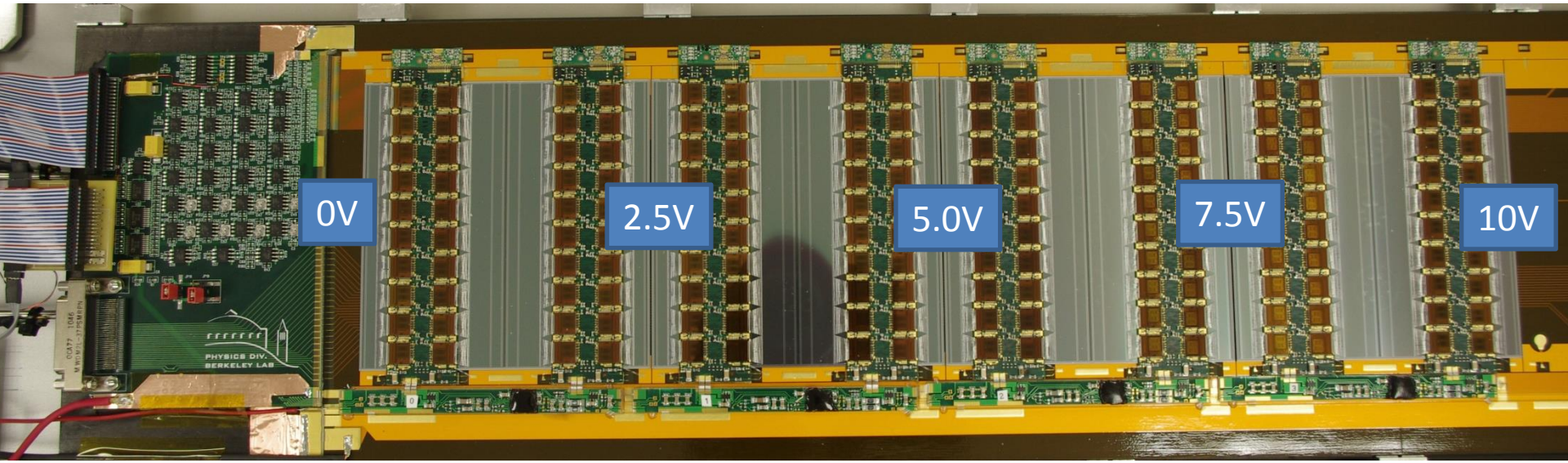
Tandem DC-DC on Stave 250

Stave 250 DC-DC ENC Results

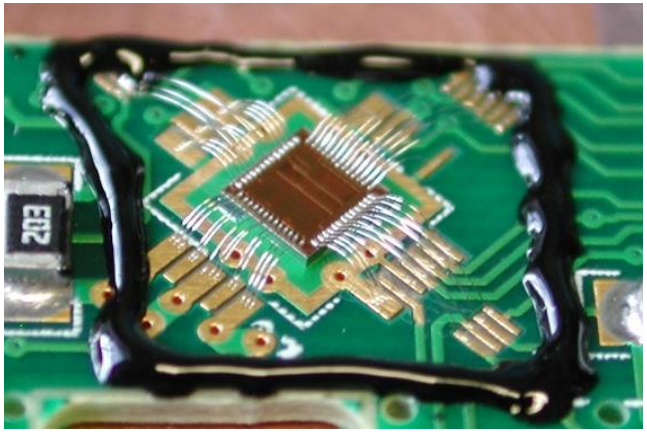


- Input Noise
  - Inner Columns 600 – 646 ENC, Outer Columns in range 610 – 677 ENC
- Double Trigger Noise Occupancy (not shown)
  - clean at 0.75fC Low occupancy at 0.50fC due to bad channels

Stave 250 SPP

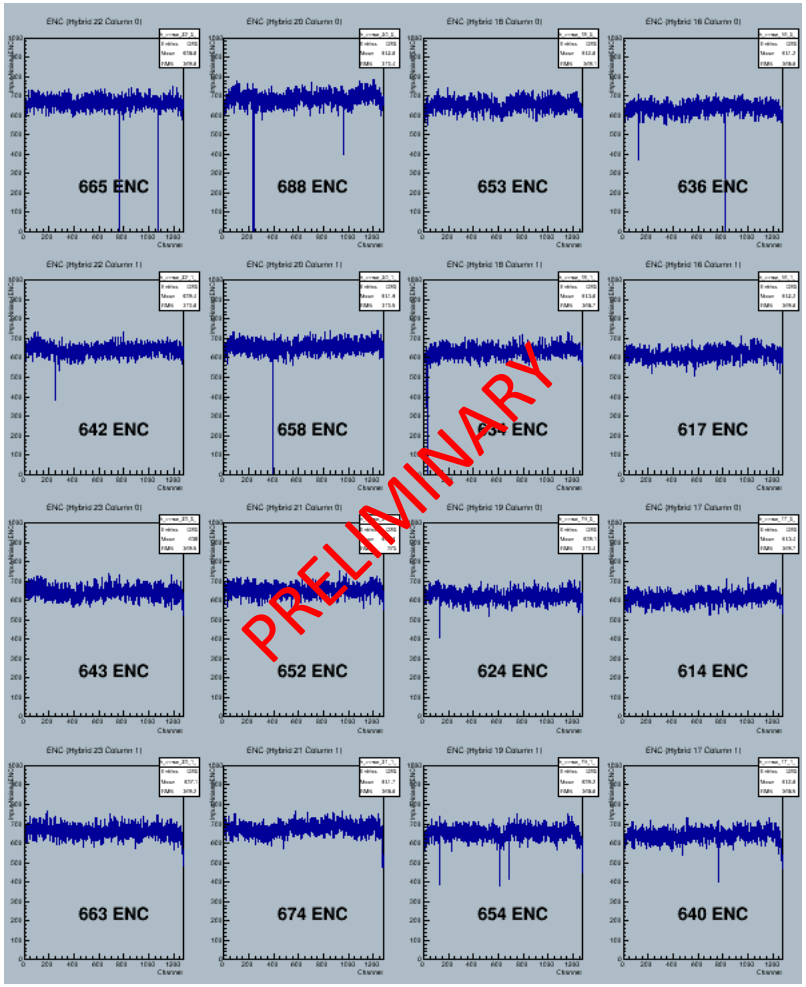


- Uses the Serial Power & Protection (SPP) ASIC
  - shunt regulation
  - bypass (under DCS control)
  - over voltage protection
- Still work in progress
  - Presently 4 (of 12) modules on the stave
  - Testing and optimisation continue



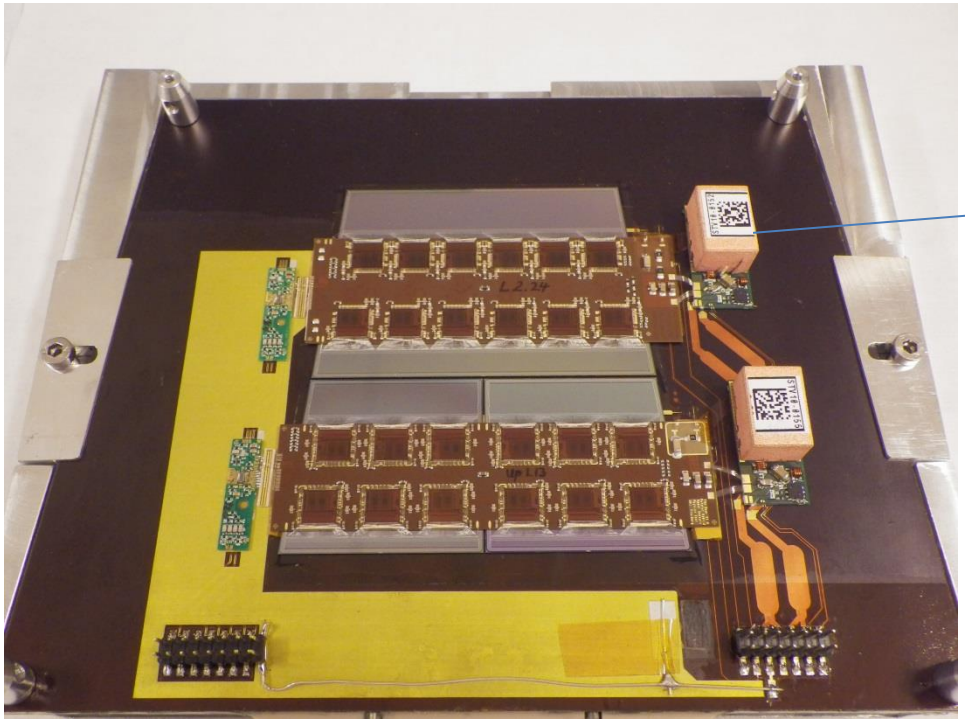
SPP chip

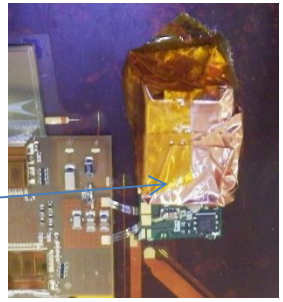
Stave 250 SPP ENC Results

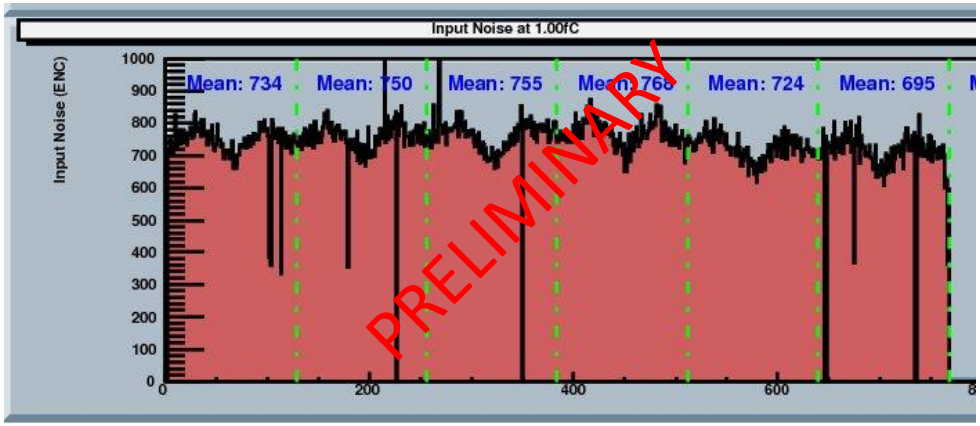


- Basics working, but latest ENC result is slightly higher than for Stave 250 DC-DC
  - Optimisation continues

First Petalet Results







- Additional Shielding around and under converter found necessary for best noise performance.
- Reasons to be confirmed. Possibilities include:
  - STV10 uses non-blind vias: signals may couple into CF skin and hence sensor backplane (no shield under sensor as for DC-DC staves)
  - HV bonds in close proximity to gap between shield and PCB
- Investigations continue

- Meanwhile noise approaching expectation
  - Characteristic shape related to integrated fanins on the sensors

Summary

130nm chipset

- HCC submission expected May
- Good results from ABC130
  - Results from half module in near future
- Smaller DC-DC converter made and under test
  - Works well but height will be a critical parameter
- Programme in place to identify radiation hard HV switch transistors
  - Awaiting full results from most recent irradiations

250nm chipset

- 12 module DC-DC powered stave
  - good noise performance throughout
- 12 module serially powered stave
  - Under construction, basics working for 4 modules
- First “Petalets” assembled and under test
  - Require additional shielding of DC-DC due to layout differences