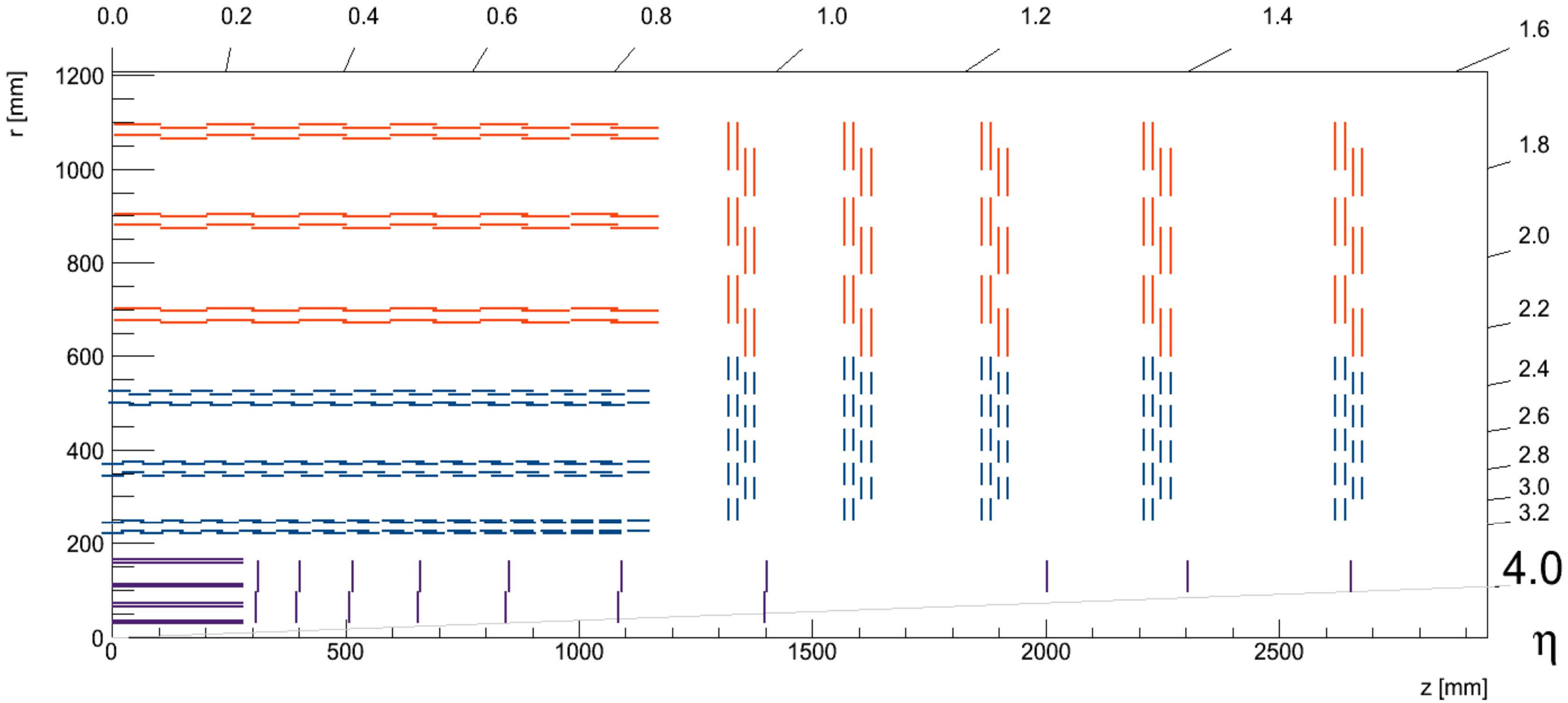
CMS Strips Readout

current status
future plans

Mark Raymond
ACES Workshop, March 2014

HL-LHC CMS tracker



beyond pixels, tracker implemented by two different module types

3 outer layers: ~ 10,000 2S modules, strips only, this talk

3 inner layers: ~ 7,500 PS modules, strips + pixels, next talk

HL-LHC challenges: power and triggering

both **2S** and **PS** modules must provide information to level 1 trigger

strips readout chip history

2 versions have now been produced - both in 130nm CMOS

CBC1 (2011)

128 wire-bond pads, 50 μm pitch
front end designed for short strips, up to 5 cm
DC coupled, up to 1μA leakage tolerant, both sensor polarities
binary unsparsified readout
pipeline length 6.4 μsec

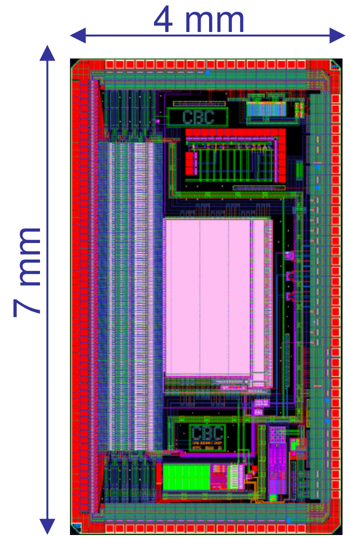
chip worked well in lab and test beam (few workarounds)

no triggering features

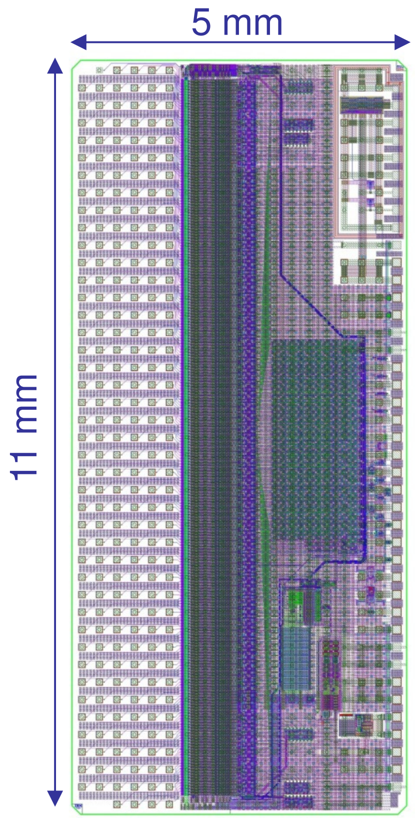
CBC2 (January, 2013)

254 channels
~same front end, pipeline, readout approach as CBC1

but
bump-bond layout
includes triggering features



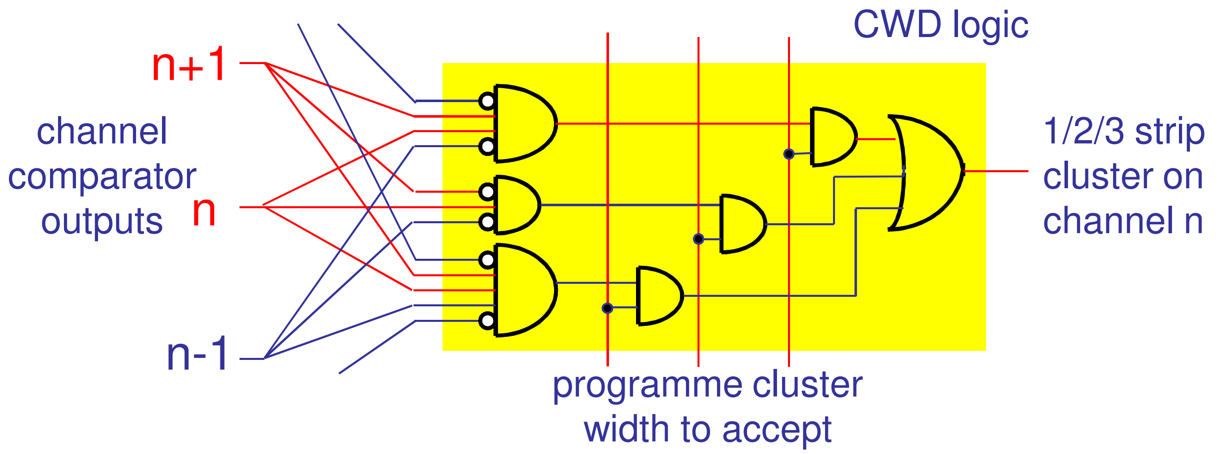
CBC1



CBC2

triggering implementation

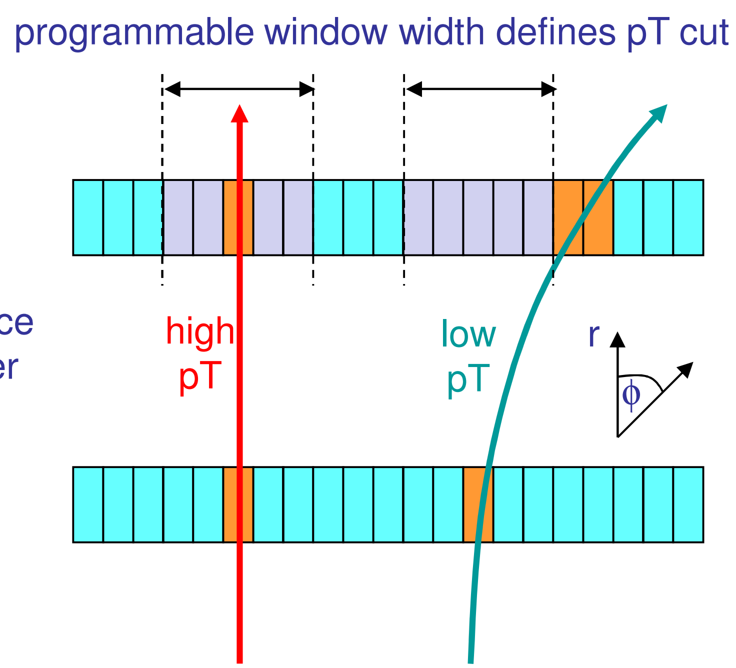
cluster width discrimination



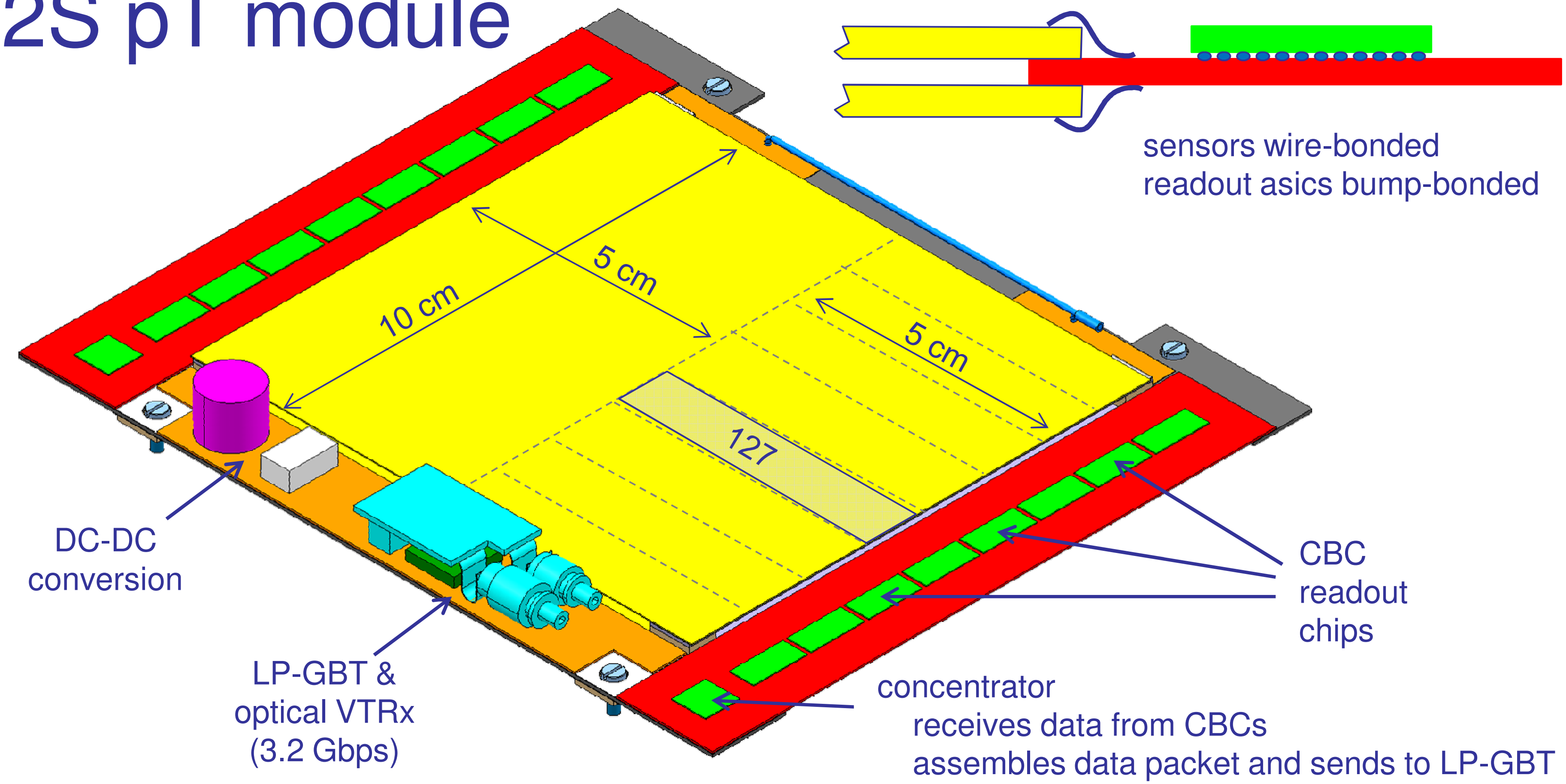
correlation

seed cluster in lower layer in coincidence
with cluster within window in upper layer

=> **pT stub**



2S pT module

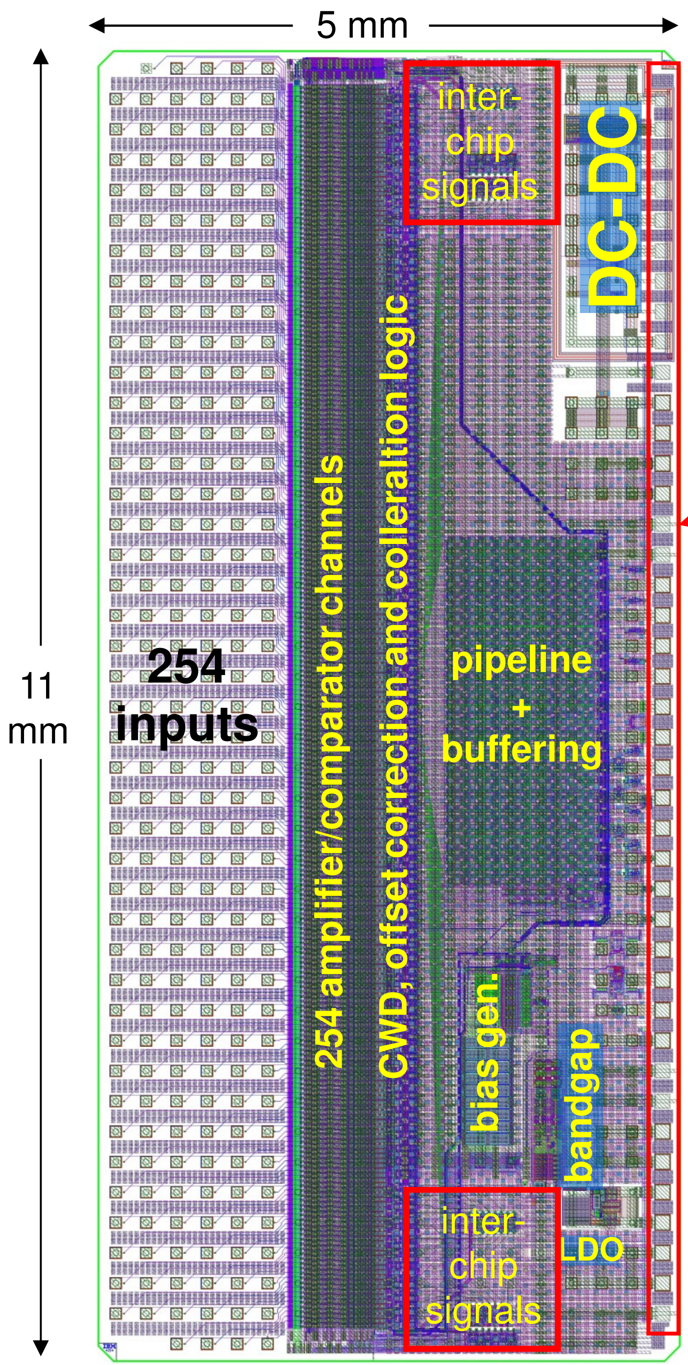


1 module type, ~10 x 10 cm^2 active sensor area for whole of region beyond r = 50 cm (endcaps too)

self-contained single, testable object; only needs power and optical connection to function

2S => 2 silicon sensors, each read out at both ends, strips 5 cm x 90 μm pitch, ~4000 channels total

16 bump-bonded CBC readout asics, each reads 127 strips from top layer, 127 from bottom



CBC2 layout

C4 bump-bond layout, 250 µm pitch, 19 columns x 43 rows

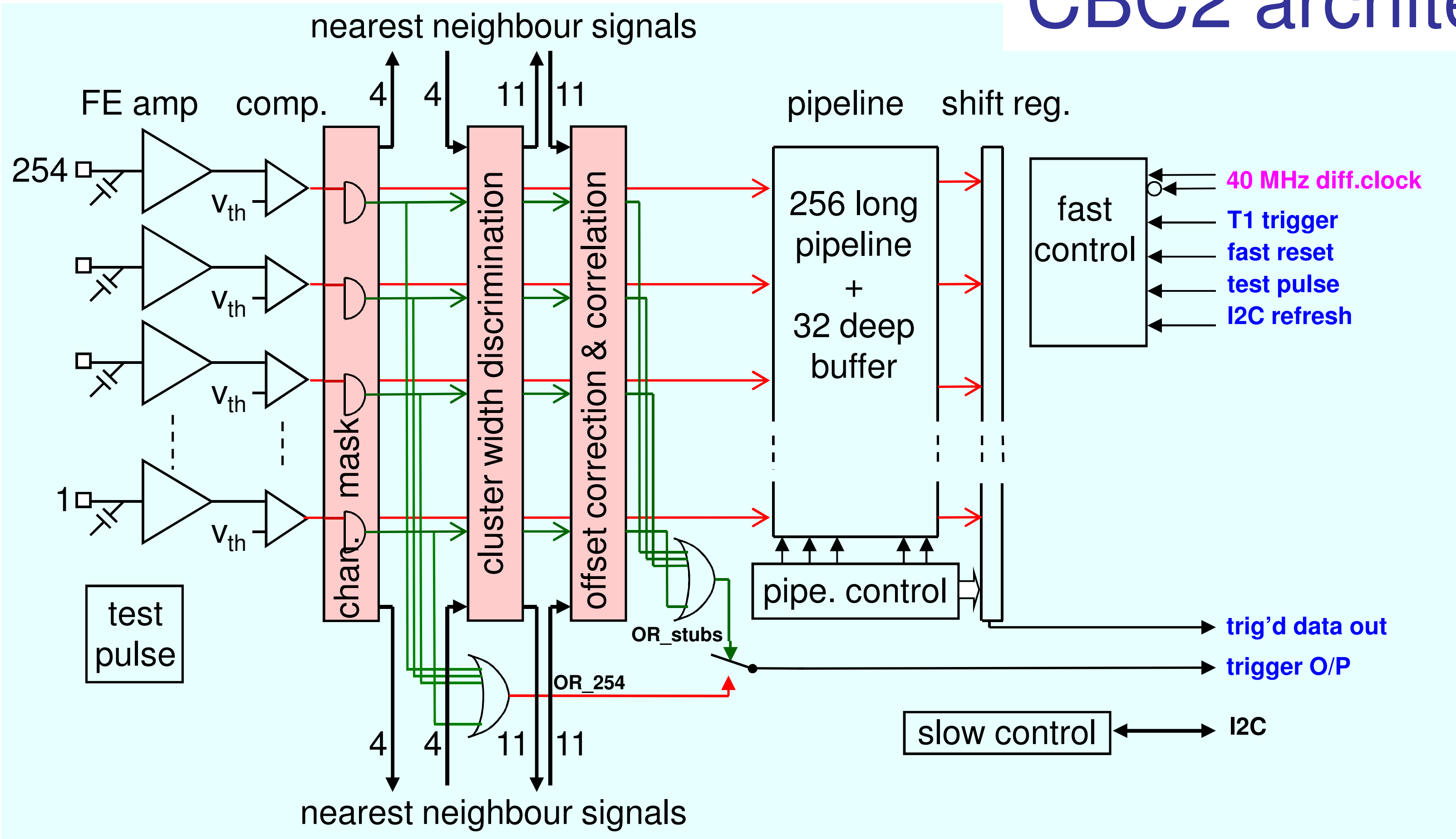
254 inputs (127 from each layer)

30 interchip signals (15 in, 15 out), top and bottom
for CWD and correlation continuity across chip boundaries

right-most column wire-bond (for wafer probe test)
access to:
- power
- fast control
- I2C
- outputs

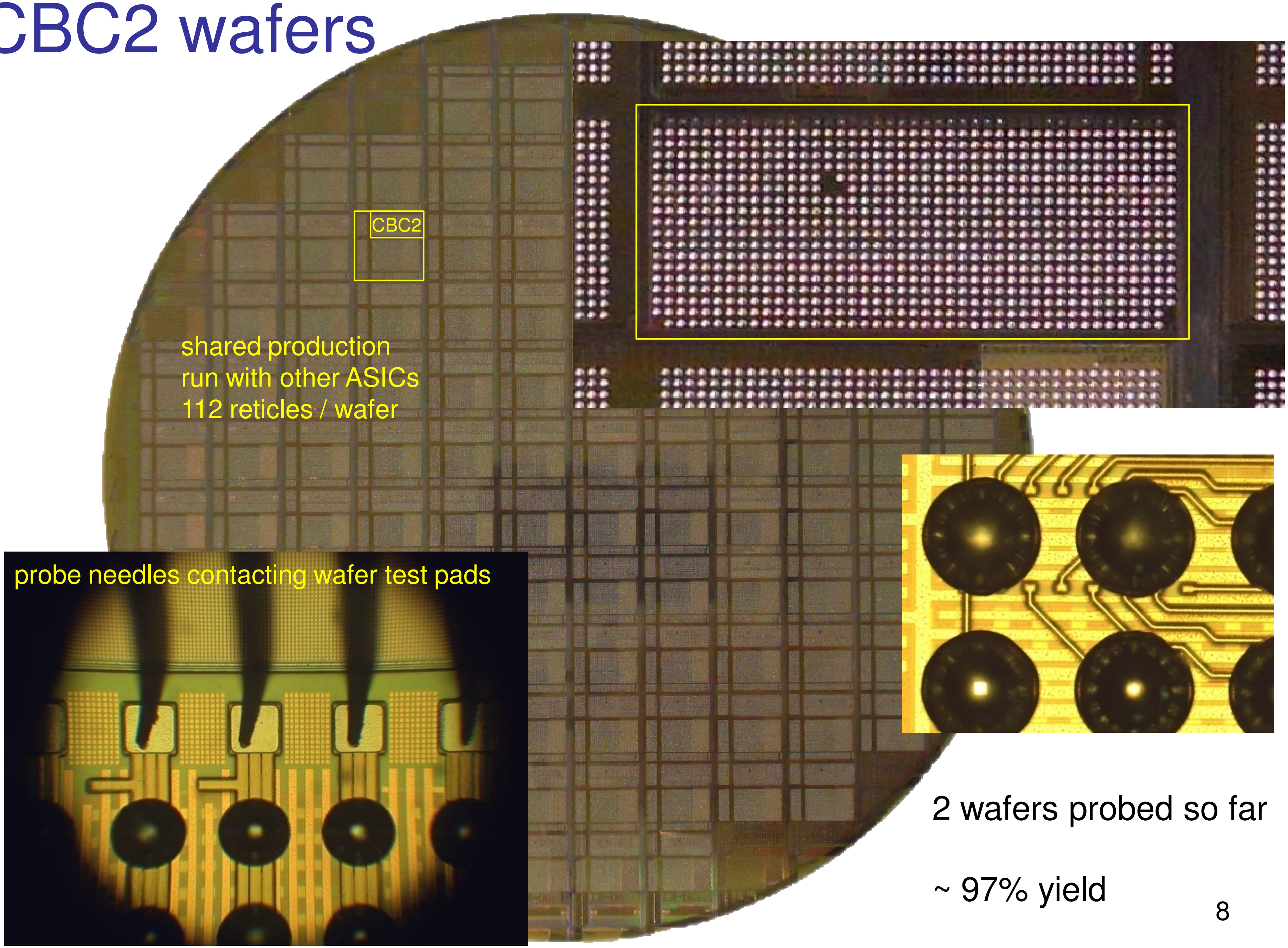
D. Braga,
M. Prydderch,
P. Murray
(STFC, RAL)

CBC2 architecture



254 channels: 127 from each sensor layer
channel mask: block noisy channels from trigger logic
CWD logic: exclude wide clusters >3
correlation logic: for each cluster in lower layer look for cluster in upper layer window
trigger output: 1 bit per BX indicates correlation logic found one (or more) stubs
triggered data out: unsparsified binary data frame in response to L1 trigger

CBC2 wafers



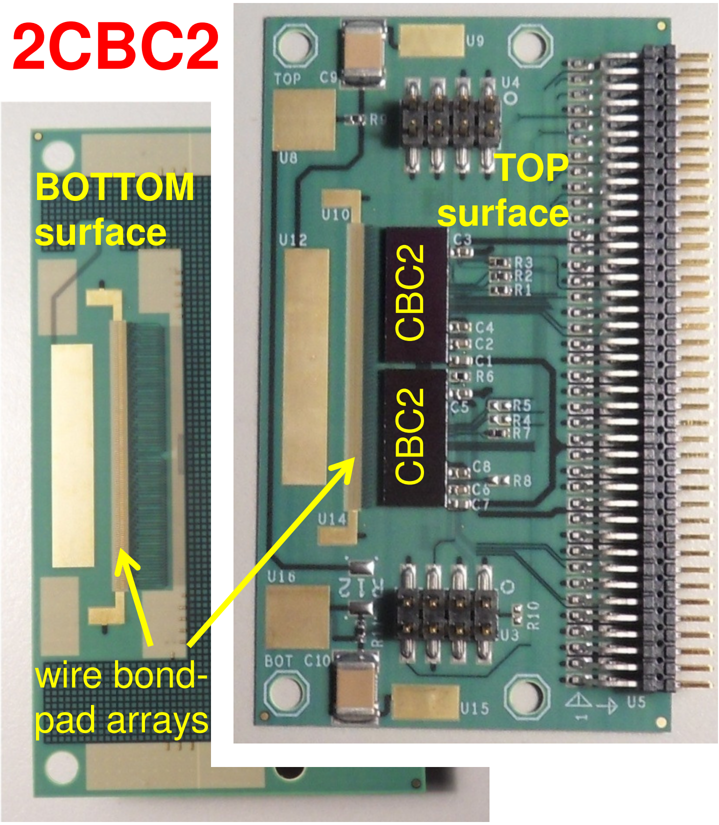
2 wafers probed so far

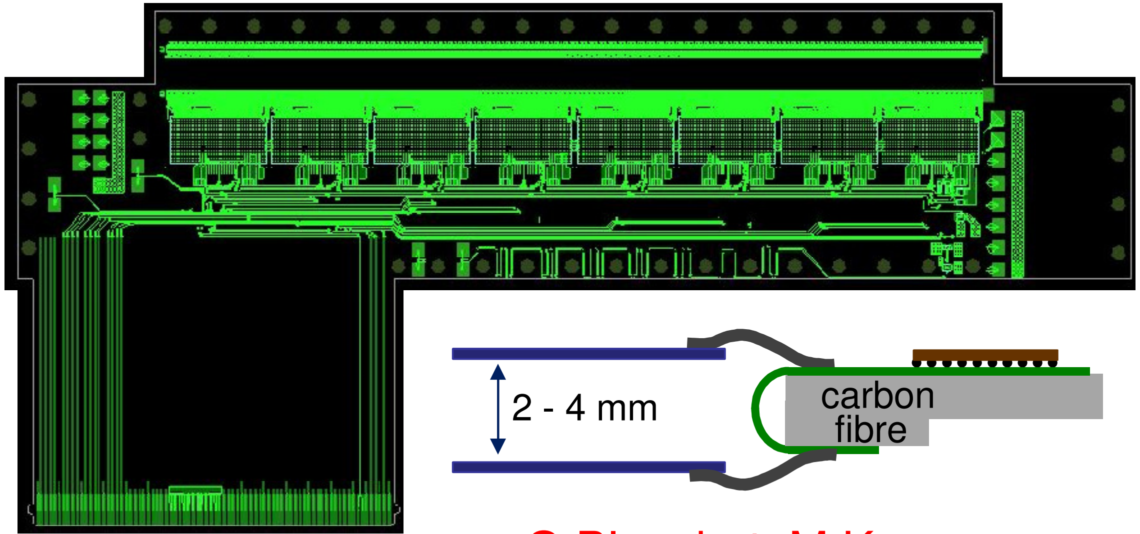
~ 97% yield

hybrid developments (CERN)

8CBC2flex

2CBC2

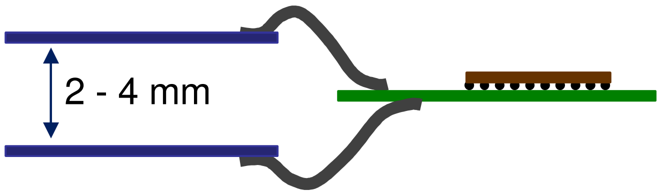




G.Blanchot, M.Kovacs

2CBC2

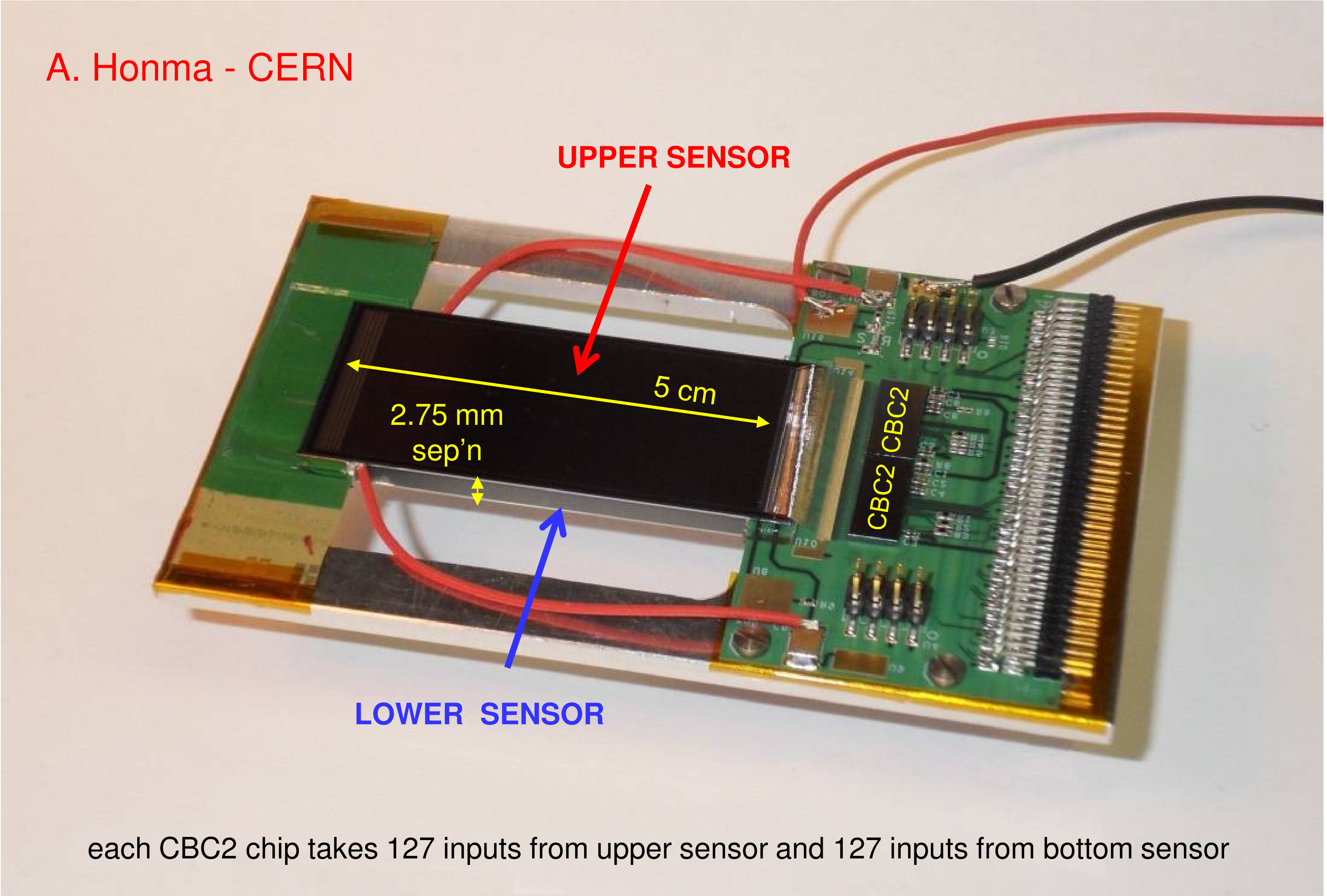
- 2 chips prototype - available mid 2013
- 6 layer "rigid" technology - (actually quite flexible - 265 µm thick)
- fully functional, but flexibility and thickness causes bonding problems when constructing modules



8CBC2flex

- full size 8 chips, 4 layers
- "wrap around" hybrid support should help with module manufacture (support thickness can be chosen to achieve desired sensor spacing)
- currently awaiting prototypes

2CBC2 module



CBC2 performance

all core functionality meets requirements

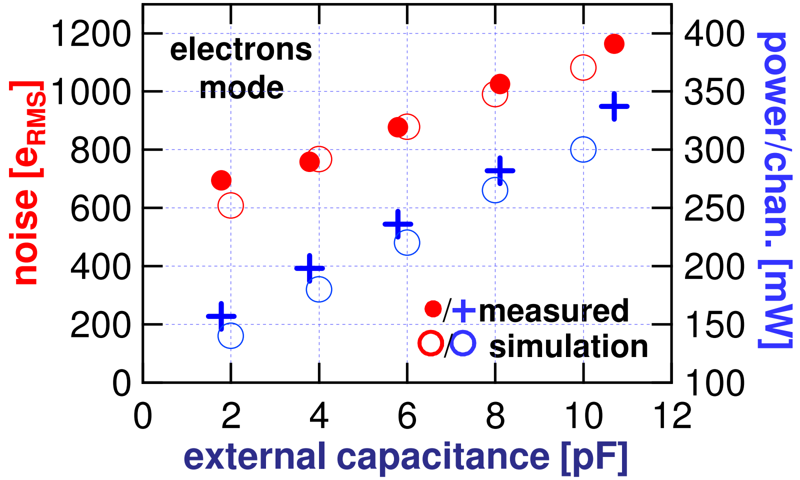
- correlation functionality verified with test pulses, cosmics (backup), and in test beam (next slide)

analogue performance close to simulation expectations and specifications

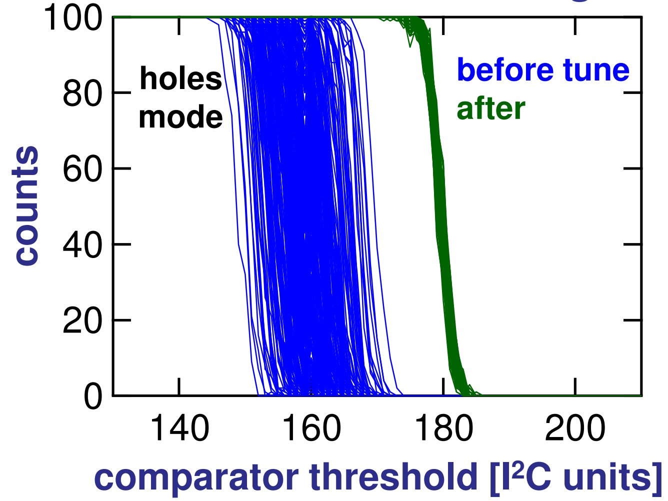
- e.g. 1000e noise for 5 cm strips (~8 pF)
- achievable for total channel power of 350 μW

radiation tests in process this year (ionizing and SEU)

noise & power vs. external capacitance



channel offsets tuning



Desy test beam

25th November - 1st December 2013

Datura telescope + 2 pT modules

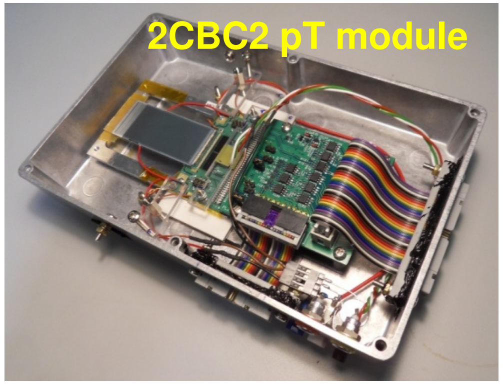
(1 rotatable to simulate B-field effect)

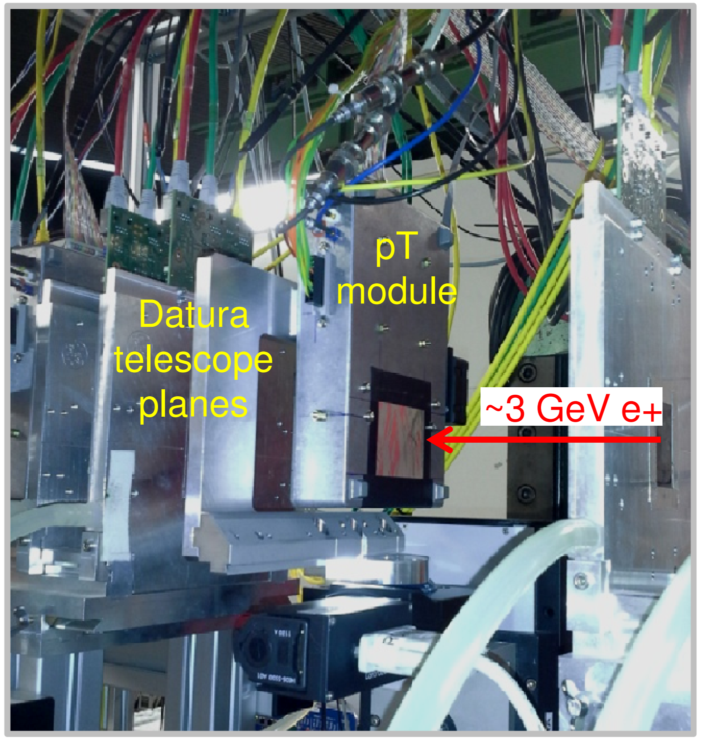
1) CNM sensors: p-on-n
   5 cm, 90 μm pitch

2) Infineon sensors: n-on-p
   5cm, 80 μm pitch

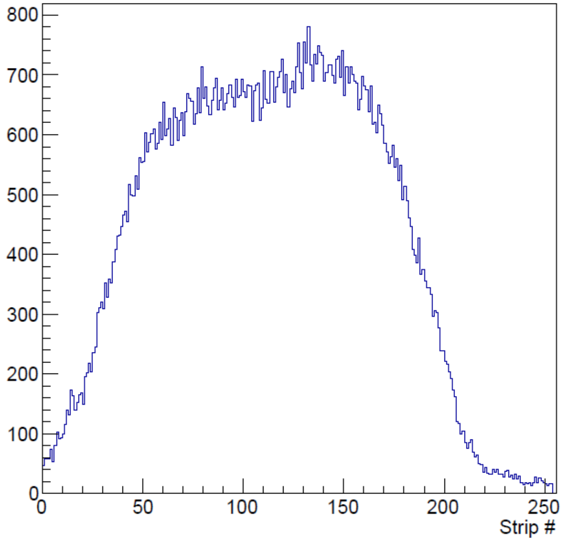
control and DAQ based on CERN GLIB emulating GBT functionality

analysis ongoing

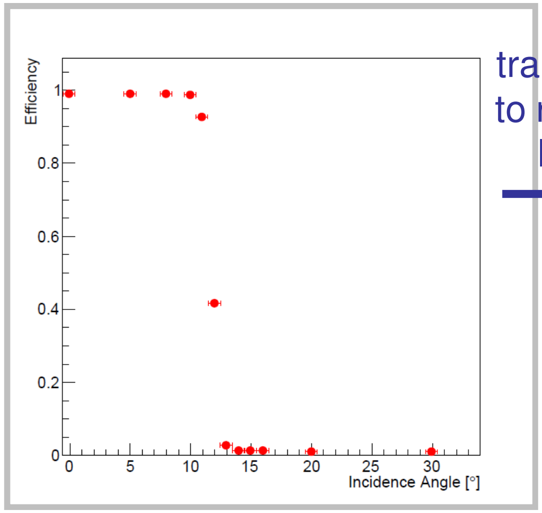




beam profile in pT module

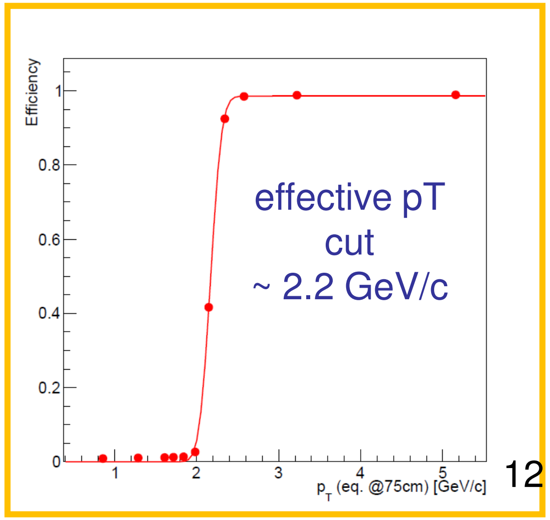


angular scan of CNM module in beam
window width = +/-7



translated to r=75cm layer

M.Pesaresi



next step: CBC3

next version of chip should incorporate all features required for HL-LHC

final choices for front end

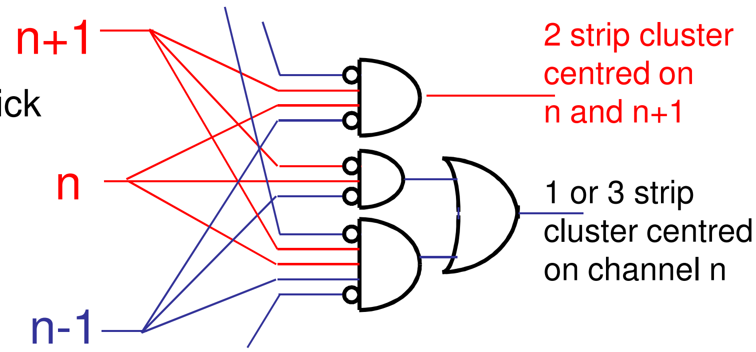
sensor baseline choice now n-on-p, AC coupled, 200 µm thick

strip length possibly up to 8 cm (8 inch wafers)

=> amplifier optimisation

½ strip cluster resolution

2 strip cluster position assigned to mid-point

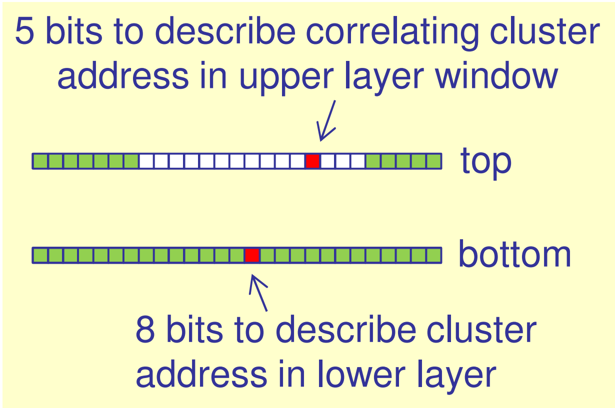


stub data definition

8 bits address (½ strip resolution) of cluster in lower layer

5 bit bend information

address of correlating cluster in upper layer



recent developments

pipeline length increase: 12 / 25 µsec

L1 trigger rate increase: 500 kHz / 1 MHz

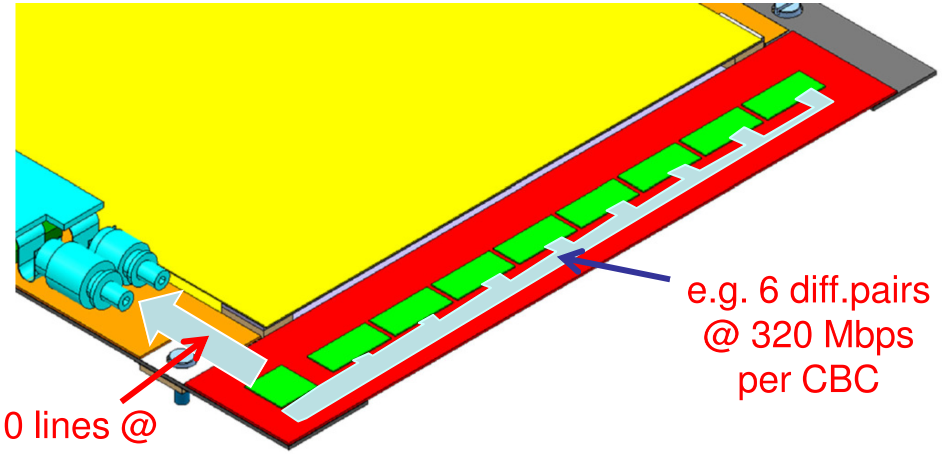
changes to bump-bond pad layout

current layout rather "close to the edge" of hybrid manufacturing capabilities

too close to minimum track widths and via diameters

bump-bond pad pitch increase is being considered

readout architecture



LP-GBT off-detector data bandwidth 3.2 Gbps

1.6 Gbps / half module
shared by stubs and readout data

stub data transmission CBC to concentrator

need capacity to transmit up to 3 stubs/BX
per CBC for negligible loss of efficiency
=> 39 bits / BX
(usually stub occupancy << 1)

readout data CBC to concentrator

at 100 kHz L1 trigger rate there was no need to sparsify
1 bit / BX CBC to concentrator, 16 bits / BX off-detector (only 20% of bandwidth)
at 1 MHz off-detector bandwidth is exceeded
we have to sparsify somewhere

choice is to sparsify readout data in concentrator

some advantages
keep CBCs operating synchronously (concentrator can check)
some functions performed only once (not 8x) - e.g. timestamping
implement purely digital concentrator functionality in low-power 65 nm

concentrator functionality under study and development at Universite Claude Bernard - Lyon

(some more details in backup)

module power comments

CBC: 1.2V

CBC2 (for 5 cm strips) ~ 350 uW / channel, 90 mW / chip

1440 mW for 16 chips

(**but** CBC3 power will increase due to additional digital functionality & data transmission)

LP-GBT: 1.2 V

500 mW (estimate)

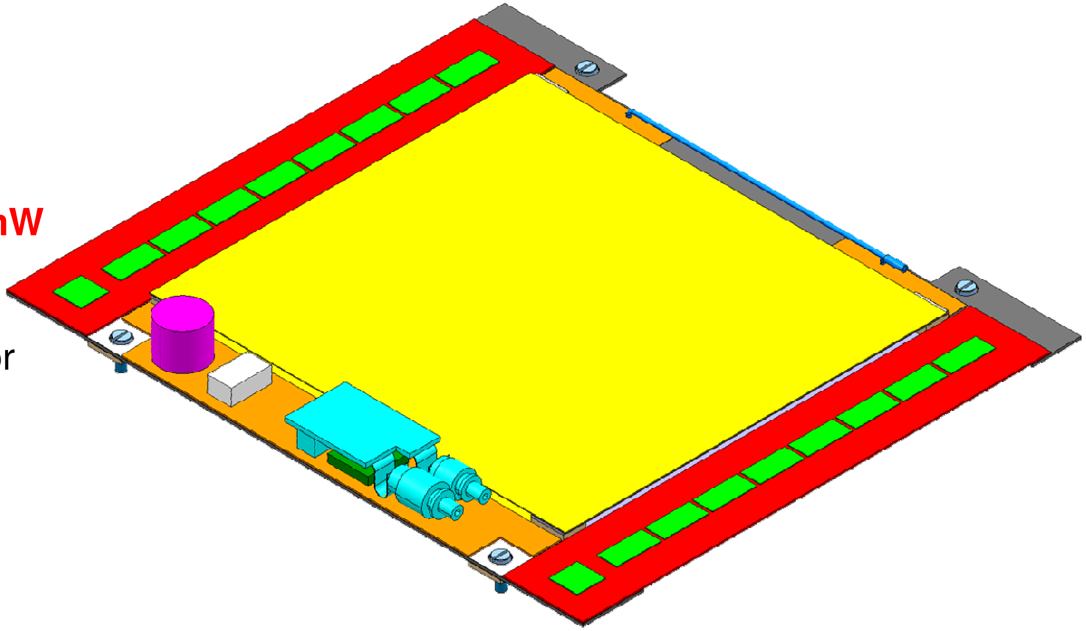
optical: 2.5 V

LP-GBLD : **200 mW**, GBTIA: **100 mW**

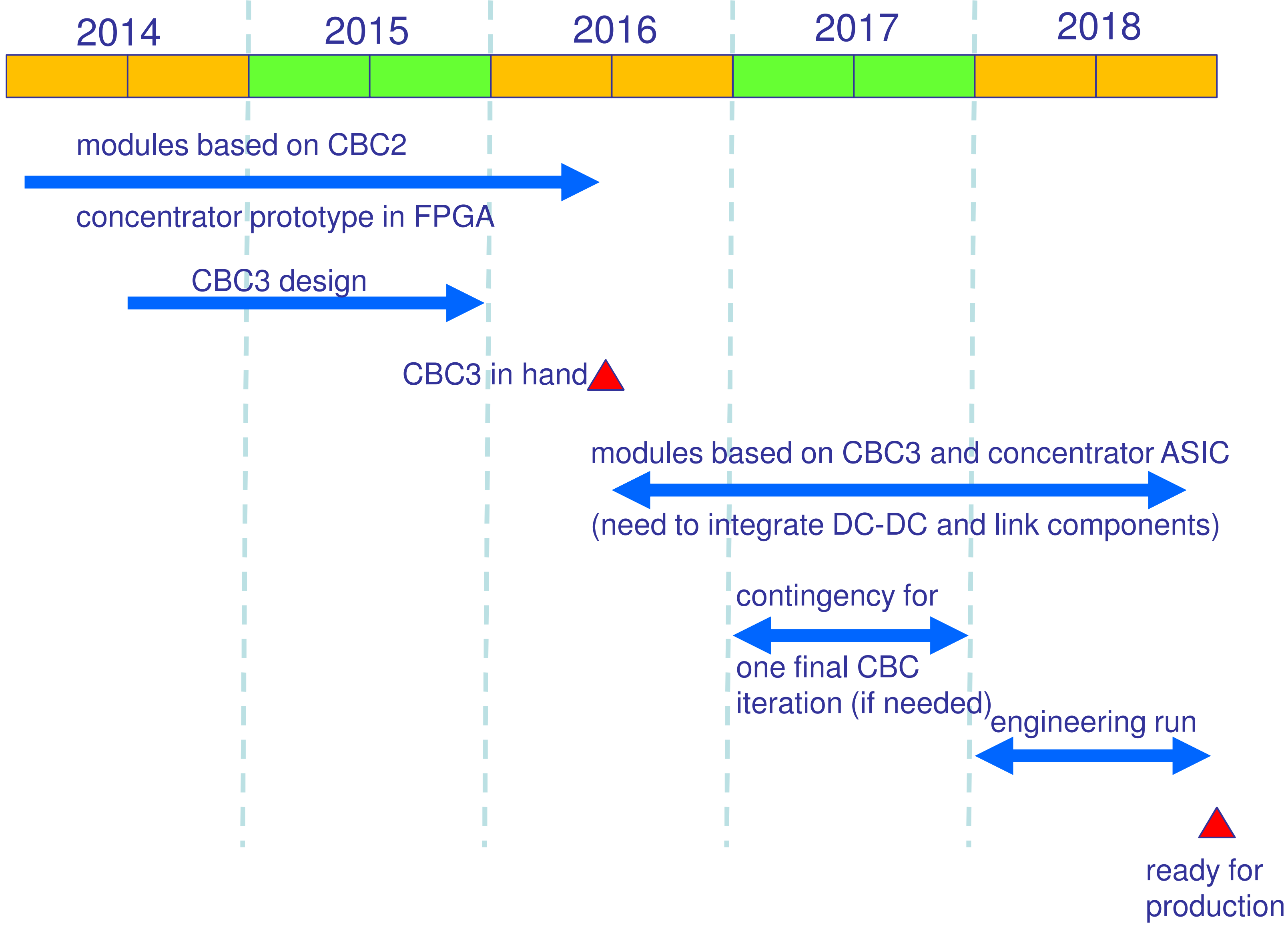
total so far: 2240 mW

but this doesn't include concentrator

< 3W per module may be achievable



CBC development timeline



summary

a lot of progress on readout of strips region of outer tracker

bump-bond chip and 2CBC2 hybrid developed

successfully operated in lab and test beam
triggering features functionality demonstrated

GLIB based DAQ system well-advanced

system level definition is progressing

when finalized can complete design of CBC3 (the final prototype)

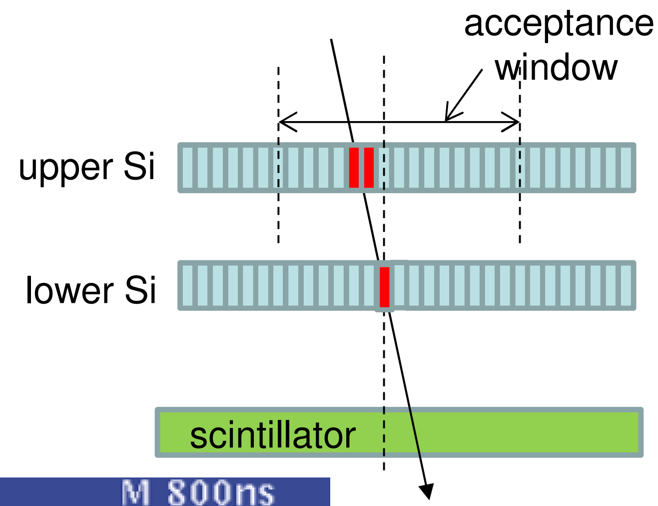
other module components can be integrated into module as they become available

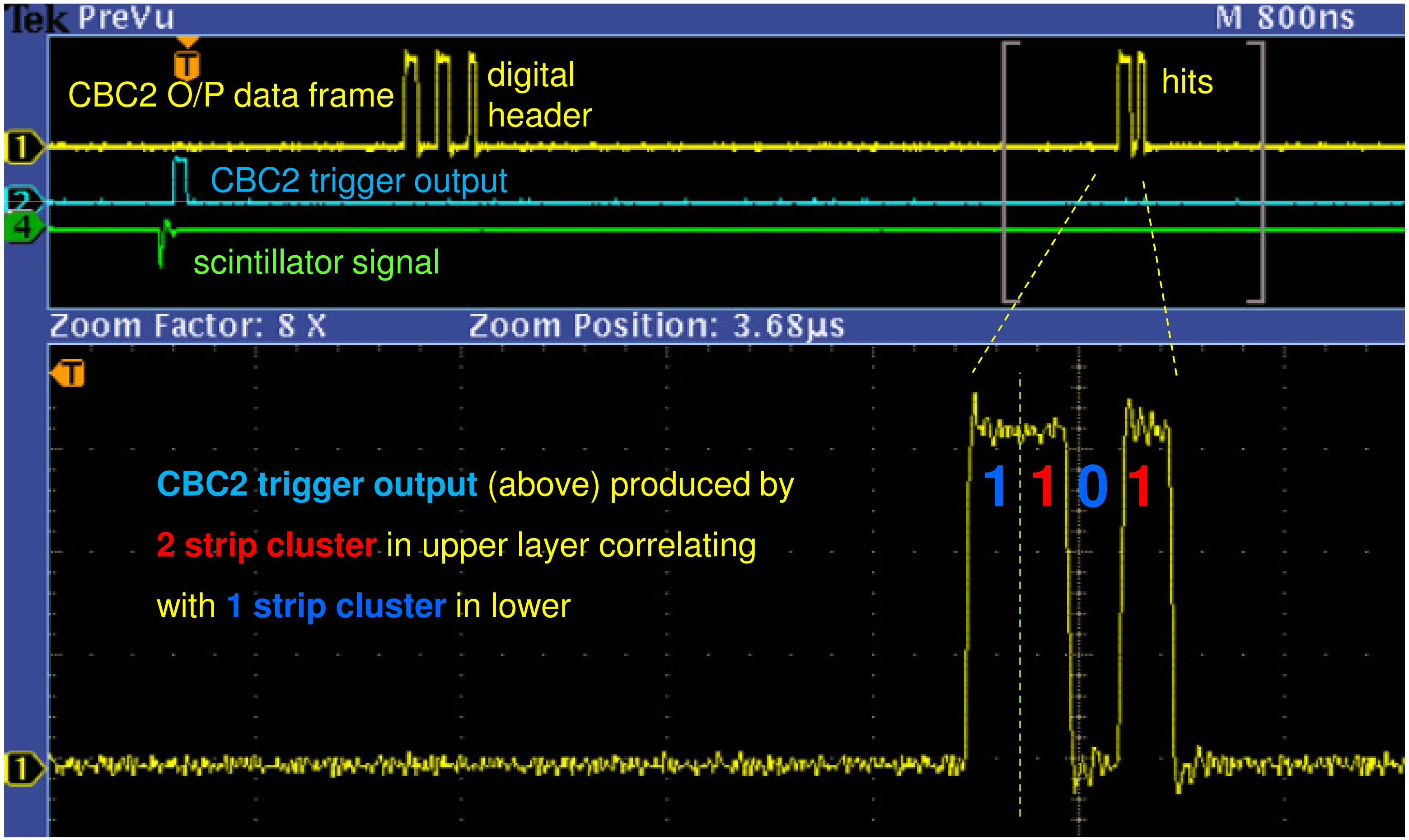
EXTRA

correlation using cosmics

data stream output bits alternate between upper and lower layers

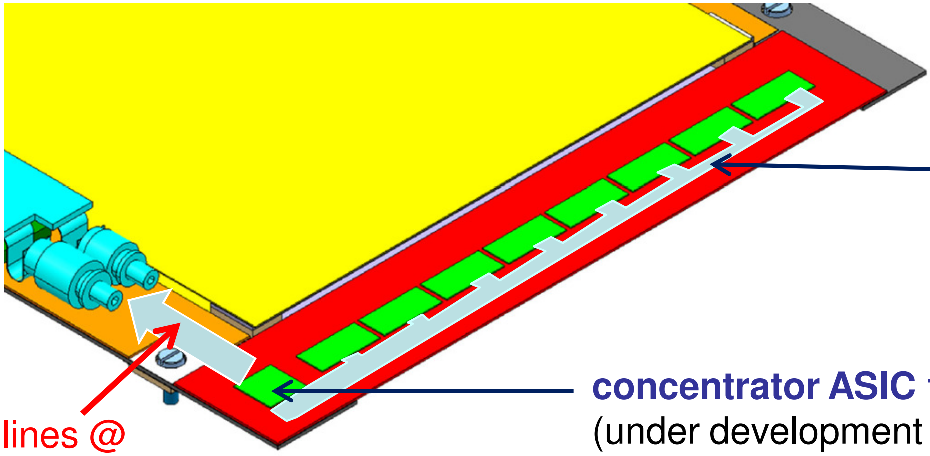
=> …0001101000…. bit pattern signifies
1 strip cluster in lower layer
and 2 strip cluster in upper layer



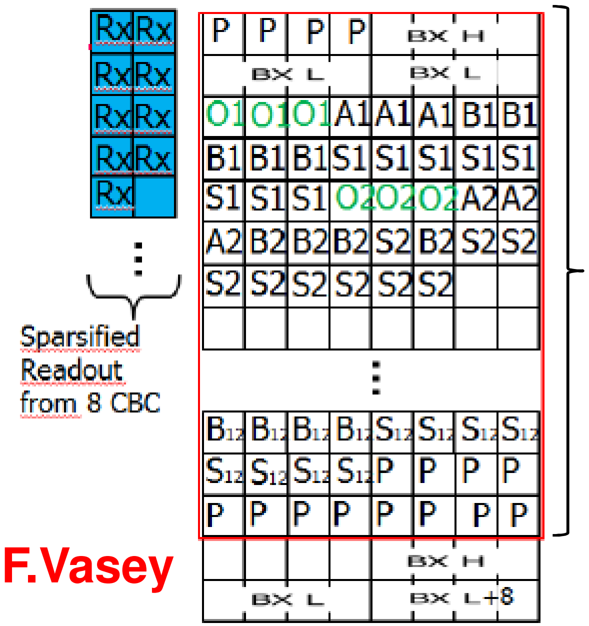


=> correlation logic working as expected

readout data details



10 lines @ 160 Mbps



200ns = 8 BX block length can contain up to 12 stubs

P = Parity and synch.
BX = timestamp T_{START}
O = offset w.r.t. T_{START}
A = CBC address
B = bend info
S = strip address

data: CBC to concentrator

39 bits / BX stub data

@1 MHz L1 need to send 254 bits/µs = ~ 7 bits/BX

=> ~ 48 bits/BX

e.g. 6 diff.pairs @ 320 Mbps

high density of tracks on hybrid between CBCs and concentrator

concentrator ASIC functionality

(under development : Universite Claude Bernard - Lyon)

- sparsify the readout data (unavoidable at 1 MHz L1)
- sort & assemble stub info
- construct and transmit combined data packet to GBT

data: concentrator to LP-GBT

- organize data in synchronous blocks of fixed length
- block lengths chosen for sufficiently high efficiency

=> fixed latency for trigger data

F.Vasey

CBC2: wafer probing results

2 wafers (of 8) probe-tested so far

basic chip setup procedure:

  standard set of I2C parameters, low resolution offset tuning

data acquisition

  supply current, bandgap and LDO output voltage
  comparator offsets and s-curves
  bias generator currents and voltages
  output data for all pipeline cells
    (looking for stuck pipeline cells)

yield ~ 97 %