CMS Pixel-Strip Project

ACES 2014 - Fourth Common ATLAS CMS Electronics Workshop for LHC upgrades

Wednesday, 19 March 2014

Kostas Kloukinas

PH-ESE, CERN

on behalf of the CMS Tracker PS module R&D team

Outline

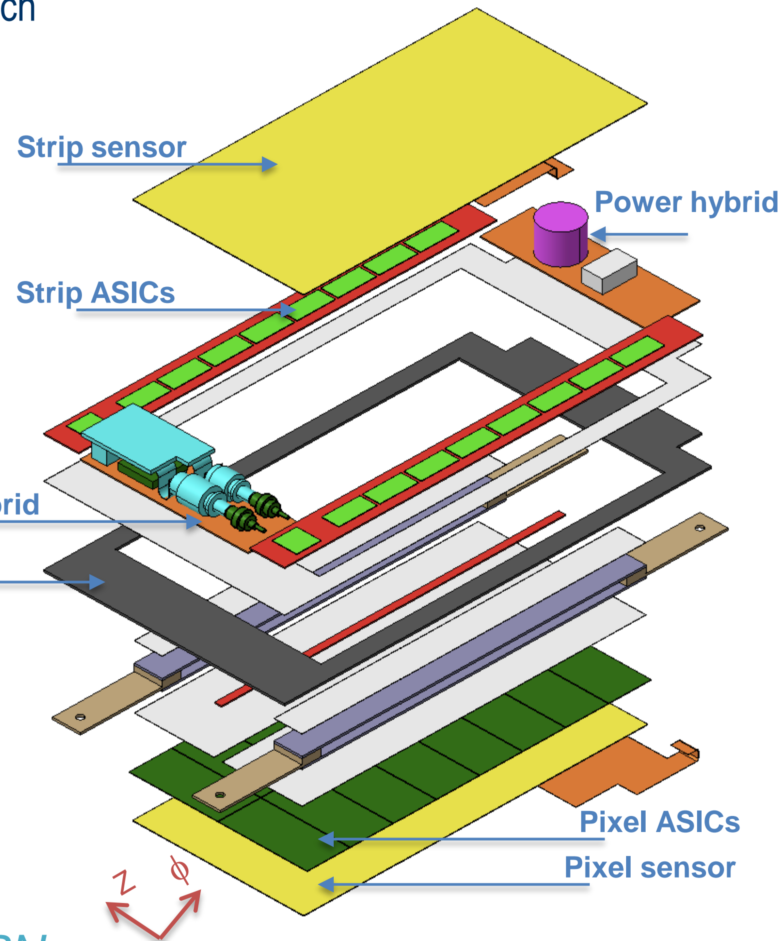
- Motivation
- The Pixel-Strip Module concept
- The Macro Pixel ASIC (MPA)
- The MPA-light prototype
- Conclusions & Future Plans

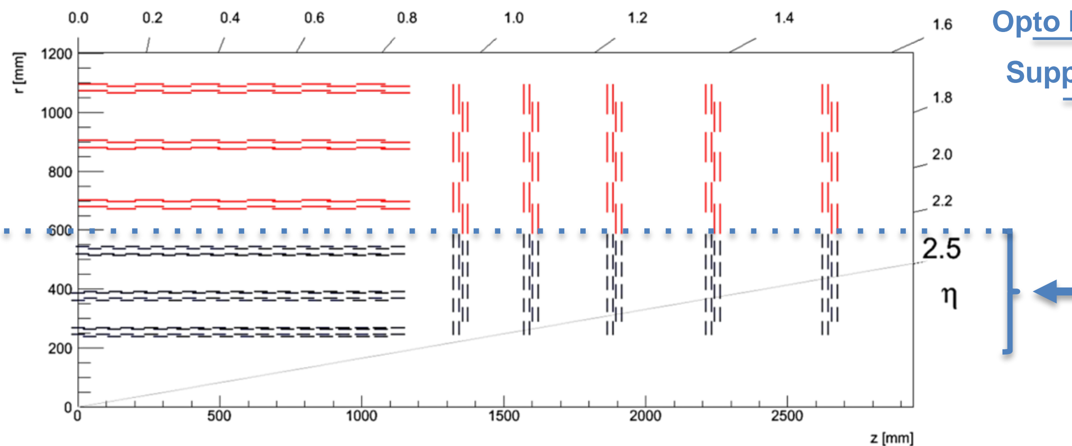
Motivation

- CMS Tracker upgrades at High Luminosity LHC
  - HL-LHC: sustained luminosity of $5x10^{34}$ $cm^{-2}s^{-1}$
  - More than 100 pileup events per bunch crossing @ 40MHZ
  - μ, e and jet rates exceed the 100 kHz rate
    - Increasing thresholds would affect physics performance
    - Performance of algorithms degrades with increasing pile-up
- Add tracking information at Level-1 selection
  - Reconstruct “all” tracks above 2 GeV
  - Identify the vertex origin along the beam axis with ~ 1 mm precision
- Modules with p_T discrimination
  - Reject locally signals from low-p_T particles

The Pixel Strip (PS) module

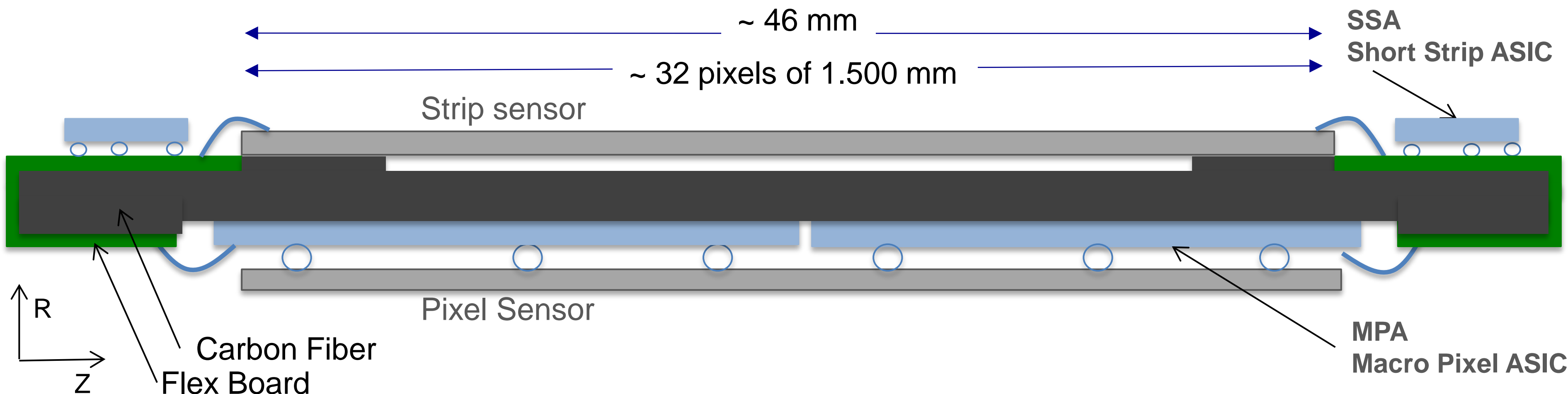
- A hybrid module of 5 x 10 cm^2 composed from:
  - One Strip Sensor layer of 2 x 960 strips of 25mm at 100µm pitch
  - One Pixelated layer of 32 x 960 pixels of 1500µm x 100µm
  - Coincidence of the two layers provides p_T cut
  - Pixel hit position provides Z coordinate information
  - The PS module is a self contained building block
- Upgrade for the Inner modules of the CMS Outer Tracker
  - Efficient at high occupancy in radial regions below 50cm

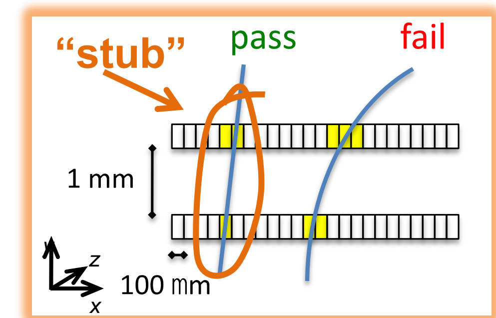




G. Blanchot, M. Kovacs C. Fuentes, F. Vasey CERN

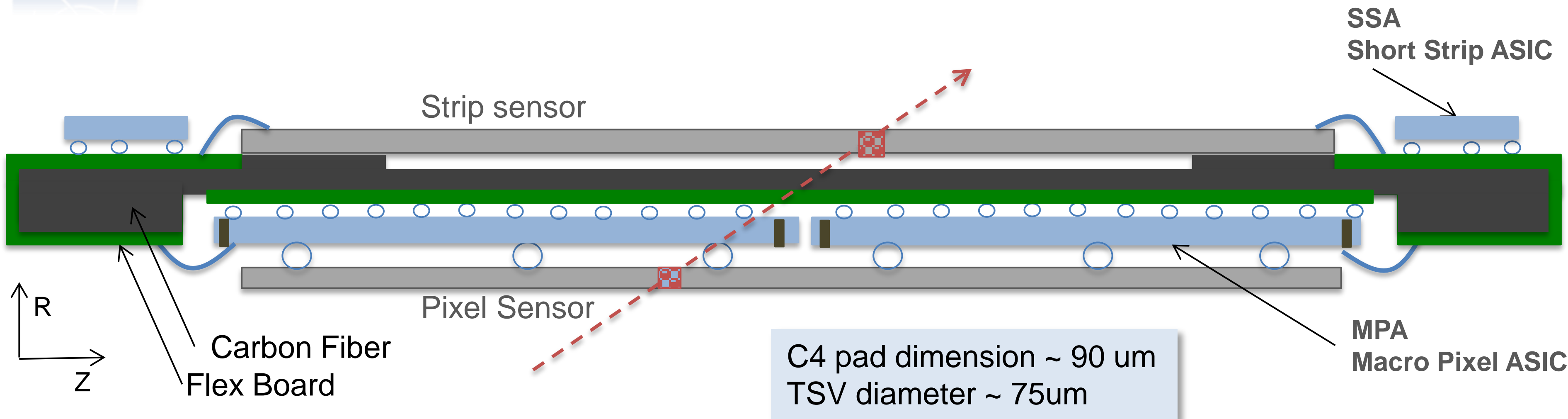
PS module (baseline)





- Each PS module is composed from Pixel and Sensor layers.
- Strips are readout from 16 **S**hort **S**trip **A**SICs (**SSA**)
- Pixels are readout from 16 **M**acro **P**ixel **A**SICs (**MPA**)
- Pixel/Strip hits are analysed to find stubs in the MPA periphery.
- A stub is a particle with a momentum > 2 GeV/c which crosses the two sensor layers.
- Found Stubs are sent out at each Bunch Crossing (25 ns) while the full event is stored locally and is sent out only if requested with a L1 Trigger signal.
- L1 Trigger Signal is generated outside from the Tracker.

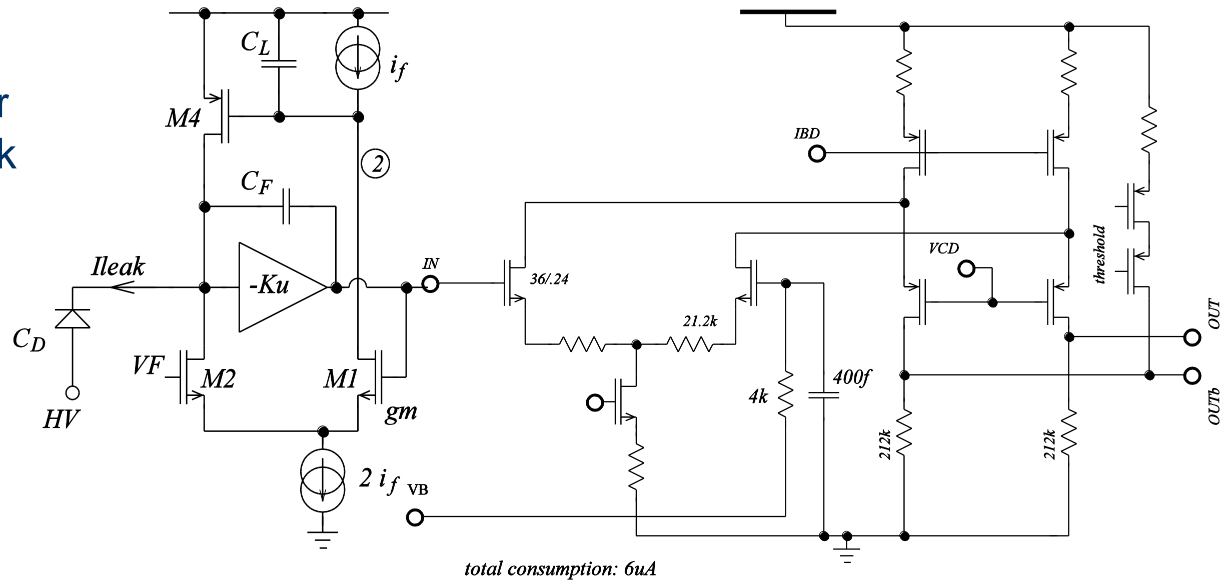
PS module with TSVs

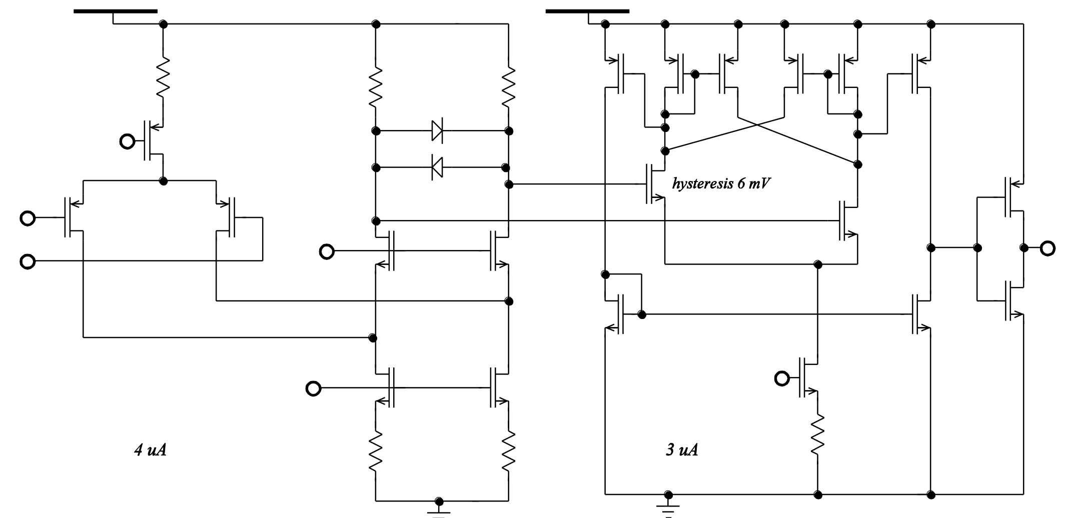


- Connectivity along Z-direction on modules can make possible the tracking of particles that cross the readout areas of two MPAs
- Increases the average readout efficiency by ~10% (more important for tracks at high η)
- This interconnectivity necessitates the use of TSVs on the MPAs
- Possible implementations include the use of bumped flex board
- This solution can improve the power distribution on the MPAs
- The TSV option is being evaluated and preliminary contacts with industry are in place

MPA analog FE architecture

- Transimpedance Preamplifier with Krummenacher feedback leakage compensation for n+ on p- detectors
- Single-ended to differential folded cascode stage with resistive load
- Discriminator with:
  - PMOS folded cascode input
  - Swing limiter based on PMOS working in diode configuration
  - Second stage with hysteresis (6mV)



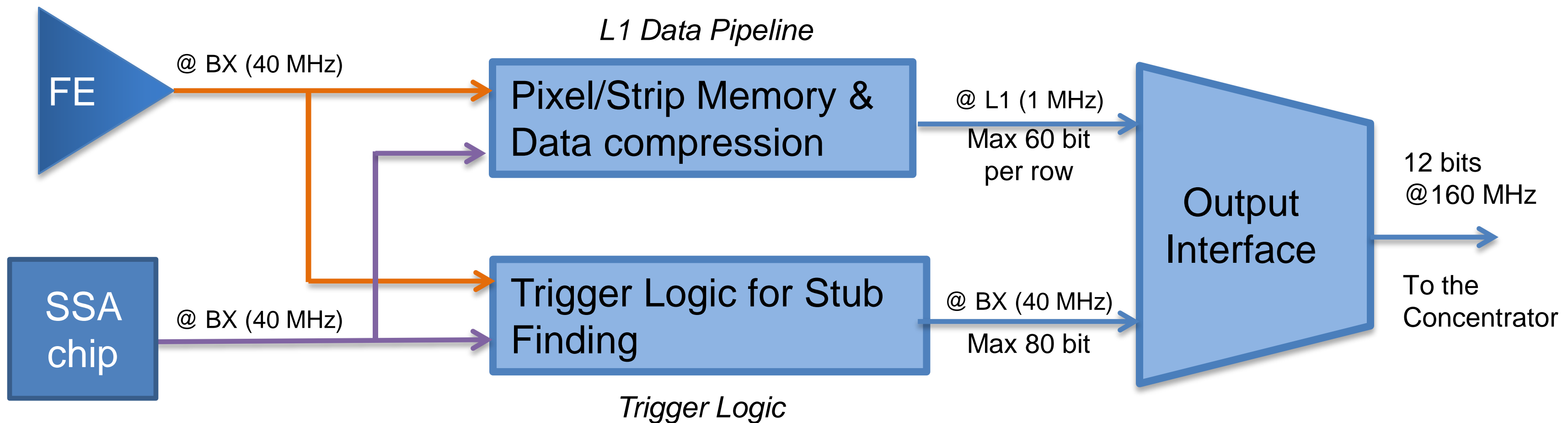


J. Kaplon, CERN

MPA Readout Data Flow

Input each 25 ns (40 MHz):

- Pixel hits from Front- End: 120 columns x 16 rows = 1920 hits
- Strip hits from SSA chip: 120 hits

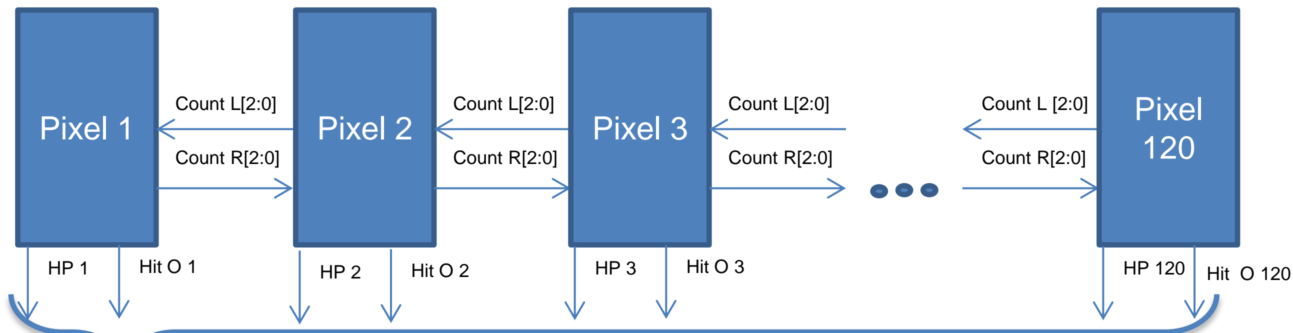


L1 Data Pipeline stores data for the duration of the L1 latency (10 or 20 μsec).
Upon arrival of L1, data are sent to the Data Compression block and then to concentrator.

Trigger Logic elaborates inputs synchronously with the bunch crossing and looks for the coincidences between pixel and strip hits in order to generate stubs.

MPA Trigger Logic for Stub finding

- Wide Cluster Elimination + Centroid Extraction (6 wire x 100 um for each pixel)

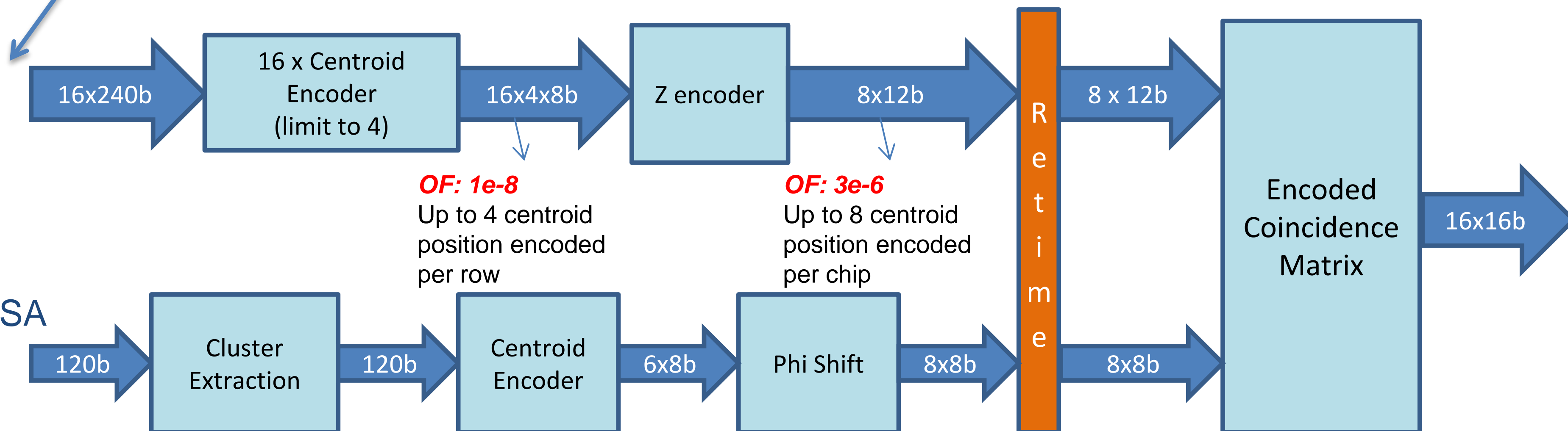


Advantages:

- *Keep all Z coordinates*
- *Find all the possible stubs*

Limitations:

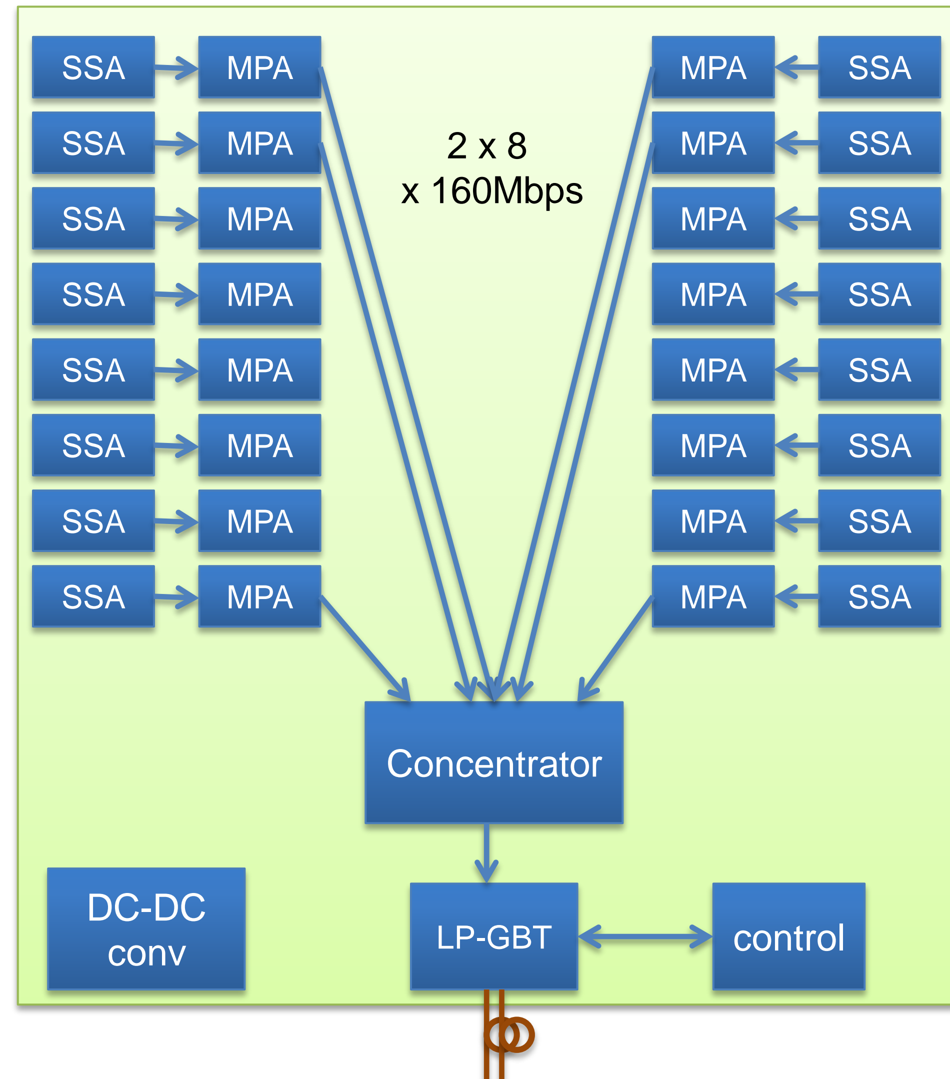
- *> 4 Centroids per row*
- *> 8 Centroids in total*



D. Ceresa, A. Marchioro, CERN

Module Readout Architecture

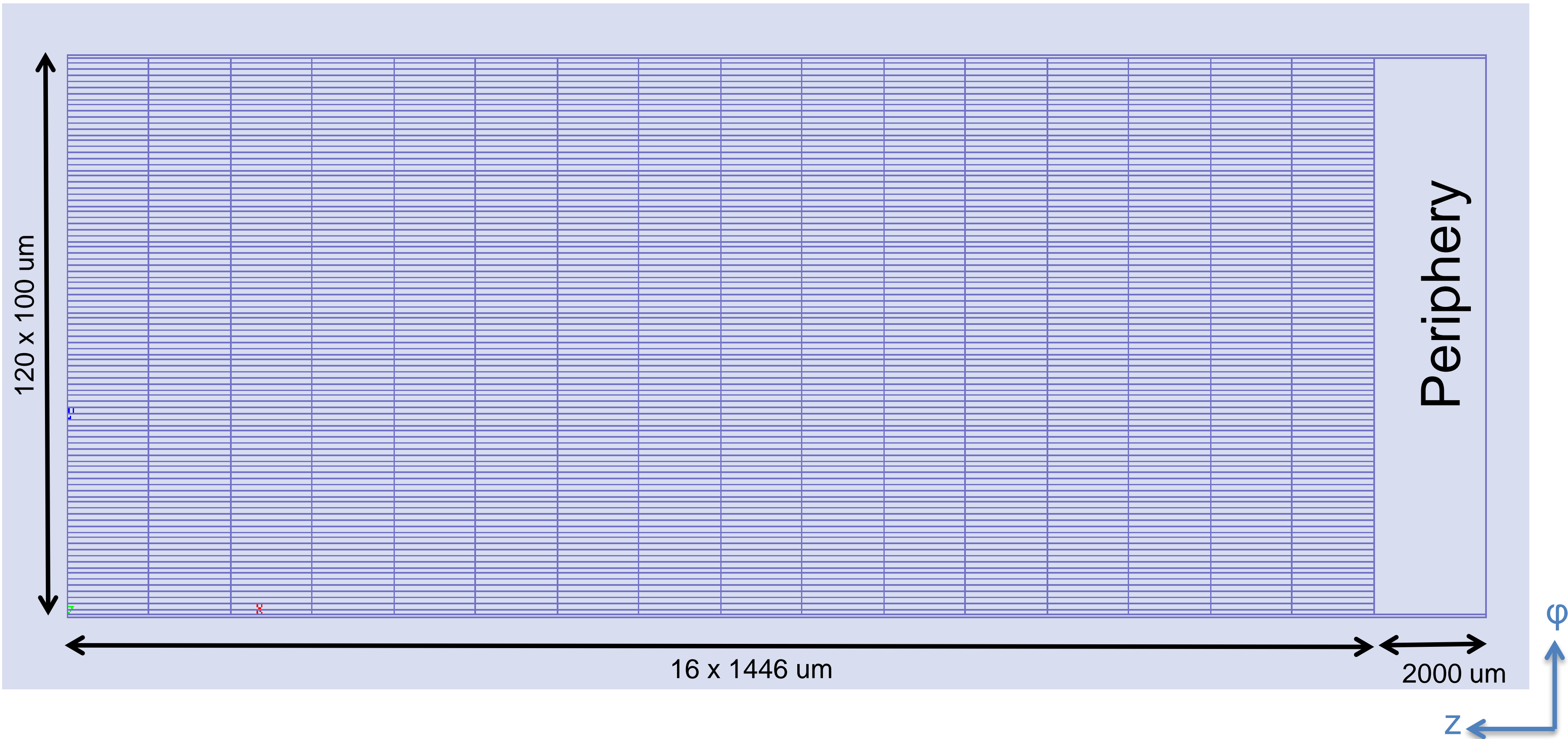
- Star bus readout
  - Low voltage differential signals
  - @ 160MBps
- Data Concentrator ASIC
  - Aggregates data from MPAs
  - Construct data packets
  - Transmit data via the LP-GBT
  - Handle channel bandwidth for Trigger & Readout data
    - Respecting a fixed trigger latency
    - Minimize readout event losse
  - 130nm or 65nm (low power) process
- LP-GBT
  - Low Power GigaBit Transceiver
  - 65nm (low power) process



MPA overall requirements

- Power per module for readout ASICs: 4 W
  - < 250 mW per MPA chip
  - < 1/3 into analog, i.e. 80 mW, or < 40 µW/pixel
- 65nm LP (Low Power) process (LP also means “slower”!)
- Analog FE circuitry:
  - 1.2V supply, < 30µA/channel (up to discriminator output, not including common biases overhead)
  - 22 ns pulse shaping S/N: > 20
- Digital logic :
  - 1.2V supply, possibly 0.85V for slow digital circuitry
  - Low power design techniques in clock distribution network
  - Development of special low leakage SRAM for readout FIFOs (outsourced IP block)
  - Development of CMOS IO pads using thin gate devices (outsourced IP block)

MPA Global Floorplan



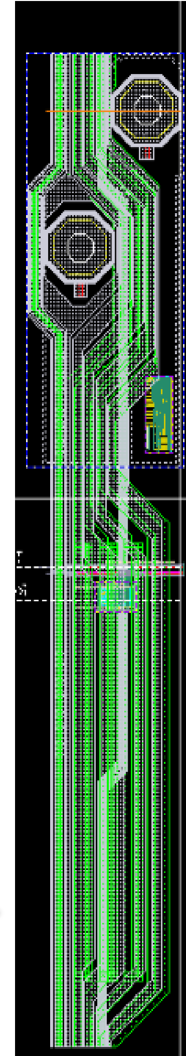
- 120 columns x 16 rows = 1,920 pixels

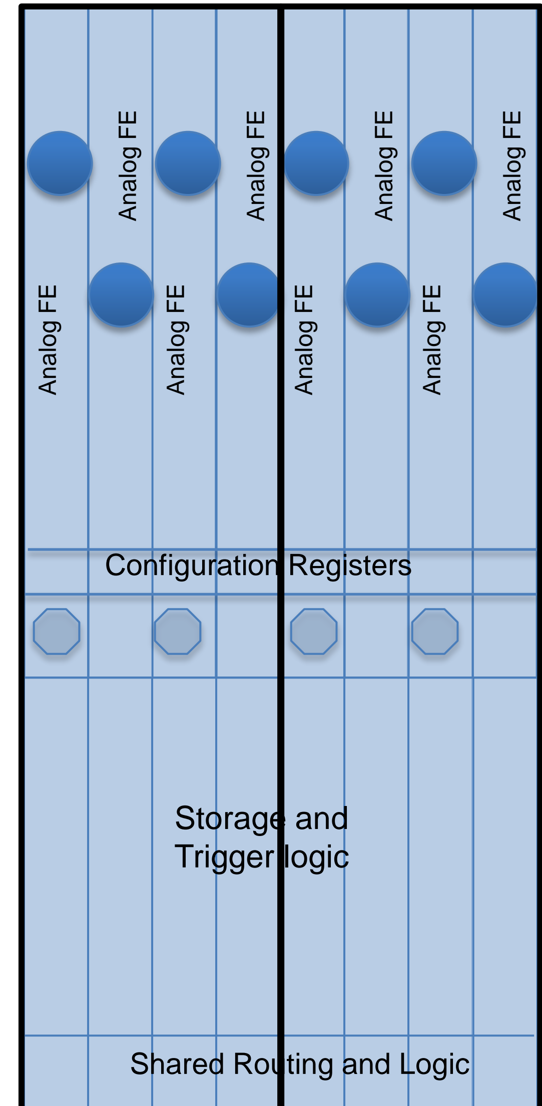
MPA Pixel Floorplan

- Pixel Floorplan providing a framework for:
  - detector shielding from electronic noise
  - routing power of critical analog blocks
  - routing long digital lines
  - enable possible usage of TSVs
- Decision for an 8 metal stack process

M1	m1	local	cell
M2	x	local	cell
M3	x	local	cell and block
M4	x	local	cell and block
M5	x	regional	cell and group and shield
M6	z	global	clk and pwr
M7	u	global	clk, pwr and shield
M8	RDL	global	pads and GND

- Example layout of top layers



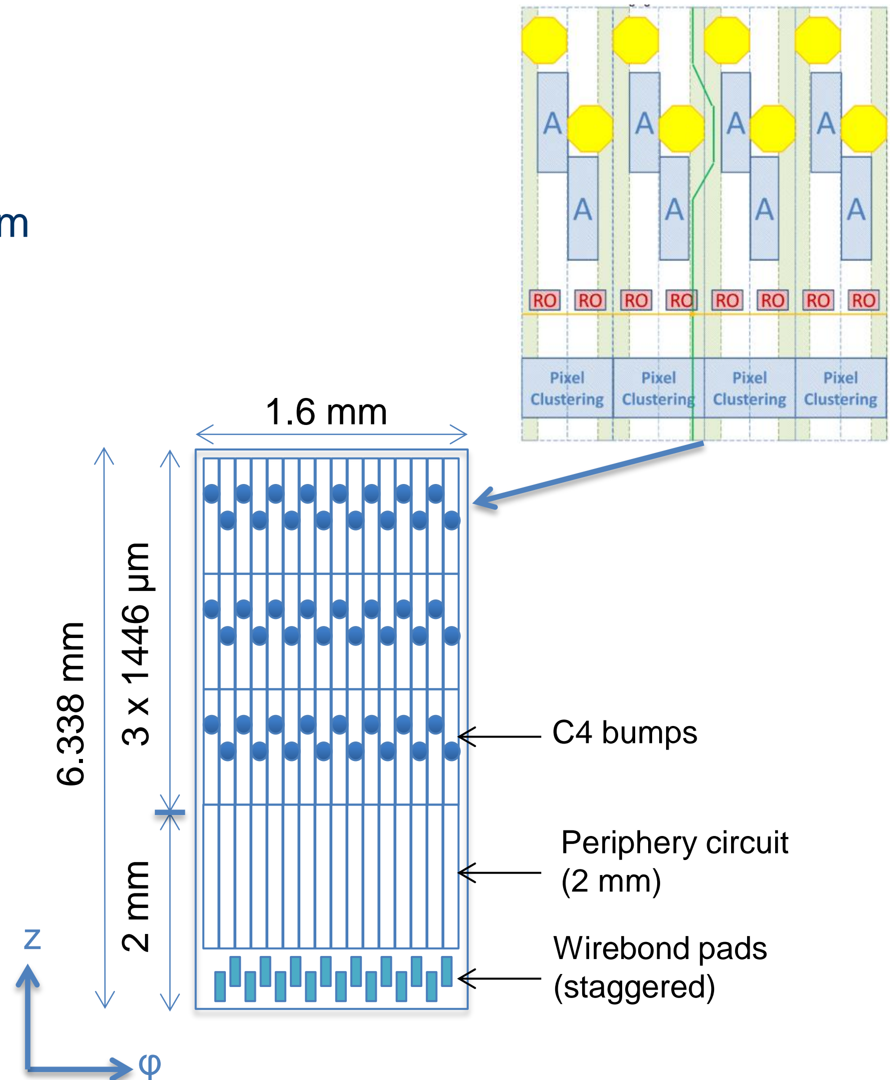


D. Ceresa, J. Kaplon, CERN

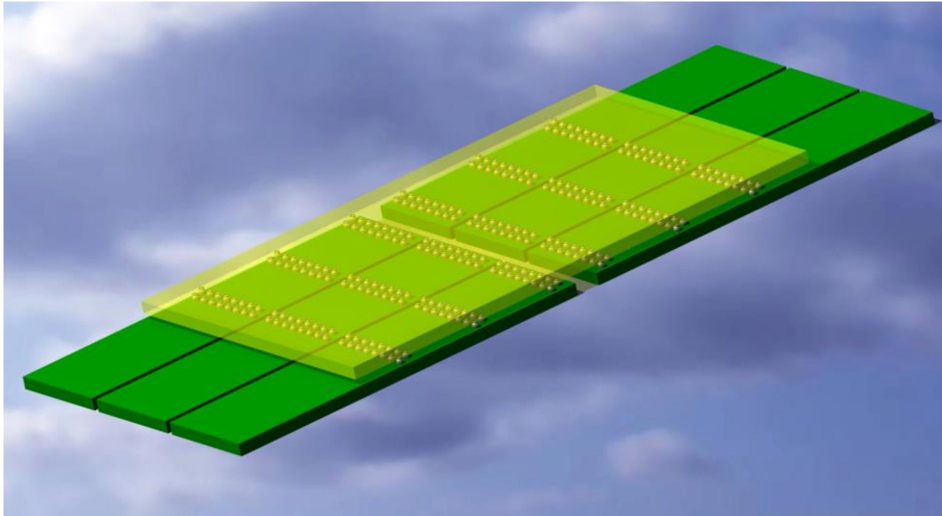
The MPA-light demonstrator

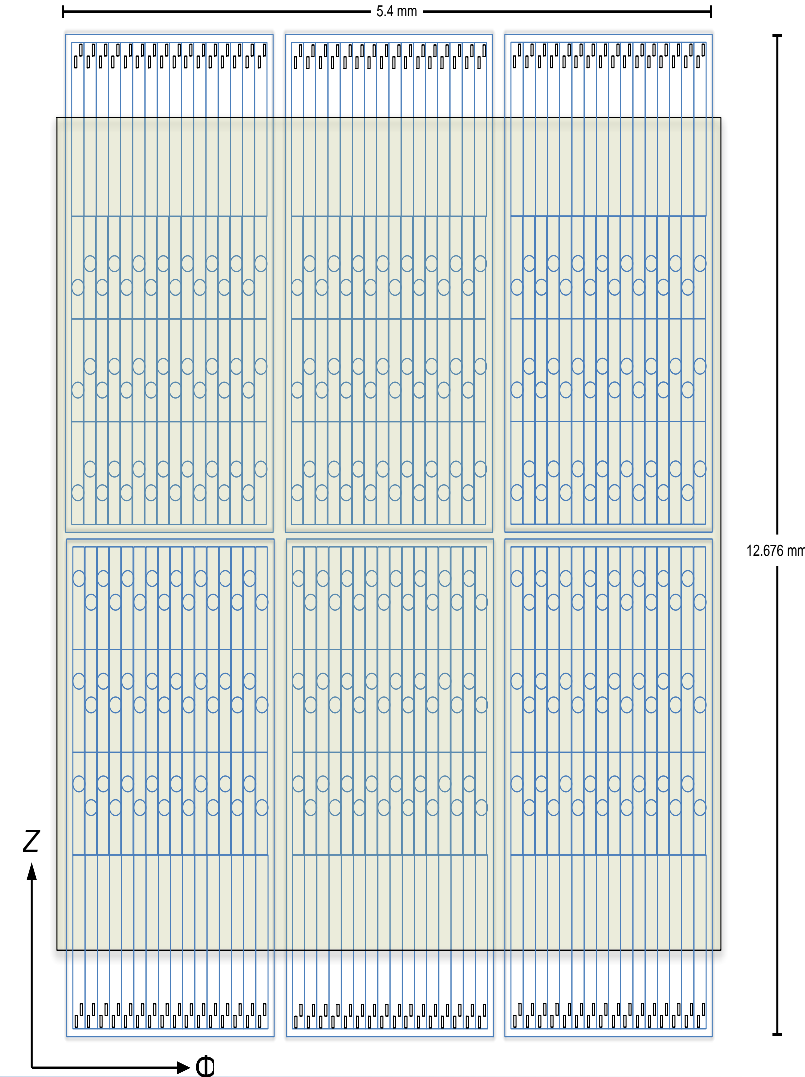
- A reduced size MPA design
  - 16 x 3 pixels (instead of 120 x 16)
  - Size of single pixel (as final): 100 x 1446 um
  - Bump-bond pad size: 90 mm
  - Pitch 200 mm horizontal, 300 mm vertical
  - Wirebond pads for hybrid connections
  - Pixel floorplanning similar to the final MPA
  - Scalable to the final design

- Purpose
  - Prototype & qualify the analog FE circuitry
  - Facilitate the development of the sensor
  - Understand and solve the numerous technical aspects of the Module Assembly



The MAPSA-light





- **MA**cro **P**ixel **S**ub **A**ssembly (MAPSA) light
- Objective is to assemble a module of 3 x 2 MPA-light chips for a total of 288 pixels
  - Bump-bondable to detector
  - Wire-bondable to hybrid
  - Floorplan allows for TSV experimentation

MPA-Light functionalities (baseline)

- Full analog chain as in final module
  - Preamp-shaper
  - Discriminator
  - DAC for threshold adjustment
  - DAC for global biasing
  - Calibration circuit
- Read-Out via single serial shift register per chip
- Capability of single-hit or multiple-hit-counter mode (16-bit) per pixel
- Configuration with serial shift register (16-bit/pixel)
- Simple trigger (OR of channels)
- No L1 buffer, no concentrator interface
- Separate analog and digital power domains
  - Analog 1.2 V
  - Digital: explore capability of decreasing supply voltage to 0.85 V
- Power & Clock Routing scheme as close as possible to the final MPA
- 65nm process on 8 metals, as in the final MPA

MPA-Light additional functionalities

- Additional functionalities focuses on the testing of the Stub Finding Logic (the logic needed to provide L1 trigger tracking information)
    - Pixel Row and Strip Clustering
    - Hits Encoder
    - Phi-Shift logic
  - Implement a “Strip-like” configuration mode for the pixels, thus emulating a strip sensor layer
  - Implement interconnect bus between MPA-light chips transmitting hits at 160MHz from the “Strip-like” layer to the pixel layer electronics
  - Implement Coincidence and Stub Sorting logic

MPA-Light Block Diagram

MPA light CHIP

Analog Pixel circuitry

Optional

Pixel Clustering

Analog Pixel circuitry

Optional

Pixel Clustering

Analog Pixel circuitry

Optional

Pixel Clustering

CLK40

Optional

Optional

HITS OR

Clk Divider 160->40

Stub Logic

Stub Reg

Column OR

Analog I/O

ConfDin ConfCLKin

RODin ROCLKin

HIT

CLK 160

VDDD

GNDD

VDDA

GNDA

Strip IN/OUT

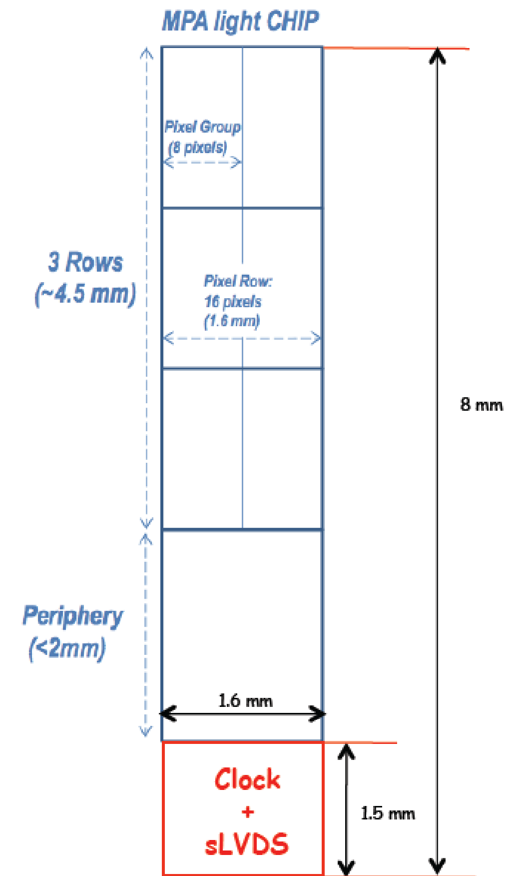
Strip Flag

Shutter

ConfDout ConfCLKo

RODout ROCLKout

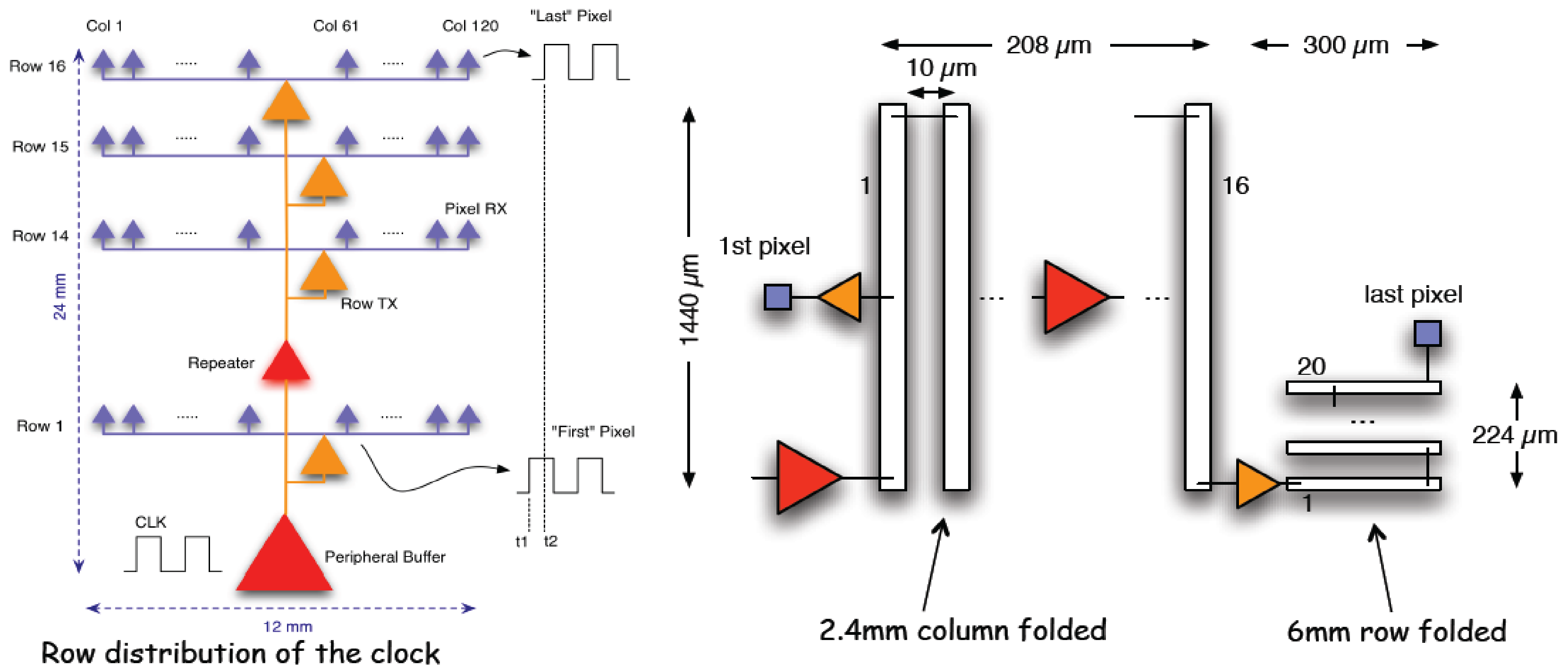
MPW run prototype



Kostas.Kloukinas@cern.ch

Test structures for MPA-Light submission

1. Drivers and receivers sLVDS-CMOS (320Mbps and 640Mbps, 0.8 and 1.2V bias voltage)
2. Test structure to simulate the propagation delay, skew and power consumption of the row distribution of the clock



Row distribution of the clock

V. Re, G. Traversi, L. Gaioni, F. De Canio – U. Pavia and INFN Bergamo

Conclusions & Future Plans

- Promising concept of Pixel-Strip module with local p_T discrimination
- Choice of technologies is driven by the optimization of the tracker performance
  - Low Power ASIC technology combined with system level Low Power techniques
  - Lightweight module assembly, avoiding the use of thick interposers
  - Use of commercial technologies compatible with large volume production having the perspective of high yield at an affordable cost
  - R&D on TSVs is an important element for the performance of the final design
- MPA-light prototyping scheduled for end of Q3 2014
- MAPSA-light prototyping targeted for the end of Q4 2014
- Results will pave the way towards the final PS module design (2016-17)

Acknowledgements:
Most of the ideas and the work by A. Marchioro

sLVS Differential IO pads

- Development of *scalable Low Voltage Signaling (sLVS) differential* IO pads for PS module ASIC interconnections:
  - SSA to MPA
  - MPA to Concentrator
- Different loads:
  - 300 fF (SSA outputs)
  - 10 pF (MPA outputs)
  - 2.5cm, 6cm, 10.5cm long transmission line on the thin hybrid toward the concentrator
- Low-power consumption design: 15mW
  - 12 differential lines at 320 Mbps (1.25mW per link, i.e. TX/RX)
  - 6 differential lines at 640 Mbps (2.5mW per link, i.e. TX/RX)
- Power supply: 1.2V (nominal)
  - Work in progress targeting 0.85 V

V. Re, G. Traversi, L. Gaioni, F. De Canio – U. Pavia and INFN Bergamo