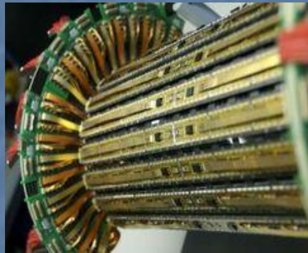
ATLAS–CMS-LCD **RD53** collaboration:

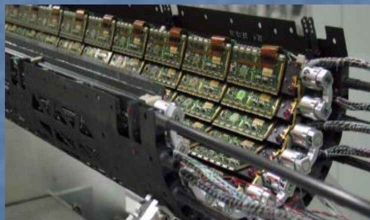
Pixel readout integrated circuits for extreme rate and radiation

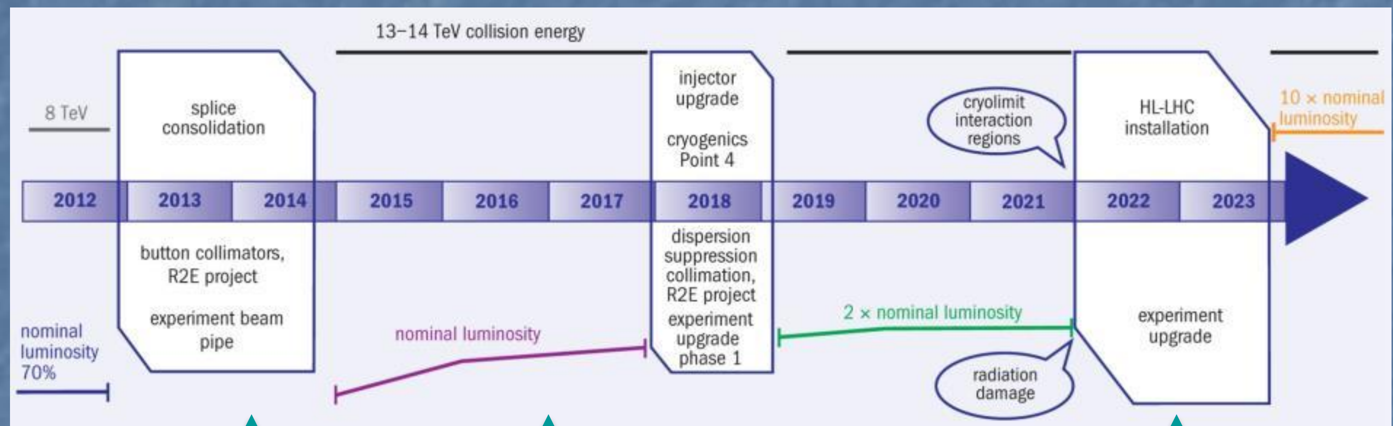
Jorgen Christiansen on behalf of RD53

LHC Pixel upgrades

- Current LHC pixel detectors have clearly demonstrated the feasibility and power of pixel detectors for tracking in high rate environments
- Phase0/1 upgrades: Additional pixel layer, ~4 x hit rates
  - ATLAS: Addition of Inner B Layer (IBL) with new 130nm pixel ASIC (FEI4)
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG)
- **Phase2 upgrades**: ~16 x hit rates, ~4 x better resolution, 10 x trigger rates, 16 x radiation tolerance, Increased forward coverage, less material, , ,
  - Installation: ~ 2022
  - Relies fully on significantly improved performance from next generation pixel chips.







ATLAS Pixel IBL

CMS Pixel phase1

CMS & ATLAS phase 2 pixel upgrades

100MHz/cm^2

400MHz/cm^2

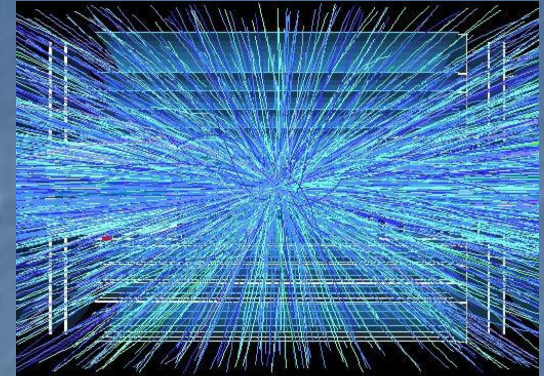
1-2GHz/cm^2

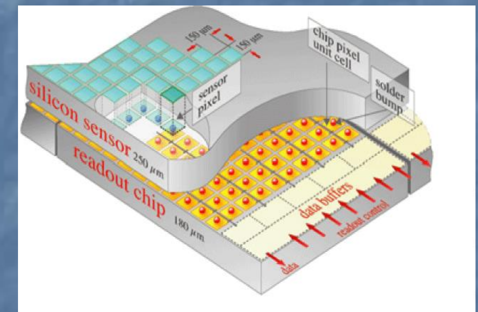
Phase 2 pixel challenges

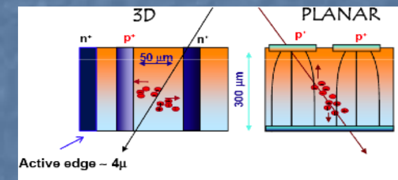
- ATLAS and CMS phase 2 pixel upgrades very challenging
  - Very high particle rates: 500MHz/cm^2
    - Hit rates: 1-2 GHz/cm^2 (factor ~16 higher than current pixel detectors)
  - Smaller pixels: ~¼ (~50x50um^2 or 25x100um^2)
    - Increased resolution
    - Improved two track separation (jets)
    - Outer layers can be larger pixels, using same pixel chip
  - Participation in first/second level trigger ? (no)
    A. 40MHz extracted clusters (outer layers) ?
    B. Region of interest readout for second level trigger ?
  - Increased readout rates: 100kHz -> ~1MHz
    - Data rate: 10x trigger X >10x hit rate **= >100x !**
  - Low mass -> Low power

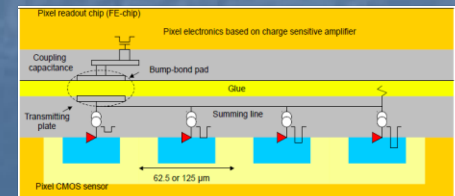
  Very similar requirements (and uncertainties) for ATLAS & CMS
- Unprecedented hostile radiation: ~1Grad, ~10^{16} Neu/cm^2
  - Hybrid pixel detector with separate readout chip and sensor.
    - Monolithic seems unfeasible for this very high rate hostile radiation environment
  - Phase2 pixel will get in 1 year what we now get in 10 years

  (10.000 x more radiation than space/mil !)
- Pixel sensor(s) not yet determined
  - Planar, 3D, Diamond, HV CMOS, , ,
  - Possibility of using different sensors in different layers
  - Final sensor decision may come relatively late.
- Complex, high rate and radiation hard pixel chips required









ATLAS HVCMOS program

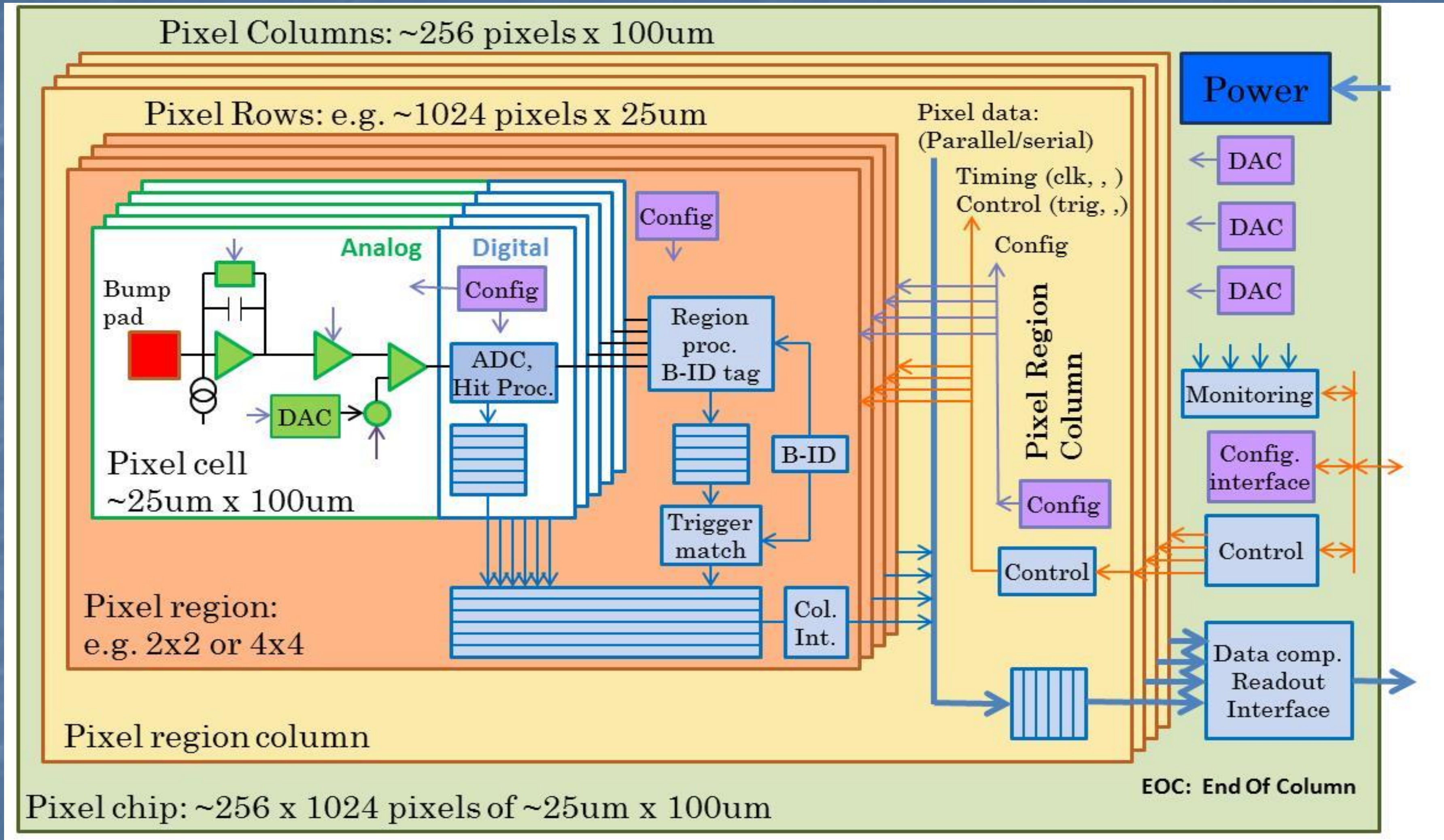
Pixel chip

- Pixel readout chips critical to be ready for phase 2 upgrades
  - Technology: Radiation qualification
  - Building blocks: Design, prototyping and test
  - Architecture definition/optimization/verification
  - Chip prototyping, iterations, test, qualification and production
  - System integration
    - System integration tests and test-beams
  - Production and final system integration, test and commissioning
- Phase 2 pixel chip very challenging
  - Radiation
  - Reliability: Several storage nodes will have SEUs every second per chip.
  - High rates
  - Mixed signal with very tight integration of analog and digital
  - Complex: ~256k channel DAQ system on a single chip
  - Large chip: >2cm x 2cm, ½ - 1 Billion transistors.
  - Very low power: Low power design and on chip power conversion
- ATLAS and CMS have evolved to similar pixel chip architectures and plans to use same technology (65nm) for its implementation.
- Experienced chip designers for complex mixed signal ICs in modern technologies that must work in a extremely harsh radiation environment is a scarce and distributed "resource" in HEP.

Pixel chip generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2: HL-LHC
Pixel size	100x150um^2 (CMS) 50x400um^2 (ATLAS)	100x150um^2 (CMS) 50x250um^2 (ATLAS)	**~ 50x50um^2**
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, HVCMOS ?
Chip size	7.5x10.5mm^2 (ATLAS) 8x10mm^2 (CMS)	20x20mm^2 (ATLAS) 8x10mm^2 (CMS)	**> 20 x 20 mm^2**
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	**~1G**
Hit rate	**100MHz/cm^2**	**400MHz/cm^2**	**1-2 GHz/cm^2**
Trigger rate	100kHz	100KHz	200kHz - **1MHz**
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	6 - **20us**
Hit memory per chip	0.1Mb	1Mb	~16Mb **(160x)**
Readout rate	40Mb/s	320Mb/s	**1-4Gb/s (100x)**
Radiation	**100Mrad**	**200Mrad**	**1Grad**
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	**65nm**
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	**Digital**
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	**In Pixel buffering**
Power	~1/4 W/cm^2	~1/4 W/cm^2	**1/2 - 1 W/cm^2**

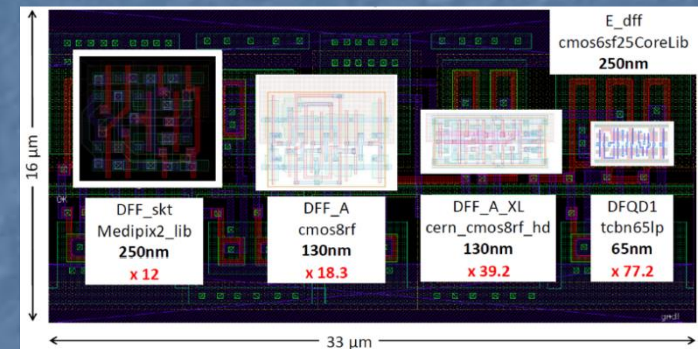
3rd generation pixel architecture



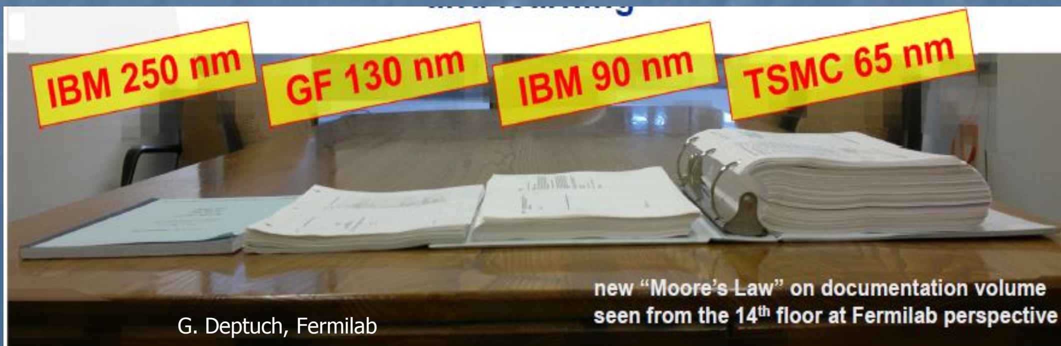
- 95% digital (as FEI4)
- Charge digitization (TOT or ADC)
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column
- Chip size: >20 x 20 mm^2

Technology: Why 65

- Mature technology:
  - Available since ~2007
- High density and low power
  - High density vital for smaller pixels and ~100x increased buffering during trigger latency
  - Low power tech critical to maintain acceptable power for higher pixel density and much higher data rates
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Access: CERN frame-contract with TSMC and IMEC
  - Design tool set, Shared MPW runs, Libraries, Design exchange within HEP community
- Affordable (MPW from foundry and Europractice, ~1M NRE for final chips)
- Significantly increased density, speed, , , and complexity compared to 130nm !



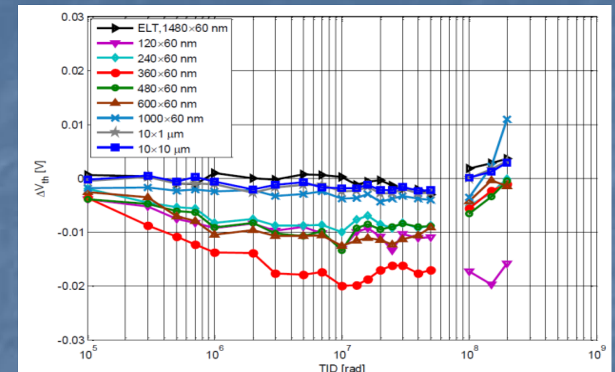
X. Llopart CERN



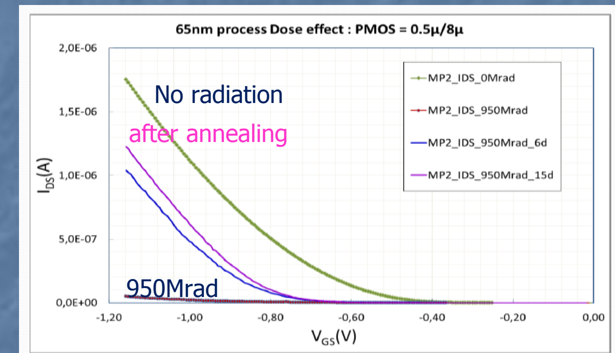
G. Deptuch, Fermilab

65nm Technology

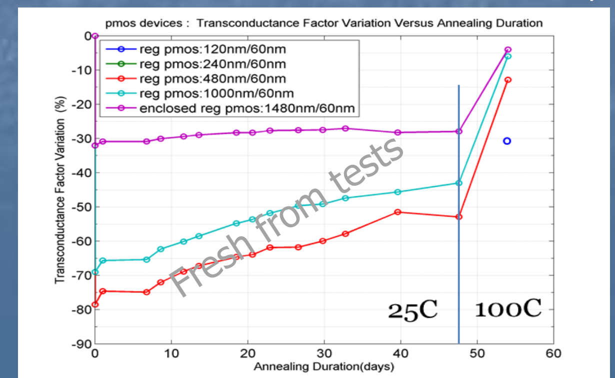
- Radiation hardness
  - Uses thin gate oxide
    - Radiation induced trapped charges removed by tunneling
    - More modern technologies use thick High K gate "oxide" with reduced tunneling/leakage ?.
  - Verified for up to 200Mrad
  - To be confirmed for 1Grad
    - PMOS transistor drive degradation, V_t shift, Annealing ?
  - CMOS normally not affect by NIEL
    - To be confirmed for 10^{16} Neu/cm^2
    - Certain circuits using "parasitic" bipolars to be redesigned ?
  - SEU tolerance to be built in (as in 130 and 250nm)
    - SEU cross-section reduced with size of storage element, but we will put a lot more per chip
  - All circuits must be designed for radiation environment (e.g. Modified SRAM)
- Annealing scenario critical
  - Detectors will run cold (~-20°C)
  - Yearly annealing periods ? (room temp or higher ?)
- If unacceptable degradation then other technologies (alternative foundries, 40nm, etc.) must be evaluated and/or a replacement strategy must be applied for inner pixel layers.



S. Bonacini, P. Valerio CERN



M. Menouni, CPPM



ATLAS – CMS RD collaboration

- Similar/identical requirements, same technology choice and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS – ATLAS RD collaboration
  - Even if we do not make a final common pixel chip
- Forming a RD collaboration has attracted additional groups and collaborators
  - Synergy with CLIC pixel (and others): Technology, Rad tol, Tools, etc.
- RD53 collaboration recommended by LHCC June 2013
  - Institutes: 17 (+ 3 new applicants)
    - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, RAL, UC Santa Cruz.
    - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino.
  - Collaborators: ~100, ~50% chip designers
  - Collaboration organized by Institute Board (IB) with technical work done in specialized Working Groups (WG)
  - Initial work program covers ~3 years to make foundation for final pixel chips
  - Co-spokes persons: ATLAS: M. Garcia-Sciveres, LBNL. CMS: J. Christiansen, CERN
- RD53 web (new): www.cern.ch/RD53/

Working groups

WG	Domain
WG1	Radiation test/qualification: M. Barbero, CPPM
	Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm
WG2	Top level: (M. Garcia-sciveres, LBNL)
	Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.
WG3	Simulation/verification framework: T. Hemperek, Bonn
	System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells
WG4	I/O : To be started
	Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.
WG5	Analog design / analog front-end: V. Re, Bergamo/Pavia
	Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends
WG6	IP blocks: (J. Christiansen, CERN)
	Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation

Status and plans

- General
  - MOU in the pipeline
  - Some institutes have obtained funding thanks to RD53 (justified by the fact that it is for ATLAS & CMS)
  - WGs have regular meetings
  - Next collaboration workshop: April 10-11 at CERN
  - Define schedule for shared IC runs, **Full pixel chip demonstrator: 2016**
- Radiation: **Urgent**
  - **Verify that 65nm is OK,** Evaluate alternatives (2014)
  - Radiation test campaigns have started
  - Simulation models after radiation (2015)
- Analog
  - Defining requirements
  - Defined alternative schemes to be evaluated: TOT, ADC, Auto-zero, Sync – Async, etc.
  - Design/test different implementations and choose (2015)
- IPs: ~30 IP block
  - Defined who makes what.
  - Define detailed specs, how to make/deliver IPs, start design (2014)
  - IP library with layouts, simulation models, documentation, , , , (end 2015)
- Simulation:
  - Defining simulation tool (SV + UVM), bench mark, Framework definition
  - Simulate different architectures and optimize
  - SEU immunity verification
- Top: How to put such a chip together
  - Global aspects: Metal stack, Mixed signal, Power dist, Global integration, Bump-bonding pattern, ,
- IO: To be started

RD53 Summary

- Highly focused ATLAS-CMS-LCD/CLIC RD collaboration to develop/qualify technology, tools, architecture and building blocks required to build next generation pixel chips for very high rates and radiation
- Synergy with other pixel projects when possible
- Centered on technical working groups
- Baseline technology: 65nm
  - CERN frame contract/NDA/design kit .
  - Will evaluate alternatives ("emergency" plan)
- 17 Institutes, 100 Collaborators
- Initial work program of 3 years
  - Goal: Full pixel chip prototype 2016
  - Working groups have gotten a good start.
  - Common or differentiated final chips to be defined at end of 3 year R&D period

Backup slides

RD53 Outlook

- 2014:
  - Release of CERN 65nm design kit: Very soon !
  - Detailed understanding of radiation effects in 65nm
    - Radiation test of few alternative technologies.
    - Spice models of transistors after radiation/annealing
  - IP block responsibilities defined and appearance of first FE and IP designs/prototypes
  - Simulation framework with realistic hit generation and auto-verification.
  - Alternative architectures defined and efforts to simulate and compare these defined
  - Common MPW submission 1: First versions of IP blocks and analog FEs
- 2015:
  - Common MPW submission 2: Near final versions of IP blocks and FEs.
  - Final versions of IP blocks and FEs: Tested prototypes, documentation, simulation, etc.
  - IO interface of pixel chip defined in detail
  - Global architecture defined and extensively simulated
  - Common MPW submission 3: Final IPs and Fes, Small pixel array(s)
- 2016:
  - Common **engineering run**: Full sized pixel array chip.
  - Pixel chip tests, radiation tests, beam tests , ,
- 2017:
  - Separate or common ATLAS – CMS final pixel chip submissions.

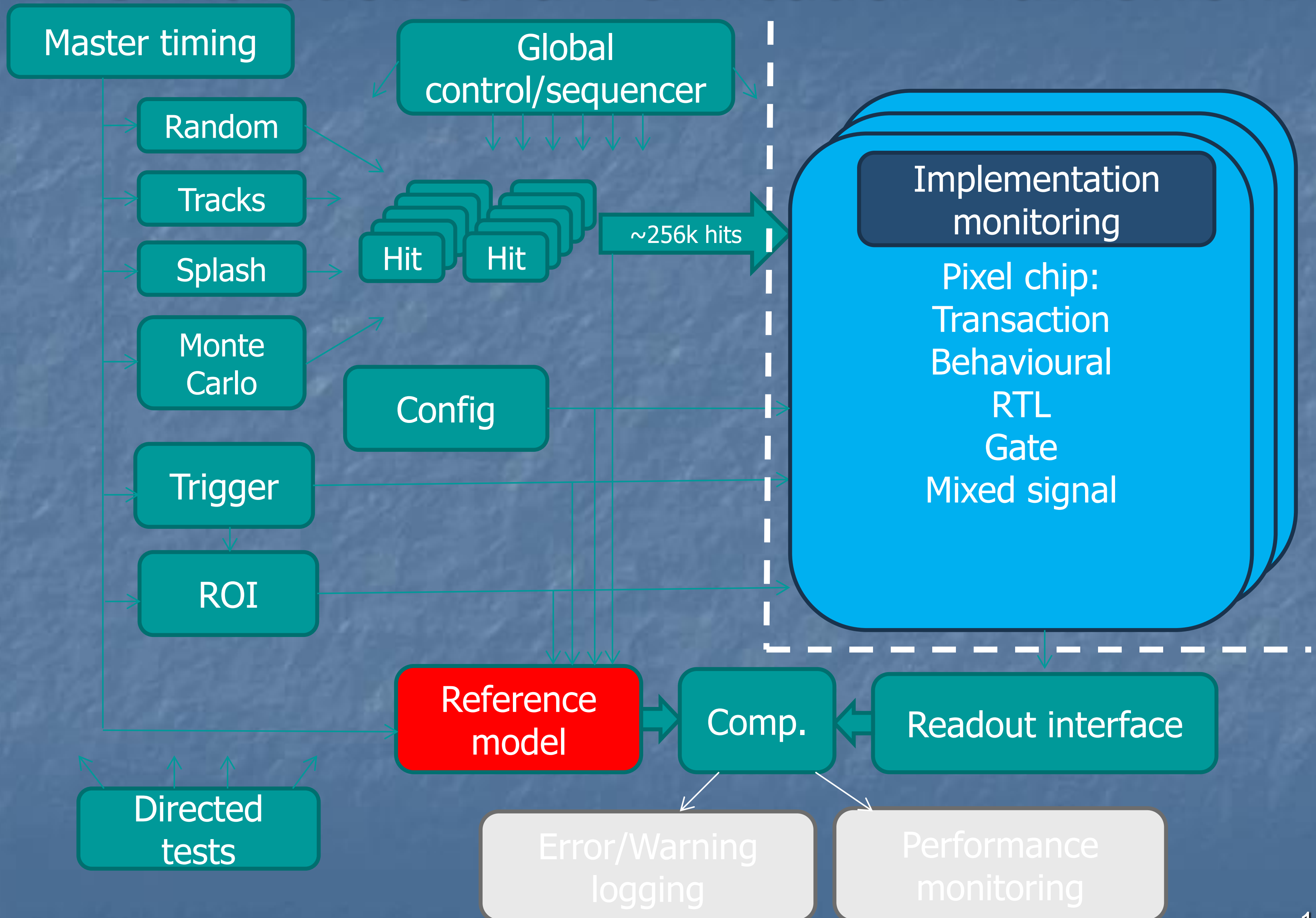
Participation matrix

Institute	WG1 Radiation	WG2 Top level	WG3 Sim./Ver	WG4 I/O	WG5 Analog	WG6 IPs
Bari	C		A			A
Bergamo-Pavia	A			C	A	B
Bonn	C	A	A	B	B	A
CERN	B(*)	(*)	A	C(*)	A	B(*)
CPPM	A	B	C	C	B	A
Fermilab	A	B			A	
LBNL	B	A	B	B	A	A
LPNHE Paris	A	B	A			A
NIKHEF		A	A			A
New Mexico	A					
Padova	A					A
Perugia	B		A			B
Pisa		B	A	A		A
PSI	B	A		C	A	A
RAL		B	B		A	C
Torino	C	B	C	B	A	A
UCSC	C	B	C			A

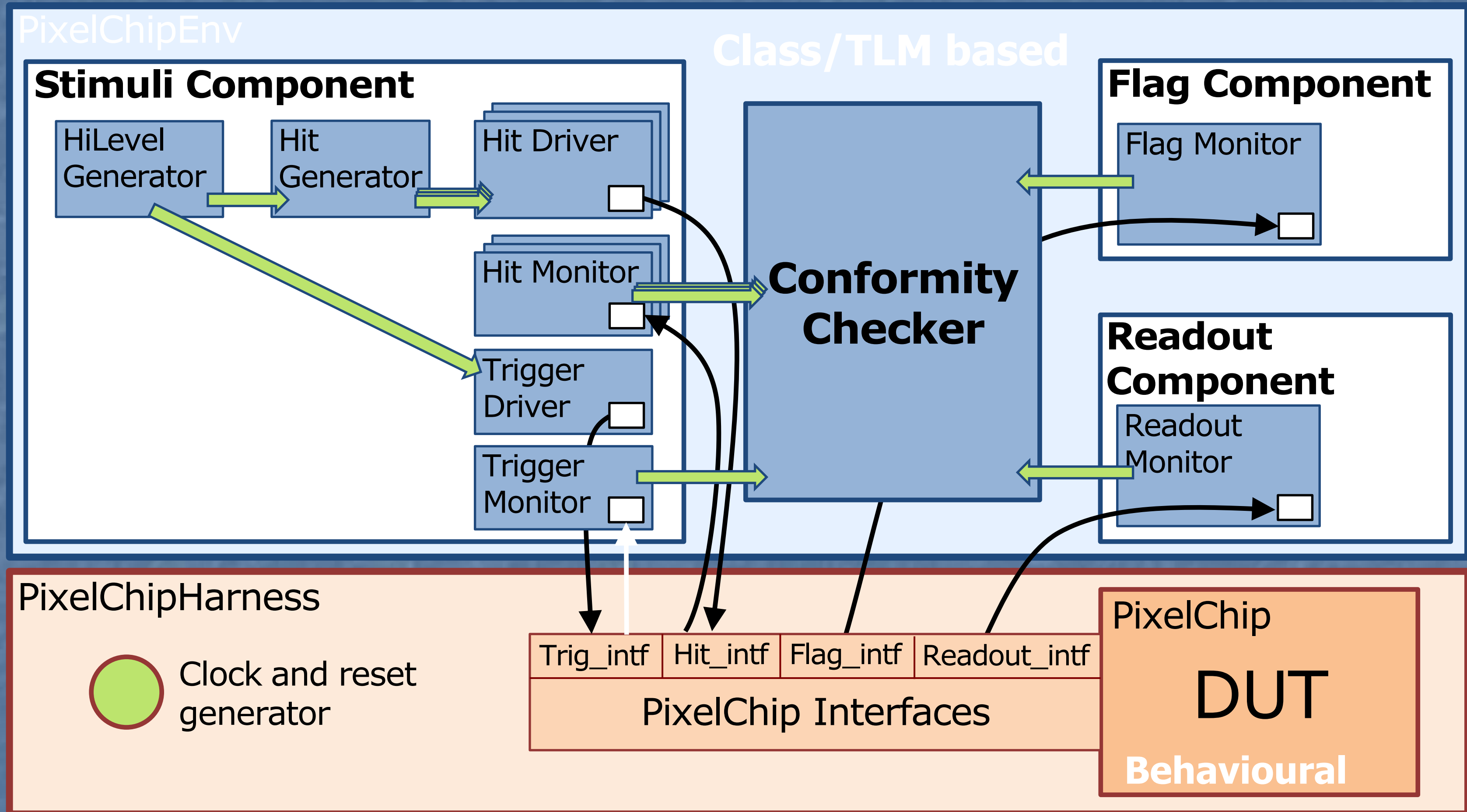
A: Core competency, B: High interest, C: Ability to help

(*): General CERN support for 65nm

Simulation and Verification framework



SV+UVM framework

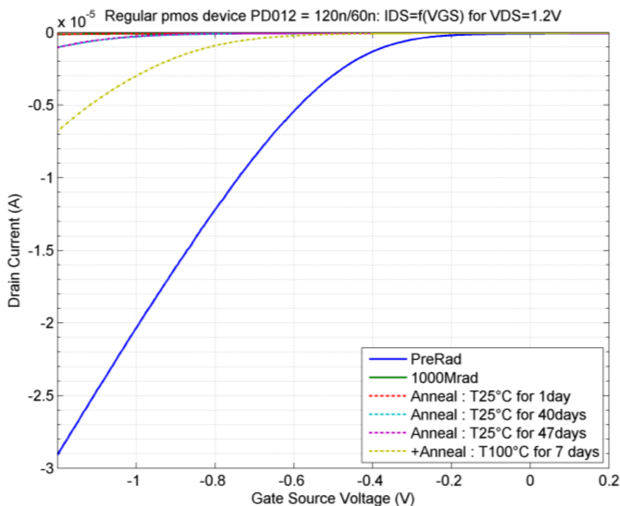


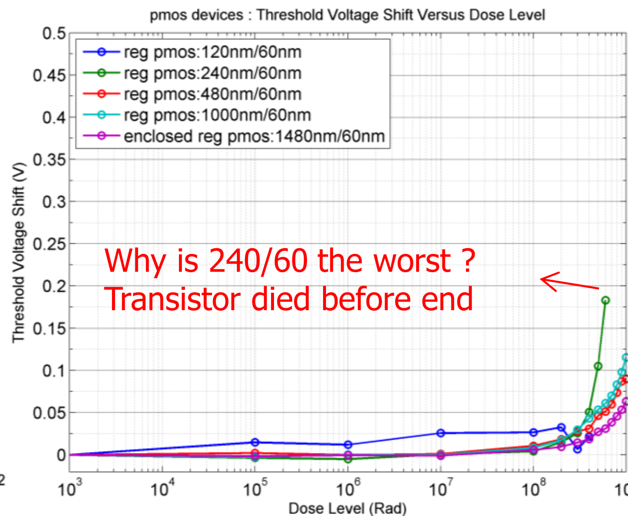
E. Conti

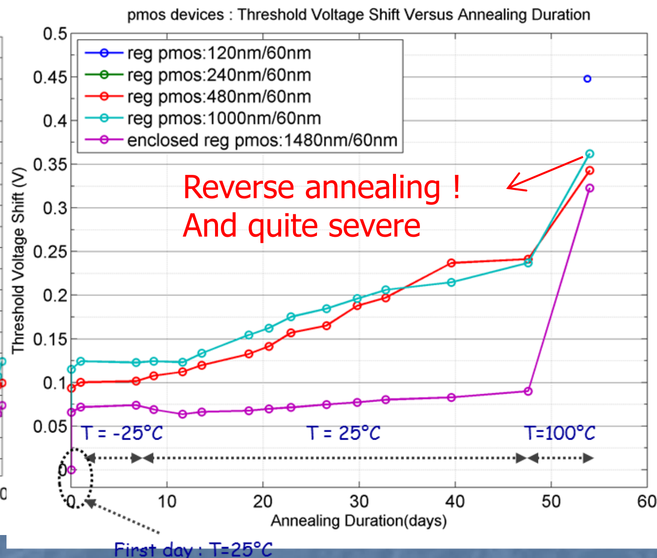
IP blocks

Country	DE		FR	NL	IT - INFN						US	FR	UK	US	CZ	Comments		
Group	Bonn	CERN	CPPM	NIKHEF	Bari	Pav/ Berg	(Milano)	Padova	Pisa	Torino	LBNL	LPNHE	RAL	Santa Cruz	(Prague)			
ANALOG: Coordination with analog WG																		
Temperature sensor.			O			(P)				(P)					(P)			
Radiation sensor			(P)			(P)				O ?					(P)			
HV leakage current sensor.			O							(P)					(P)			
Band gap reference		O	O	(P)		O							(P)			3 Groups		
Self-biased Rail to Rail analog buffer	(P)		(P)	(P)									O		(P)			
MIXED																		
8 – 12 bit biasing DAC		(P)			O										(P)			
10 - 12 bit slow ADC for monitoring		O	O		O											3 Groups		
PLL for clock multiplication	O	(P)		(P)				(P)	(P)	(P)			(P)	(P)		Together		
High speed serializer (~Gbit/s)	O	(P)		(P)					(P)				(P)	(P)				
(Voltage controlled Oscillator)				(P)				O	(P)	(P)						Needed ?		
Clock recovery and jiter filter	O	(P)							(P)				(P)					
Programmable delay	O	(P)							(P)				(P)					
DIGITAL																		
SRAM for pixel region	(P)	(P)					O							(P)				
SRAM/FIFO for EOC.	(P)	(P)					(P)		(P)					O				
EPROM/EFUSE	(P)	O	(P)															
DICE storage cell / config reg	(P)		O				(P)		(P)					(P)		Or TMR ?		
LP Clock driver/receiver	(P)					O							(P)					
(Dedicated rad hard digital library)	(P)	(P)	(P)						O			(P)	(P)			If needed		
(compact mini digital library for pixels)	(P)	(P)	(P)						O			(P)	(P)			If needed		
IO: Coordination with IO WG																		
Basic IO cells for radiation	(P)	O																
Low speed SLVS driver (<100MHz)	(P)	(P)				O			(P)	(P)					(P)			
High speed SLVS driver (~1Gbits/s)	(P)	(P)				O			(P)	(P)					(P)	Together		
SLVS receiver	(P)	(P)				O			(P)						(P)			
1Gbits/s drv/rec cable equalizer																New		
C4 and wire bond pads	(P)	O																
(IO pad for TSV)	O		(P)									(P)		(P)				
Analog Rail to Rail output buffer	O		(P)									(P)		(P)				
Analog input pad	O											(P)						
POWER																		
LDO(s)		(P)	(P)	O					(P)	(P)			(P)					
Switched capacitor DC/DC		(P)									O				(P)			
Shunt regulator for serial powering				O														
Power-on reset																New		
Power pads with appropriate ESD	(P)	O																
SOFT IP: Coordination with IO WG																		
Control and command interface		(P)			(P)				O			(P)						
Readout interface (E-link ?)		(P)			(P)				O			(P)						
Summary																		
ATLAS/CMS/Neutral	A	N	A	A	C	C	C	C	C	C	A	A	N	A	A	ATLAS	CMS	Neutral
O's	7	6	5	2	2	5	1	1	4	1	1		1	1		16	14	7
(P)'s	14	16	8	5	2	2	2	1	10	7		7	9	6	9	49	24	25

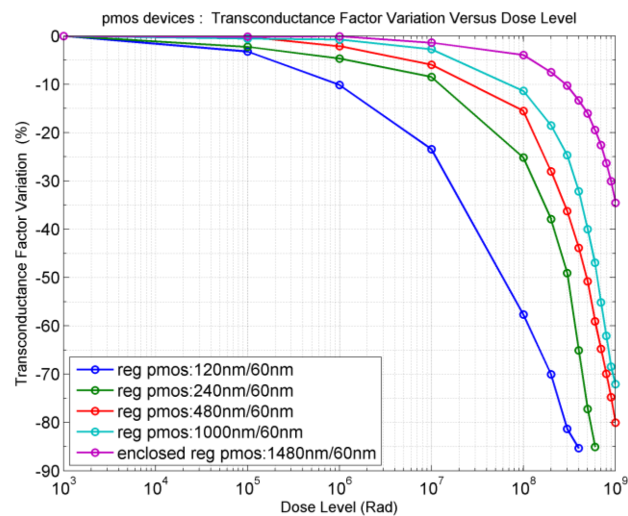
PMOS

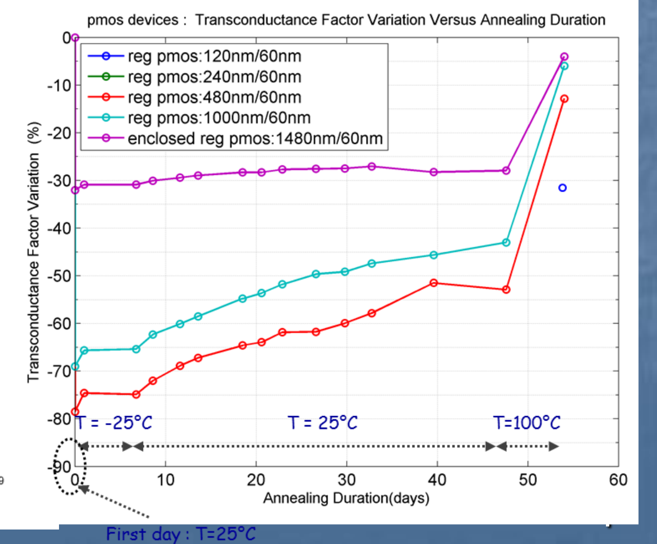




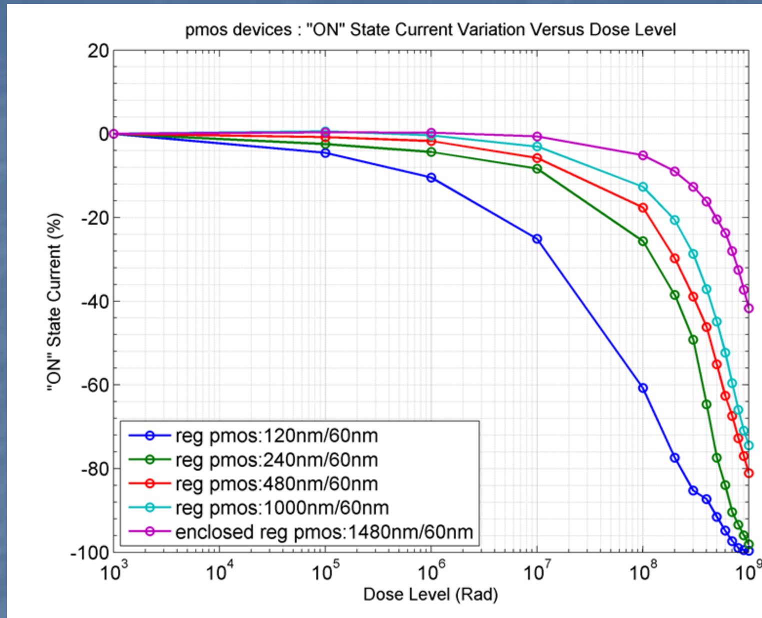


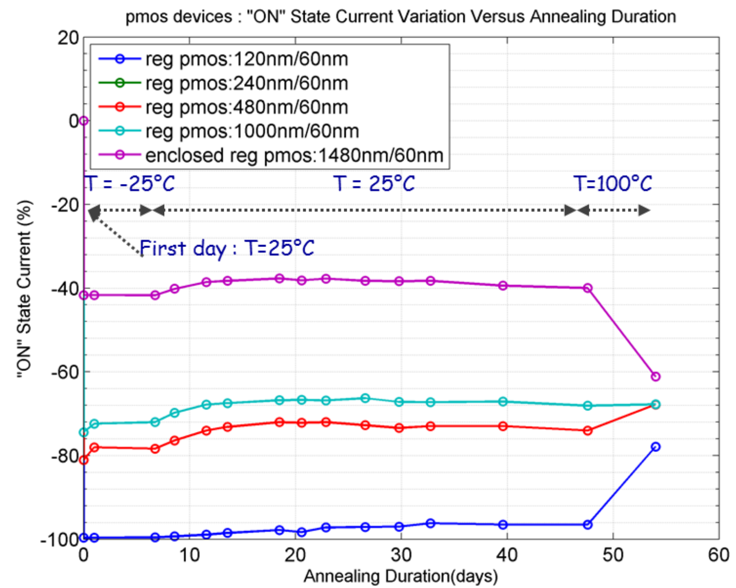
M. Menouni, CPPM



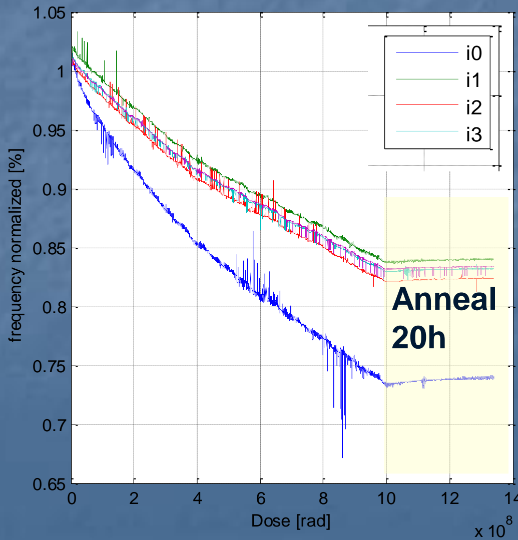


PMOS drive current (Digital)





M. Menouni, CPPM



Ring oscillator frequency with different transistor sizes and cold (-25 °C)

S, Bonacini, CERN

#	Wp	Wn	M
Ring 0	260	195	1
Ring 1	520	390	1
Ring 2	520	390	2
Ring 3	520	390	3

Acceptable for digital circuits ?
(Yes but ---)
Analog performance ?

Various interests in analog blocks

INFN (BG/PV, Torino, Padova): continuous-time front-end (PA and shaper), sybchronous comparator, ToT-based ADC, signal injection and calibration

Bonn (Prague): continuous and switched amplifier, static and dynamic comparator, SAR ADC

CERN: CLIC-PIX (ToT-based analog channel)

CPPM: high-resolution ADC (8 bits), adaptation of MAPS front-end

FNAL: Synchronous front-end, FLASH ADC (130 nm)

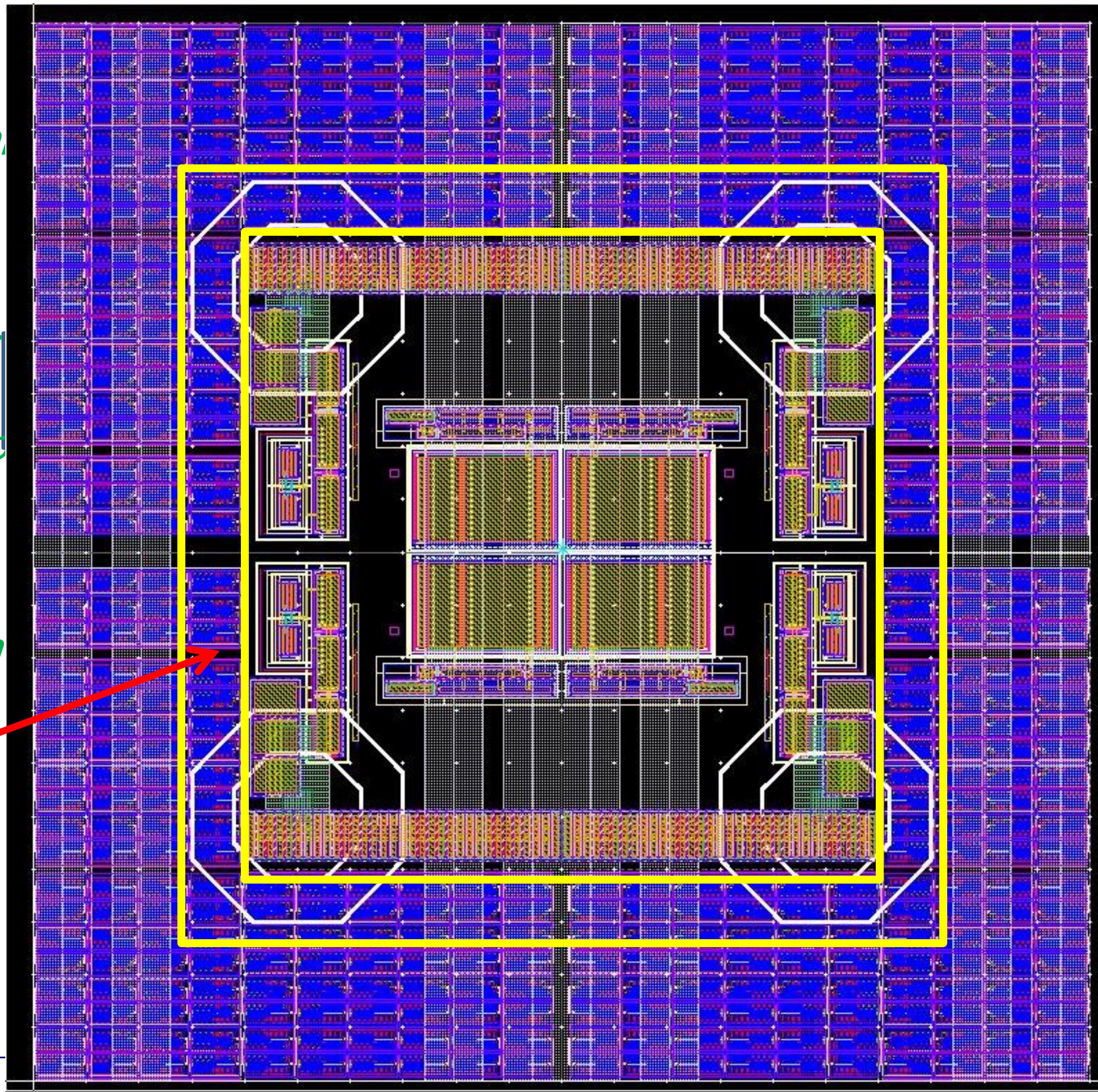
LBNL: ToT-based channel (6-7 bits resolution)

A 2X2 Unit

- Is this a digital uni
- FEI4 Bump pitch
- ~16000 Transistors
- ~32000 transistor p FEI4 equivalent-region (analog hole included)
- "Pixels" communica horizontally and
- vertically

Quiet logic Area

- Work in progress



A. Mekkaoui, LBNL

A 4X4 “Un