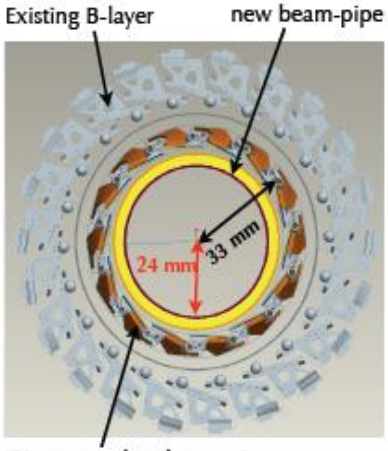
ATLAS Pixel Upgrade Phase 0 (IBL)

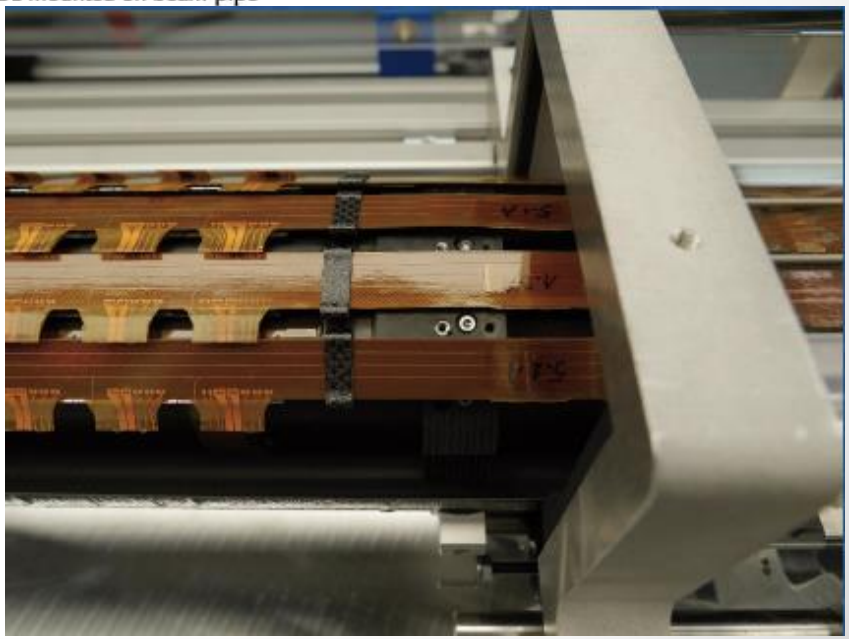
ACES Workshop 2014
18.-20.03.2014, CERN

T. Flick
University Wuppertal
for the IBL collaboration

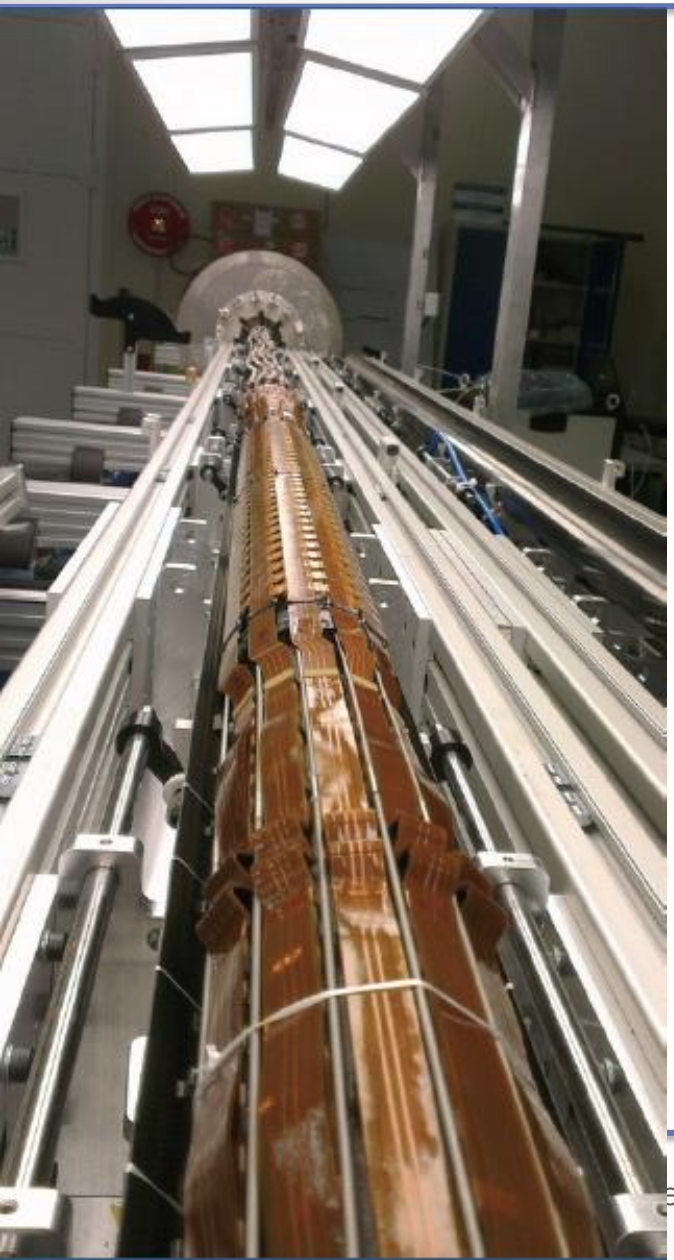
ATLAS Phase 0 Upgrade: Insertable B-Layer

- For phase 0 upgrade in ATLAS a 4th pixel layer around smaller beam pipe (ID 48 mm) will be added inside the existing 3 layers
- 14 new module carriers (staves) are being installed during these weeks.
- 32 newly designed front-end chips (FE-I4) per stave.
- New cooling system (CO_2-based) and new readout system have been developed.
- Integration of the IBL stave directly on the beam pipe to be installed together.





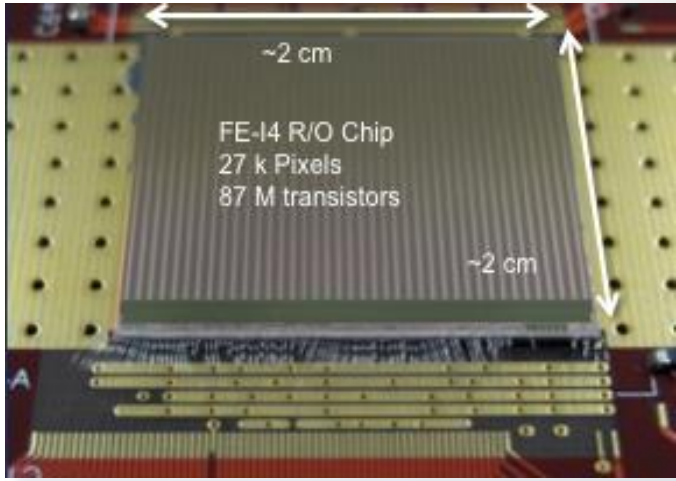
New Electronics for IBL



- New on-detector electronics:
  - FE-I4 – to cope with higher hit occupancy and radiation level closer to the interaction point as well as serving smaller pixel size.
  - Optoboard – to be placed further outside from the detector, implementing commercial connector housings, but uses same ASICs as for the current pixel detector (DORIC and VDC)
- New off-detector electronics:
  - Readout Driver (ROD) – to handle higher bandwidth and steer new front-end electronics
  - Back of Crate Card (BOC) – to serve higher bandwidth links and implement 2x more channels for detector and S-Link interface.
  - Basic structure in the readout is same as for the Pixel Detector, using VME-crate standard.

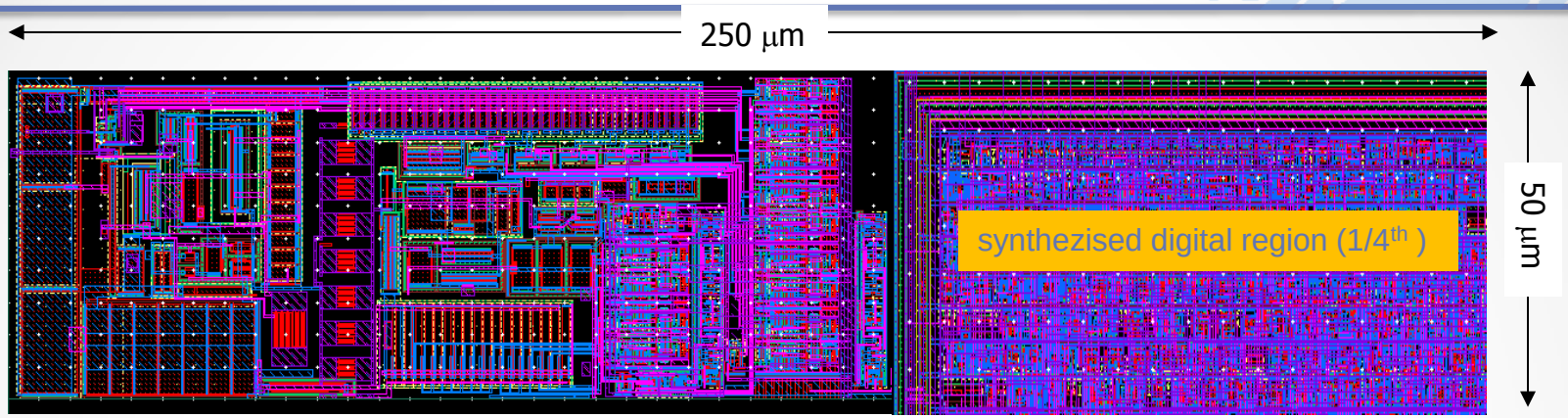
Front-End ASIC (FE-I4)

- As IBL is closer to the beam pipe, higher radiation levels and occupancy have to be handled.
- A new ASIC has been developed for IBL: **FE-I4**
- Designed in 130 nm feature size
- Chip provides 26880 pixel cells in 80 columns x 336 rows
- 87 million transistors
- Dimensions: 19 mm x 20 mm



- Pixel size: 50 µm x 250 µm
- 4 pixel readout: analog section per pixel, digital section shared
- Energy measurement via Time-over-Threshold (TOT) mechanism

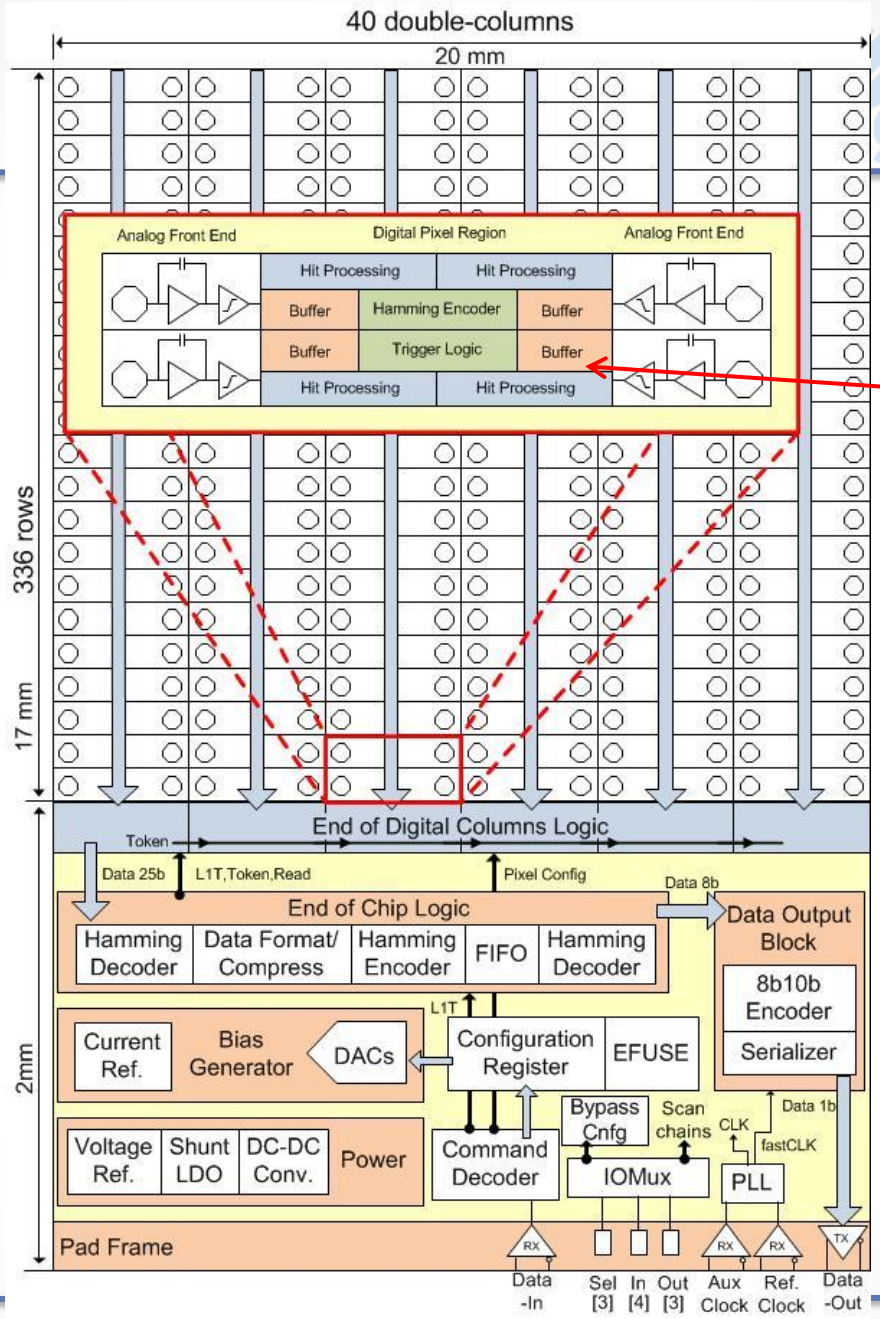
FE-I4 Design Features



- Smaller pixel size (better granularity), but big array -20 x 17 mm^2 active- (simpler module, less material).
- Low power (analog / digital array), low noise (digital / analog separation, T3 deep nwell), high radiation tolerance (130 nm) up to 250 MRad.
- 8-metal layers (good power distribution)
- New pixel digital organization: buffers in 4-pixel region (only triggered hits are transferred to EoDC) → efficient at high rate.
- Reduced analog capability + data reformatting + 160Mb/s data transmission → high rate data transmission.
- 130 nm process: well supported, commercial digital design tools.

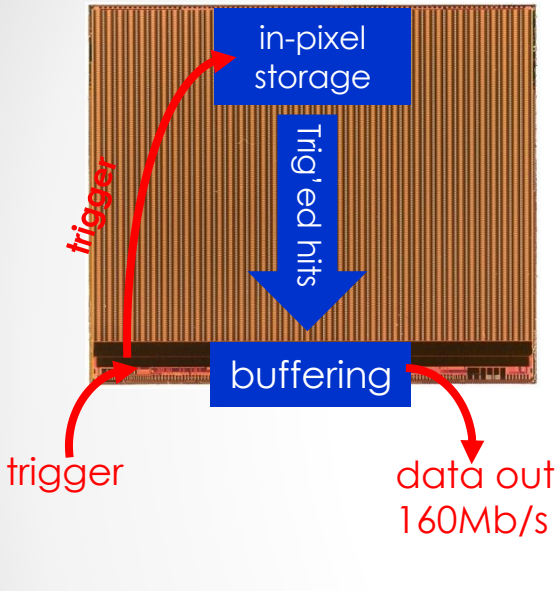
pixel array:
336 × 80 pixels

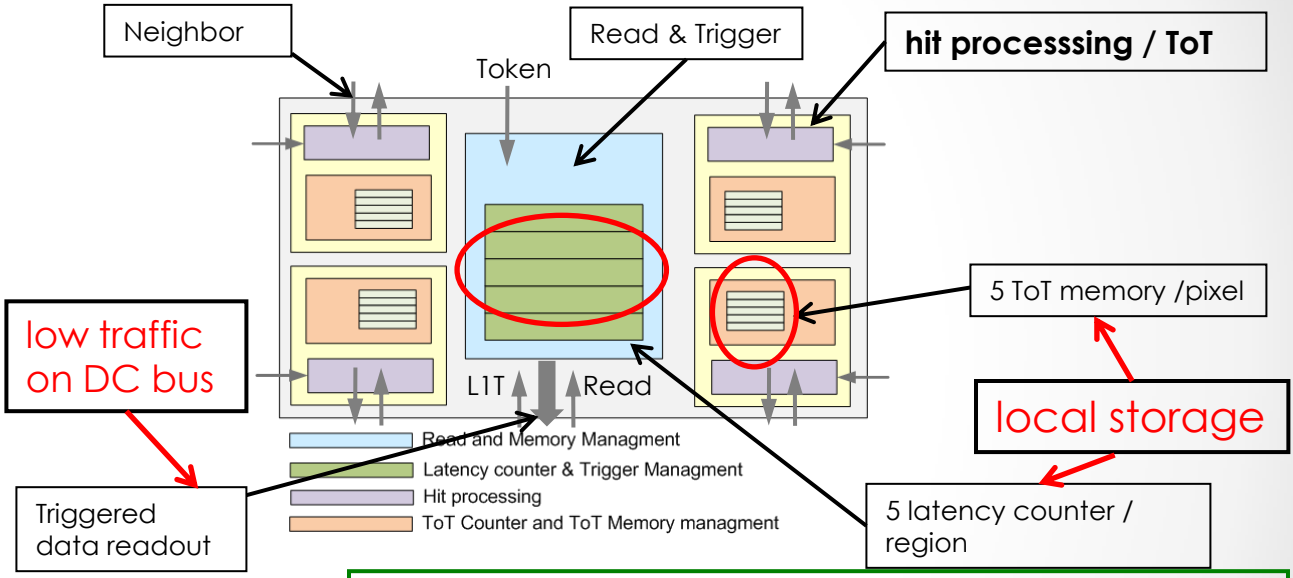
periphery



Performance at high hit rate

- FE-I4: local "in-pixel" storage + trigger propagated up the array.





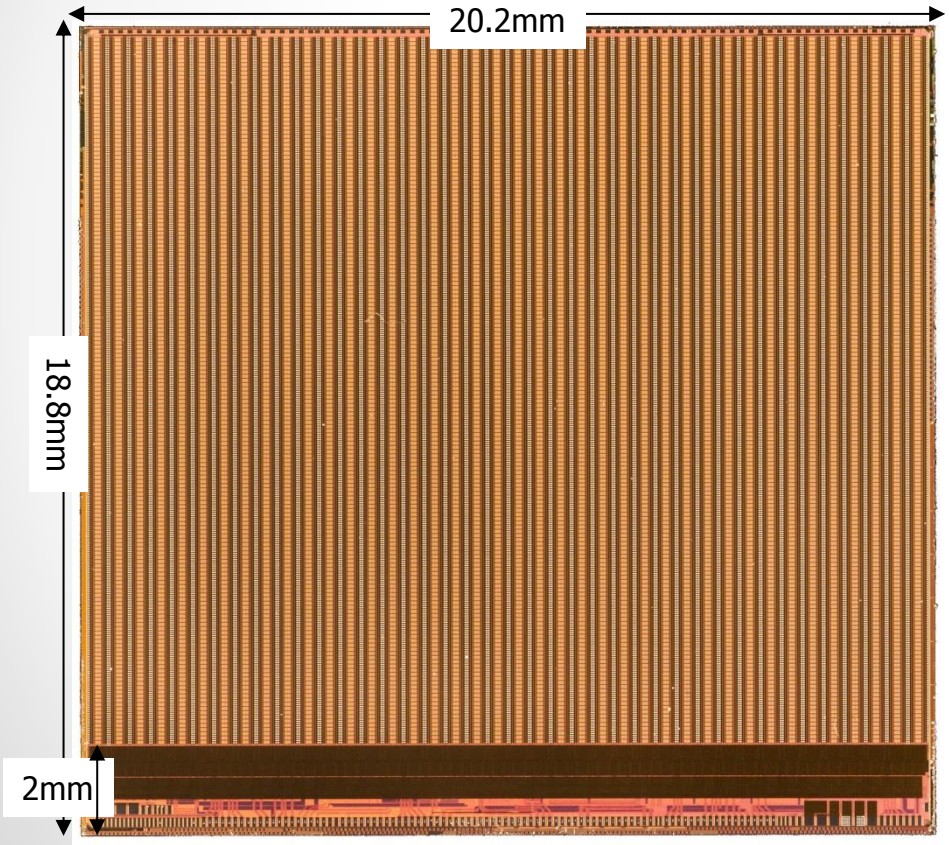
- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC → DC bus traffic "low".
- Each pixel is tied to its neighbors "time info" (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time. Handle on timewalk.

Summary:

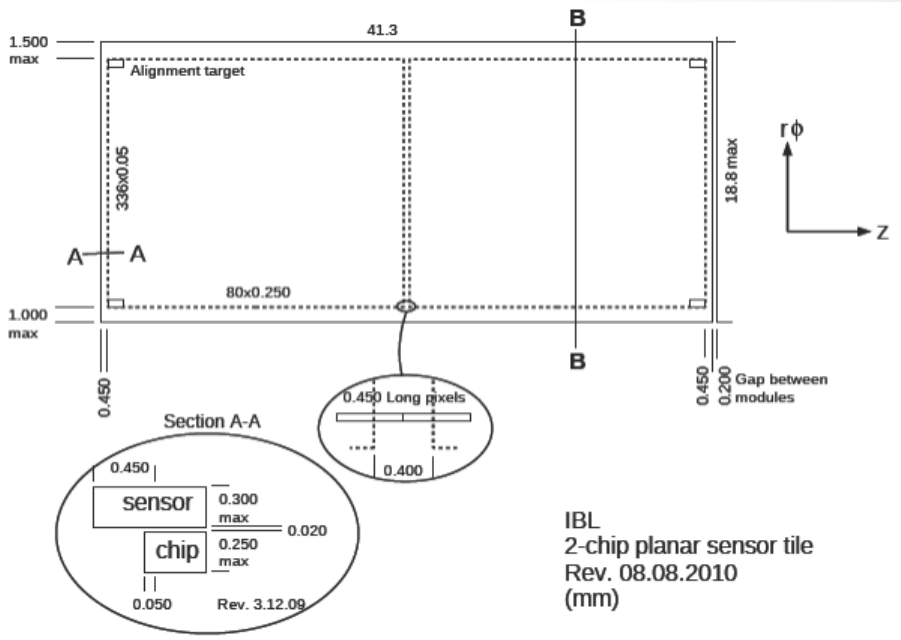
- Physics simulation → Efficient architecture.
- Spatial association of digital hit to recover lower analog performance.
- Shared resources & hit not moved around → Lowers digital power consumption.

FE-I4 Module

- FE-I4: 2.02 × 1.88cm^2.
- Active area: ~90%
- 26,880 pixels (80 × 336)



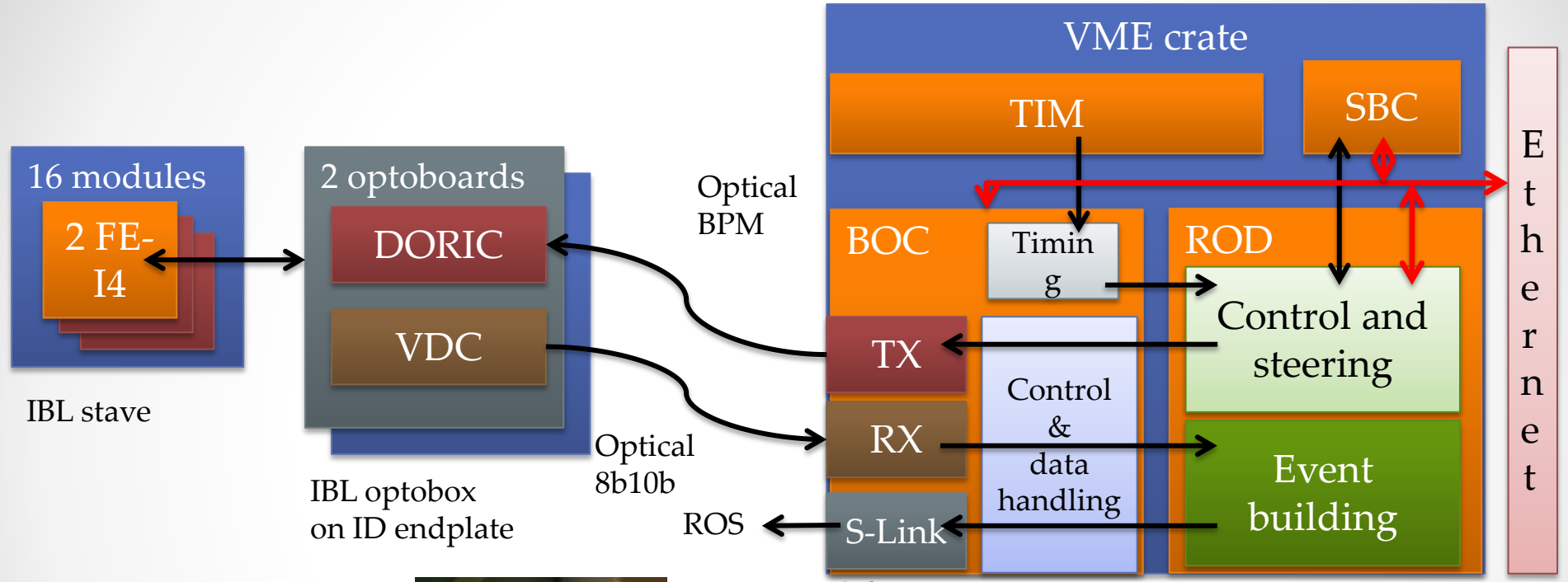
- Modules made from 2 ICs.
- Shared clk and cmd inputs.
- Each IC has dedicated output.
  ➔ Simpler module concept!



FE-I4 Improvement Thoughts

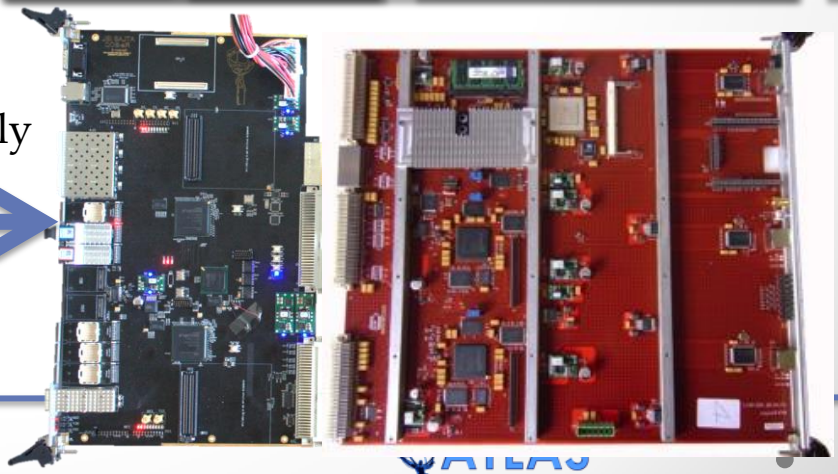
- Increase TOT resolution (currently 4 bits only) for better dE/dx measurements.
- Mechanism for digital region power consumption reduction was implemented into FE-I4B (clock gating), should this be changed?
  - Leaving empty regions unclocked reduces average power consumption.
  - Consequence is a varying power consumption which can be seen in threshold variation (hit/trigger activity driven). Small effect but measurable.
  - Cooling is sized for peak power consumption anyhow.
- Clock and command are decoded in optoboard and sent to the FE. Could be decoded in chip.
- Regulators are connected externally.

ATLAS IBL Readout Structure



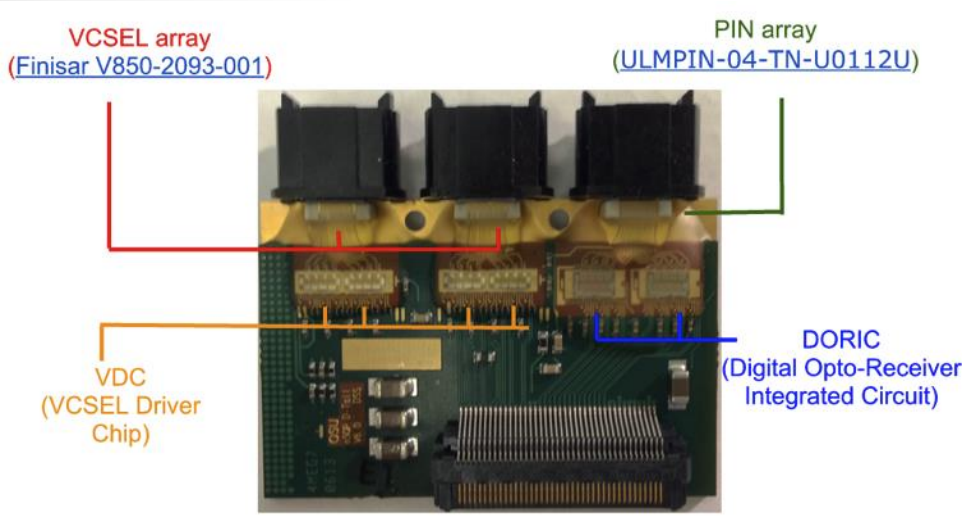
electrically

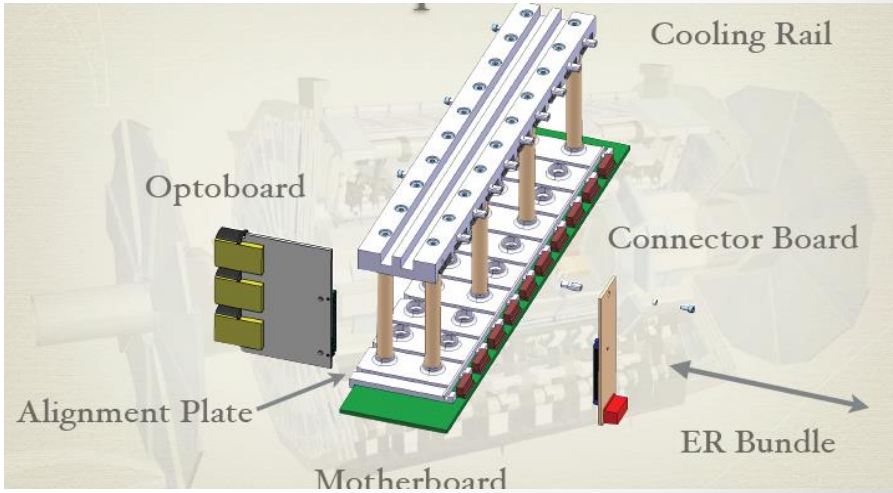
Optically



Optical components

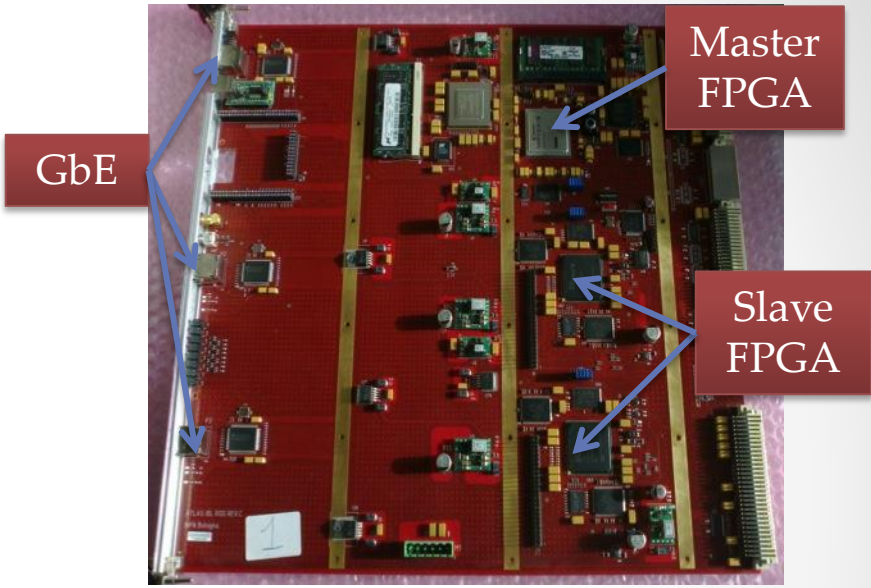
- Commercial SNAP12 Rx/Tx plugins for off-detector (on Back-of-Crate card)
- On-detector components custom made (Optoboard)
  - 2 VCSEL array & 1 PiN diode array for optical communication
  - 2 custom made ASICs (Digital Opto-Receiver IC, VCSEL Driver Chip), radiation hard
- Distance to detector module ~ 5.5m → data transmission via electrical path.



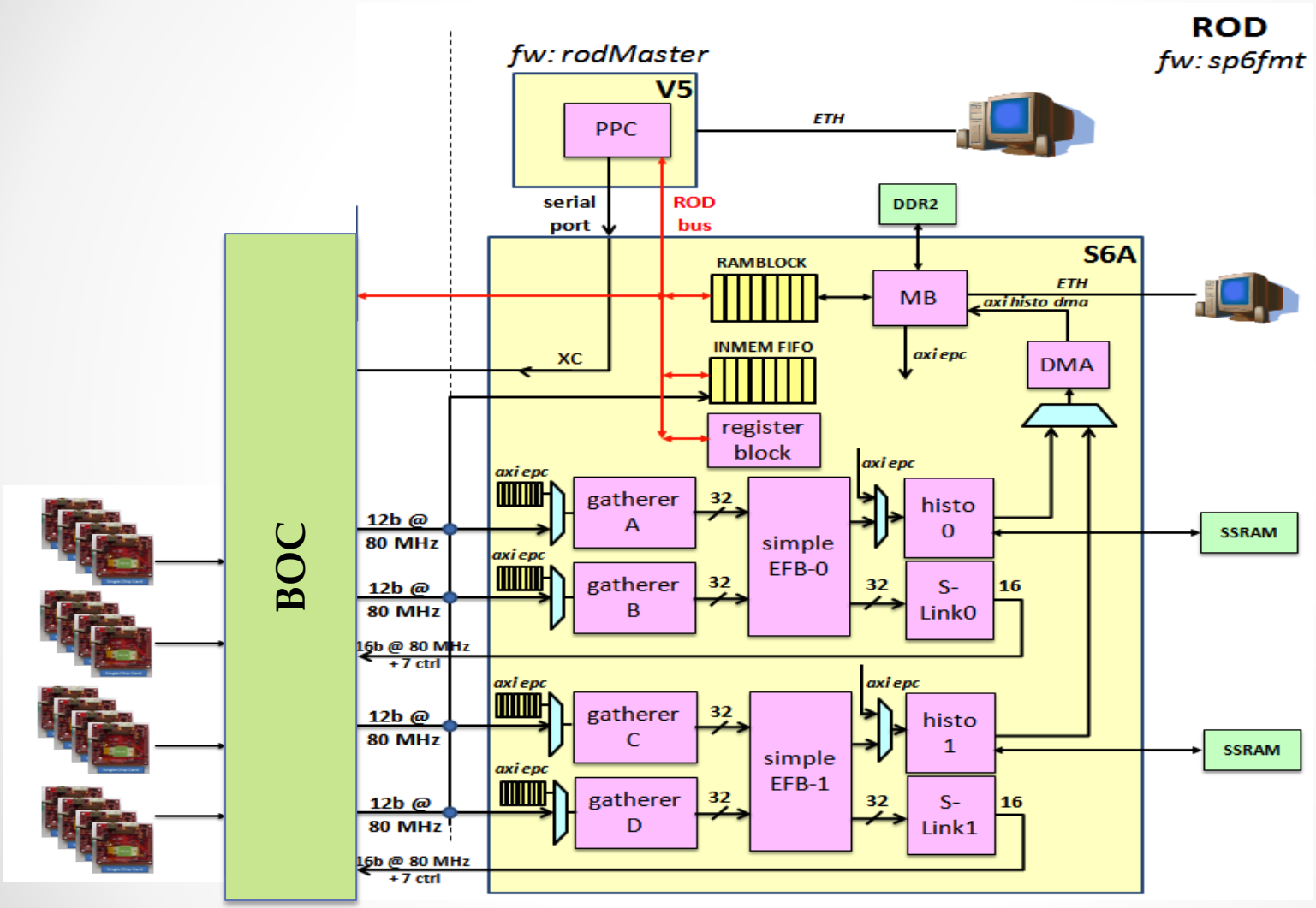


IBL Readout Driver

- Control card (9U VME):
  - Detector calibration
  - Physics data taking
- Master FPGA (Virtex 5 with PPC):
  - Control data generation
  - Run control
- 2 Slave FPGAs (Spartan 6):
  - Data interface to and from Back of Crate Card
  - Data preparation and histrogramming
- Data transmission in calibration mode via Ethernet to fit-farm computers
- Design requirement: Backward compatibility to old system

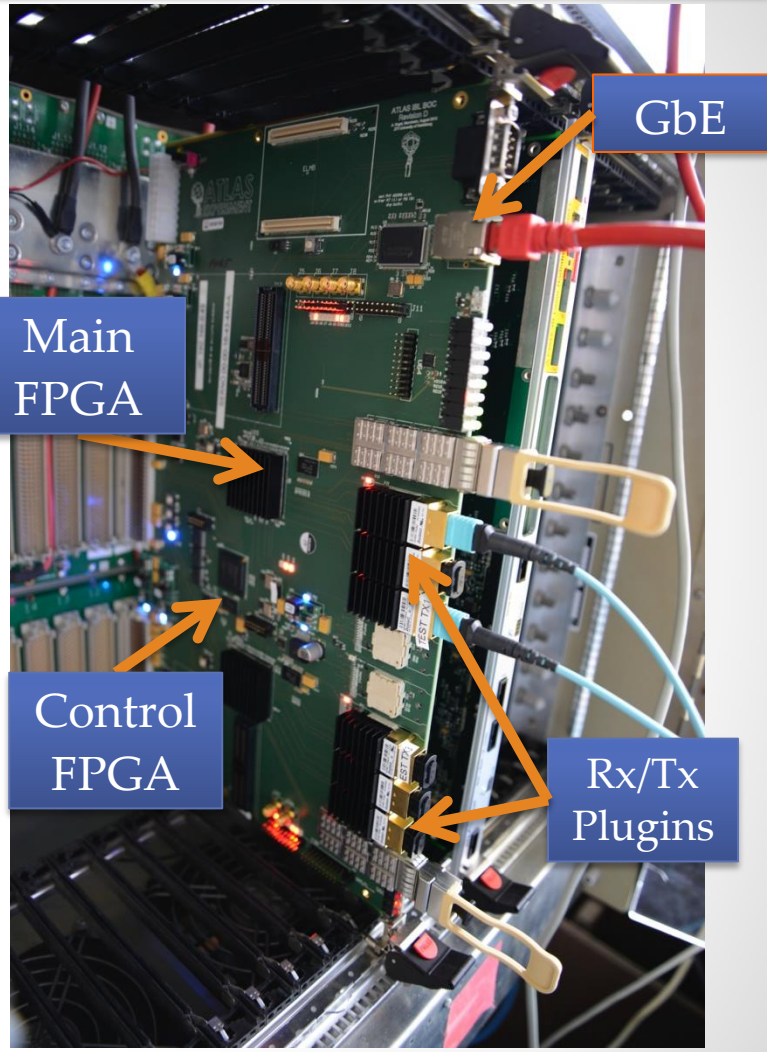


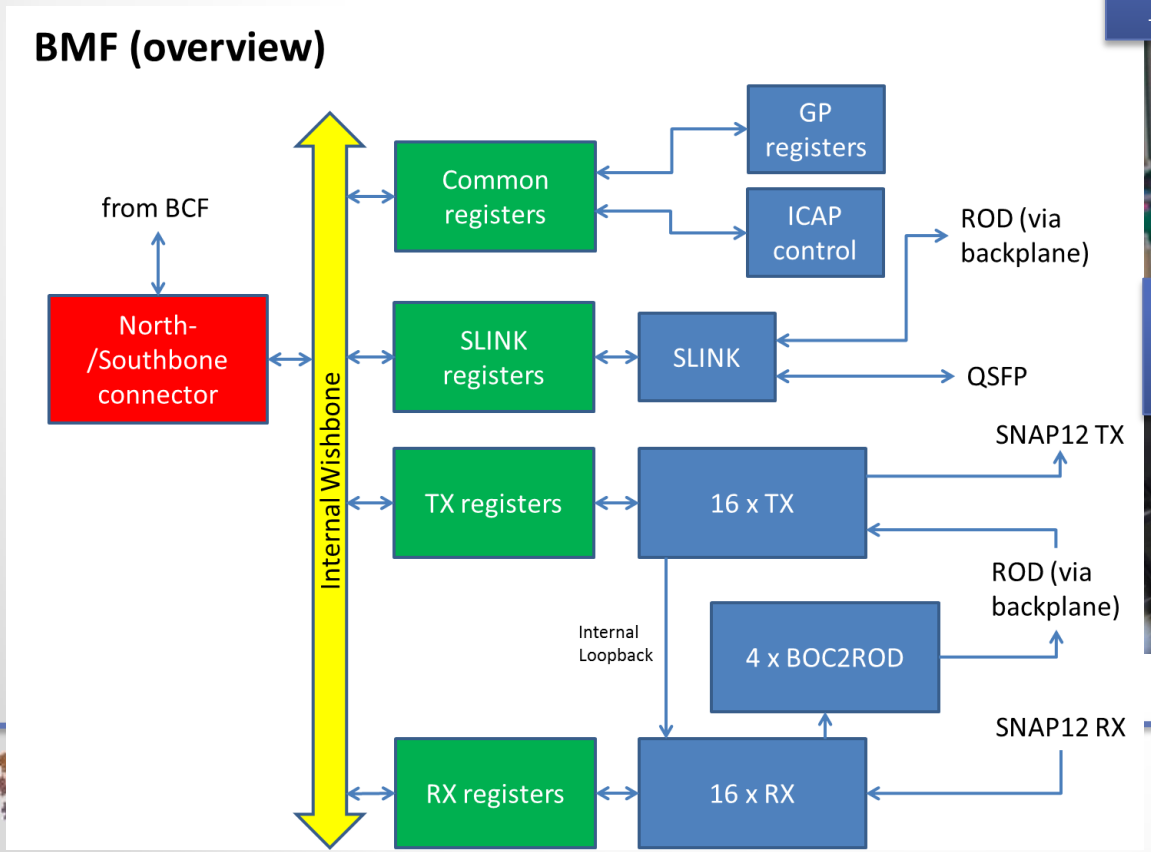
ROD FW Functionality



IBL Back of Crate Card

- Derives the timing for on- and off-detector electronics from timing interface (TIM)
- Optical interface to/from detector and Readout Buffers
- Data en-/decoding for detector communication



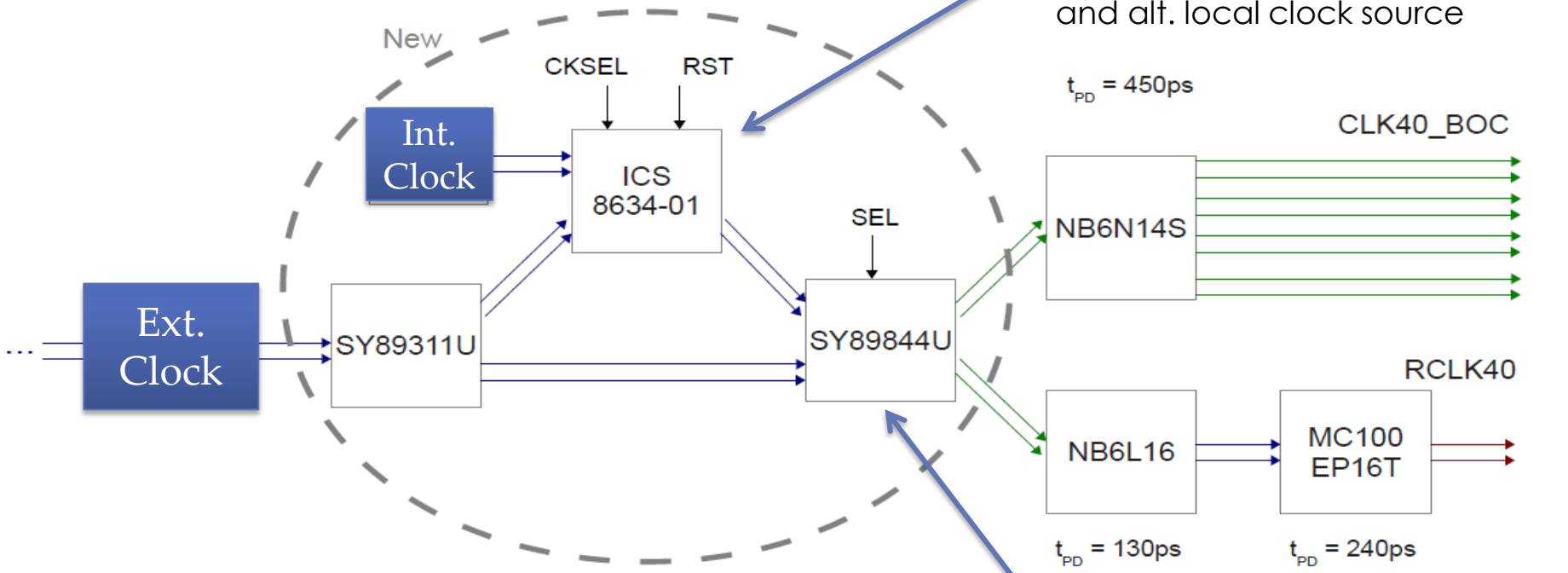


ATLAS EXPERIMENT

BOC revD clocking circuit

- CDCE62002 has been replaced due to non deterministic phase:

ICS8634-01: zero-delay PLL to provide minmal jitter cleaning/duty cycle adjustment and alt. local clock source



SY89844: MUX to select cleaned clock (default) or direct clock from delay line (variable duty cycle and jitter)

- Final clock cleaning in FPGA-PLLs, if needed at all
- Clock selection logic uses separate clock.

Readout Summary

- Newer FPGA technology would reduce boards needed
  - All IBL readout could go into one board plus opto connections.
  - Optical interface board could be completely passive.
  - Rule should be: Use the fastest I/O available in the chosen technology
- Main topic about the readout is FW and on board SW development
  - Careful planning and then enough manpower is needed
- FPGAs offer a great flexibility so that many different use cases can be realized in FW, while HW might be common.
- Only connection scheme, channel number, readout bandwidth must be detector specific