CMS Phase 1 Pixel Upgrade

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ACES 2014
Fourth Common ATLAS CMS Electronics Workshop
**Targets of Pixel Phase 1 Upgrade:** Installation 2016-17 EYETS

- Baseline $L = 2 \times 10^{34} \text{ cm}^{-2} \text{sec}^{-1} \& 25\text{ns} \rightarrow 50\text{ pileup}$
- Tolerate $L = 2 \times 10^{34} \text{ cm}^{-2} \text{sec}^{-1} \& \textbf{50ns} \rightarrow 100\text{ pileup}$, with reduced performance
- Survive Integrated Luminosity of $500\text{fb}^{-1}$ (Layer 1 $2 \times 250\text{fb}^{-1}$)
- Strategy of evolutionary upgrade with minimal disruption of data taking
- Same detector concept but **higher rates for ROC, data link & DAQ**
- More Robust tracking $3 \rightarrow 4$ pixel hits (e.g. future tracking point losses in strip system)
# System Parameters: Present & Upgrade

<table>
<thead>
<tr>
<th>Parameter of Pixel System</th>
<th>Present</th>
<th>Phase 1 Upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td># layers (tracking points)</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>beam pipe radius (outer)</td>
<td>29.8 mm</td>
<td>22.5 mm (LS1)</td>
</tr>
<tr>
<td>innermost layer radius</td>
<td>44 mm</td>
<td>29.5 mm</td>
</tr>
<tr>
<td>outermost layer radius</td>
<td>102 mm</td>
<td>160 mm</td>
</tr>
<tr>
<td>pixel size ((r-\varphi \times z))</td>
<td>(100 \mu \times 150 \mu)</td>
<td>(100 \mu \times 150 \mu)</td>
</tr>
<tr>
<td>In-time pixel threshold</td>
<td>3400 e</td>
<td>1600 e</td>
</tr>
<tr>
<td>pixel resolution (&lt;r-\varphi&gt; \times &lt;z&gt;_{\eta=0.25})</td>
<td>(10 \mu \times 28 \mu)</td>
<td>(10 \mu \times 28 \mu) (or better)</td>
</tr>
<tr>
<td>cooling</td>
<td>(\text{C}<em>6\text{F}</em>{14}) (monophase)</td>
<td>(\text{CO}_2) (biphase)</td>
</tr>
<tr>
<td>material budget (X/X_0) ((\eta=0))</td>
<td>6%</td>
<td>5.5%</td>
</tr>
<tr>
<td>material budget (X/X_0) ((\eta=1.6))</td>
<td>40%</td>
<td>20%</td>
</tr>
<tr>
<td>pixel data readout speed</td>
<td>40MHz (analog coded)</td>
<td>400Mb/sec (digital)</td>
</tr>
<tr>
<td>1st layer module link rate ((100%))</td>
<td>13 M pixel/sec</td>
<td>52 M pixel/sec</td>
</tr>
<tr>
<td>ROC pixel rate capability</td>
<td>(~100 \text{ MHz/cm}^2)</td>
<td>(~580 \text{ MHz/cm}^2)</td>
</tr>
<tr>
<td>control &amp; ROC programming</td>
<td>TTC &amp; 40MHz I^2C</td>
<td>TTC/TCDS &amp; 40MHz I^2C</td>
</tr>
</tbody>
</table>
Phase 1 Pixel DAQ

FED upgrade is required:

- More modules & optical readout links
  - 3→4 layers (768→1184 modules), 2→3 disks (192→672)
- Higher luminosity & data rates from modules (25 ns, 50 ns)
- Higher output rate to Central DAQ
- New 400 Mbps digital protocol for readout links

FEC upgrade considered as an option (c.f. TDR):

- Control & Clock/Trigger distribution unchanged
- Can initially operate with present VME-based system
  - Stock of VME FECs and parts is (very) limited
  - Additional control links needed for FPix
- Would improve configuration time & SEU recovery
Phase 1 Readout Architecture

Modules
- Token Bit Manager
- Hi Density Interconnect
- 2x8 ROCs

(672+1184) (FPix+BPix)

Forward FPix:
3 disks/side

Barrel BPix:
4 barrel layers

- Optical hybrids
- Flex
- Twisted

~1 m

12 ch fiber ribbons
~100 m

Service Electronics
(96+64)

- Service Cylinders
- US Cylinders

Detector

Service Cylinders

USC Racks (µTCA)

Central DAQ

2x10 Gbps

AMC13 (2+4)

TCDS (1+1)

Clk, L1A

DC-DC

(4+4)

DOH

CCU

TK-FEC (1+1)

mFEC (x8 link)

PX-FEC (6+4)

mFEC (x16 link)

12ch Rx

12ch Rx

12ch Rx

12ch Rx

12 ch fiber ribbons

FED (16+40)

- Token Bit Manager
- Hi Density Interconnect
- 2x8 ROCs

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Read Out Chip PSI46dig

Paul Scherrer Institute

Minimal ROC changes to improve existing Column Drain Architecture; 250nm CMOS (IBM)

Upgrade ROC must be capable for:

- increased luminosity by LHC machine $\sim 2 \times 10^{34}$
- higher pixel rates due to reduced Layer 1 radius ($r_{L1} = 30 \text{ mm}$)
- higher data output rate capability due to 50ns LHC operations
- reduced sensor signals due to irradiation (L1 sensor $\sim 250 \text{fb}^{-1}$)

ROC changes: (reduce data losses from e.g. buffer overflows)

- increase DC time-stamp- / data-buffers 12 / 32 $\rightarrow$ 24 / 80
- ROC internal token passage & double buffered (64) readout
- 160 Mbit/sec digital readout for pixel address & pulse heights
- ROC level 8-bit ADC for pixel pulse height digitization
- reduced pixel in-time threshold of 1600e (present 3400e)

$\rightarrow$ PSI46dig_v2 submitted Oct. 2013; works well in beam tests, production order soon

PSI46dig+ for Layer 1 ROC pixel rates $< 580 \text{ MHz/cm}^2$ (Engineering Run Spring 2014)

PSI46dig+ = Improved ROC with Dynamic Column Drain Cluster (DCDC) architecture & reset free DB operation. Change to internal DC mechanisms, otherwise same from outside
Token Bit Manager

TBM manages readout of ROC token rings & defines data packets
• Passes L1A, caches triggers, manages RO token, adds TBM header/trailer

400 Mbps Output:
• Data Keeper Interleaves two 160 Mbps ROC chains to 320 Mbps output
• 4B/5B NRZI encoding (→400 Mbps) for balanced code on optical link

Fast 40 MHz I2C interface for programming ROC parameters
Layer 3,4 & Fpix: TBM08 single output; Layer 1,2: TBM09 dual output
TBM08 prototype run & testing complete; TBM08a/TBM09 preseries March 2014

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FED Main Functions

- Receive TTC for BX Clock/L1A/B-channel
- Receive (asynchronous) optical input on 12-ch ribbons
- Decode digital pixel data @ 400 Mbps 4B/5B NRZI
  - DeMux & decode 2 TBM/ROC chains per input channel
- Buffer event fragments from each channel
- Assemble event fragments from same trigger, encode & transmit to central DAQ
- Handle exceptions from input channels
- State machine for TTS feedback to central trigger/DAQ
  - Ready, Busy, Warn, Out-of-sync, Error
- Local DAQ readout via subsystem CPU access
- Diagnostic monitoring during data taking via subsystem CPU
Exception Handling

• Handle Exceptions from input channels
  • (While maintaining synchronization with central DAQ)
  • Timeouts for missing data
  • Overflows for too much data
  • Detect Out-of-sync: TTC event# ≠ TBM event#
  • Disable problematic channels & recover automatically when possible
  • Detect TBM header/trailer error conditions

• State machine for TTS feedback to central trigger
  • Busy, Ready, Warn, Error, Out-of-sync
  • N.B. present use of Warn for fast resets & adjustable thresholds for OOS, Busy
Phase 1 FED Concept

• Meetings & Workshops in 2012-2013
  • Requirements, use cases, (re)evaluate options (VME | uTCA)
  • Concept: double-width uTCA AMC
    o 4x 12-ch optical receiver on FMC
    o FPGA for decoding, buffering, event building
    o 2x 10 Gpbs optical output

• Plan for uTCA FED reaffirmed in August 2013
  • Build on synergy with uTCA developments in CMS & present pixel FED experience
  • Hardware – CERN/ESE group based on FC7
  • Firmware – Vienna, Strasbourg
    o Vienna – front-end fw: decoding incoming data, error handling
    o Strasbourg – back-end fw: event building, DAQ-links
  • Involve other pixel groups on online software, system tests, production testing
    o CERN-CMS, Cornell, FNAL, KSU, Rice, Vanderbilt & Others
FC7 Platform

- FMC Carrier Xilinx Series 7
  - Jointly developed at
  - Imperial College (Mark Pesaresi) and
  - CERN/ESE (Paschalis Vichoudis)

- Double-width uTCA AMC
  - Kintex 7 FPGA (XC7K420R/480T)
    - 400k logic cells, 30Mb RAM
    - 400 std IO, 32 GTX, rates to 10Gbit/s
  - Two FMC connectors
    - Host optical transceivers
  - MMC, 4 GB SRAM, uSD card

- R0b prototypes tested
  - GTX MGTs working well at 10 Gbps
  - FMC connections as intended
  - MMC, core firmware in place

- R0b now in production for TCDS upgrade
- R0b FC7s for pixel DAQ development
- Refined design (if needed) for pixel FED/FEC production 2014-2015
- Pixel requirements & firmware
  - CERN, Strasbourg, Rice, Vienna, Kansas State
Pixel FED Opto FMC

- FED & FEC would use FPGA Mezzanine Cards to mount optical components
- First RX prototypes ready:
  - FMC with 2x 12-way optical receivers (FITEL)
  - Testing of Fitel Rx underway @400 Mbps
- DAQ link adds SFP+ to FMC
  - 10 Gbps DAQ link implemented by CMS-DAQ group as fw block
  - Also used by AMC13xg
- FC7-based FED with two FMCs would host four 12-ch receivers & two 10 Gbps SFP+ TRx for central DAQ

FITEL receiver on socket with heat-sink
Also can be mounted directly on PCB
Note fiber pigtail to front-panel connector

SFP+ optical TRX module
FED Input Link Data Rates

- Number of Links chosen to manage expected data rates
- Full Geant 14 TeV MC simulation @ 2.5 E34 25 ns & 50 ns
  - Note 2.5E34 taken for estimates here

<table>
<thead>
<tr>
<th>Location</th>
<th># Links/2x8 Module</th>
<th>Link Rate 25 ns BX</th>
<th>Link Rate 50 ns BX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1</td>
<td>4</td>
<td>140 Mbps</td>
<td>269 Mbps</td>
</tr>
<tr>
<td>Layer 2</td>
<td>2</td>
<td>78 Mbps</td>
<td>137 Mbps</td>
</tr>
<tr>
<td>Layer 3</td>
<td>1</td>
<td>81 Mbps</td>
<td>133 Mbps</td>
</tr>
<tr>
<td>Layer 4</td>
<td>1</td>
<td>57 Mbps</td>
<td>85 Mbps</td>
</tr>
<tr>
<td>Inner Rings</td>
<td>1</td>
<td>129 Mbps</td>
<td>231 Mbps</td>
</tr>
<tr>
<td>Outer Rings</td>
<td>1</td>
<td>68 Mbps</td>
<td>107 Mbps</td>
</tr>
</tbody>
</table>

Layer 1 Limits: 15% Margin @ 2.5E34 50ns

Note: Links saturate at 320 Mbps & will give dead-time sometime before
Estimated Output Rates

- **L**=2.5E34 25/50 ns
- Full Geant simulation
- Averages for 12-ch receivers
- Natural groupings of 2*12-ch inputs to one output link
- 5 Gbps marginal
  - No link overhead included
- Specify 10 Gbps
  - Capable for saturated input links: FED not a bottleneck
  - Central DAQ FERROL upgrade (LS1) will support
- Avg. Event Size (2*12-ch)
  - BPix 2430/4860 bytes
  - FPix 2500/5000 bytes
  - ~2/4 Gbps (per link)

<table>
<thead>
<tr>
<th>Layer</th>
<th>12-fiber Evt size (kB)</th>
<th>12-fiber Rate (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.48/4.96</td>
<td>1.98/3.99</td>
</tr>
<tr>
<td>2</td>
<td>1.14/2.28</td>
<td>0.91/1.82</td>
</tr>
<tr>
<td>3</td>
<td>1.01/2.02</td>
<td>0.81/1.62</td>
</tr>
<tr>
<td>4</td>
<td>0.54/1.08</td>
<td>0.43/0.80</td>
</tr>
<tr>
<td>Din</td>
<td>1.99/4.04</td>
<td>1.59/3.23</td>
</tr>
<tr>
<td>Dout</td>
<td>0.78/1.55</td>
<td>0.62/1.24</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2*12-ch Avg</th>
<th>Output Rate 25/50ns (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1+L4</td>
<td>2.42/4.84</td>
</tr>
<tr>
<td>L2+L3</td>
<td>1.72/3.42</td>
</tr>
<tr>
<td>Din+Dout</td>
<td>2.21/4.47</td>
</tr>
<tr>
<td>Dout+Dout</td>
<td>1.24/2.48</td>
</tr>
</tbody>
</table>

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Vienna FED Deserializer Card

• Test boards with Zarlink 12-ch receiver & FPGA developed in Vienna for phase 1 FED R&D
• Mounts on present VME FED (conversion kits)
  • Firmware development: analog link → digital link
  • Tests of digital data transmission
    o successful with emulated data
    o same firmware used in first tests of digital modules – works!
• Deserializer firmware ported to VHDL and Xilinx for uTCA/FC7
• Used for system tests & production testing with VME systems
FECs

• FEC types
  • TK-FEC – communicates with CCU via DOH
  • PX-FEC – communicates with TBM via mDOH
  • Same hardware, different firmware
• VME Option
  • Keep present system & expand # channels (FPix)
• uTCA Option
  • Kept in planning, may be installed later (LS2)
  • Based on same FC7 board as FED
  • Optical mezzanine boards from TCDS upgrade
  • Prototype hardware and CCU firmware in progress at Strasbourg
  • Pixel firmware development in US (KSU, Rutgers)
Pixel FED & FEC FMCs

- FMC with 8x 2-way optical SFP transceivers could be mapped to 4 Digital Opto Hybrids
  - From the TCDS upgrade project
  - SFP is 1Gbps Ethernet, but works at lower data rates
  - 2 FMC/FC7 → Call this FEC\(_8\)
- QSFP optical TRx option under investigation
  - 10GbE parts must be qualified for lower data rates
  - Mounting four on FMC would double # DOH on each uTCA FEC to 16 → FEC\(_{16}\)

uTCA FEC option FC7+FMCs

TCDS upgrade 8x2 way SFP FMC Suitable for FECs

Commercial dual QSFP FMC

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• Space, infrastructure, mechanics & cooling to install at location of third forward disk in present detector
• Will install a small pilot system during LS1 in 2014 to test new phase 1 modules and readout electronics
Pixel Phase 1 Pilot System

- Two assemblies each with 4 modules (2 blades)
  - DC-DC converters on one assembly
  - Conventional powering for the other

2x8 module
Approximate
Phase 1 FPix geom.
r~ 6–13 cm

FPix cooling channel
Half-Disk mechanics

FPix-style readout
Using prototype
Phase 1 electronics

Essential *in situ* test of phase 1 electronics; leads development for full phase 1
Summary

• New phase 1 pixel detector for operation in 2017
  • Improved tracking performance at higher luminosity
  • $3 \rightarrow 4$ pixel tracking points
  • Frontend ASICs & DAQ upgraded to match requirements
• Frontend ASICs (ROC/TBM) nearing final production
  • First modules working
• DAQ backend electronics under development
  • New uTCA FED with 400 Mbps input 10 Gbps output
  • New uTCA FEC option leveraging FED development
• Small Pilot system installed in CMS during LS1 to pave the way for full system integration and fast commissioning in 2016-2017 during EYETS
Additional Material
Data Rate Studies

- Full simulation of phase 1 geometry CMSSW
  - Combine minbias and signal sample
    (t tbar as proxy)
  - @2E34 cm\(^{-2}\) s\(^{-1}\) 25 ns bunch spacing:
    o 50 pileup events
  - @2E34 cm\(^{-2}\) s\(^{-1}\) 50 ns BX
    o 100 pileup events
  - L1A rate = 100 kHz
- Measure average data rate on POH-FED links

**Conclusions:**
Hit rate in inner rings ~ layer 2
Requires 1 fiber/module on inner ring
Simulated (25ns BC) Pixel Hit Rate (Hits/cm²/s) per ROC for Layer 1

Average: 525 MHz/cm²
Range: 390 - 600

Each bin is one ROC

Visible Ladder structure
Z dependence from cluster size
Hit Rate Layer 2

Simulated Charged Particle Fluence (Hits/cm^2/s) per ROC for Layer 2

Each bin is one ROC

Average: 140 MHz/cm^2
Range: 95 – 152

Z dependence from cluster size
Figure 3.7: Forward Endcap detector pixel hit rates presented as hits/cm$^2$/s averaged over each ROC for simulated trigger events with 25 ns bunch spacings. The results for each disk for both $\pm z$ are presented separately. Each plot contains the hit rates for the inner and outer disks. The plots also indicate an expected gradual decrease in hit rates as the radius from the beam pipe increases.

Hit Rates Disk 1
Simulated (25ns BC) Pixel Hit Rate (Hits/cm$^2$/s) per ROC for Disk +1

Average:
70 MHz/cm$^2$
Inner 105
Outer 39

Range:
Inner 50–200
Outer 13–63

Hit rates similar on all 3 disks
Strong radial dependence

Each bin is one ROC

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Hit Rates Disk 3

Simulated (25ns BC) Pixel Hit Rate (Hits/cm²/s) per ROC for Disk +3

Average: 77 MHz/cm²
Inner 104
Outer 40

Range:
Inner 50–200
Outer 12–65

Hit rates similar on all 3 disks
Strong radial dependence

Each bin is one ROC
FED Teststand at TIF

- Module emulator
  - ROC test board + modified firmware (ROC/TBM emulator)
- Optical signal chain
  - POH prototype
- VME FED + daughter board
- Purpose
  - Tests of digital FED
  - Tests of digital data transmission
  - Online software development for pilot system
uTCA Status

- FED & FEC based on FC7
  - FMCs for optical Rx, TRx
- FC7: New version R0b
  - At CERN for testing (IC&CERN)
  - FMC connection & devices work
  - Testing & core fw/sw dev continues
  - Boards for FED prototypes to Strasbourg at end of March
- FED firmware:
  - TBM Deserializer ported to Xilinx in Vienna now at Strasbourg
- FEC-CCU firmware (Strasbourg):
  - VHDL translation works on mFEC
  - Ready for implementation in Virtex 6 & testing on GLIB
uTCA

CMS-approved Vadatech uTCA “Crate”

- Compact crates: 12 “double-wide” Advanced Mezzanine Cards (AMC)
- Power supply, Controller hubs
- High-speed serial connections on fabric backplane
  - PCIe, GbE, SATA, & custom
- Emerging standard for CMS & HEP
Development by (E. Hazen) Boston Univ. for common CMS uTCA electronics
Needed for clock, L1A and fast command (reset) fanout in uTCA crate
Also has 10 Gbps DAQ links available for spy/private readout
Status: Tested, first production run Dec 2013 (available 2014)
uTCA GLIB

- Double width AMC
- Fast Serial I/O
  - Two GbE
  - Two PCIe2.0 x4 lanes
- Virtex 6 FPGA
- 72 MB memory on board
- JTAG & CPLD
- 4 SFP+ optical links
  - Bidirectional 6.5 Gbps
- Two FPGA Mezz. Cards (FMC)
  - 4x6.5 Gbps
  - 80 FPGA connections
- R&D platform for pixel FEC
  - FMC(s) for optical receivers

CERN GLIB – gigabit link interface board uTCA crate or bench top with PC via e-net
Successor project FC7 with Xilinx series 7 FPGA
In development 2013 (UK/CERN)