ATLAS FTK

Alberto Annovi – INFN Frascati
On behalf of the FTK working group
Fast Tracking in Pixel and SCT detectors

Example:
R-phi view of Barrel region:

3 PIXEL layers + IBL

Track crosses 12 detector layers

4*2 SCT layers
A track co-processor for HLT

Close to offline do resolutions for b-tagging

Improved performance with IBL under study
Applications: taus, MET, jets, full scan searches
FTK in the TDAQ system

Full scan track finding $p_T > 1 \text{ GeV/c} \ @ 100 \text{ kHz}$
Latency $O(100 \mu s)$
Tracks available to HLT at full L1 rate
FTK in the TDAQ system

- Pixels & SCT
- RODs
- Data sharing 64 $\eta$-$\phi$ towers

100 kHz Event Rate

ACLs workshop, March 19th, 2014

Data preparation & global functions

AM Pattern recognition & 8 layer track fitting 512 pipelines

12 layer track fitting & duplicate removal

FLIC

Second Stage Fit (4 brds)

Core Crate $45^\circ\pm10^\circ$ in $\phi$
8 $\eta$-$\phi$ towers
2 PU/tower

DO TF Proc. unit

DO TF Proc. unit

DO TF Proc. unit

Data Formatter

Cluster finding

Pixels & SCT

RODs

Raw Data ROBs

Track Data ROB

FTK ROBs

HLT Processing
FTK_IM and Data Formatter

FTK_INPUT MEZZANINE
INFN FRASCATI
U. WASEDA
U. THESSALONIKI

DATA FORMATTER
FERMILAB & U. CHICAGO

+ 4 FTK_IM/DF
+ Total 16x2Gb/s input & out to DF
+ Each FTK_IM
  + Receive ROD's data
  + strip and pixel clustering
  + has 2 Spartan6 150T FPGAs

CUSTOM 2D CLUSTERING ALGORITHM
MULTI-CORE IMPLEMENTATION TO PROCESS WITH PIXEL 40MHz HIT RATE

ATL-DAQ-PROC-2013-037

FROM DETECTOR
X16
TO PU, SSB AND DF
~200Gb/s TOTAL

A. ANNOVI FOR THE FAST TRACKER GROUP
Processing 64 $\eta$-$\phi$ towers in parallel

64 $\eta$-$\phi$ towers definition
4 $\eta$ towers *

* 16 fold $\phi$ symmetry

ACES workshop, March 19th, 2014
ATCA Data Formatter

64 $\eta$-$\phi$ towers definition
4 $\eta$ towers *

* 16 fold $\phi$ symmetry

32 Data Formatters

ACES workshop, March 19th, 2014
ATCA Data Formatter

The DF meets the BW requirements with significant margin

<table>
<thead>
<tr>
<th></th>
<th>BW requirement</th>
<th>Reserved BW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total (output stream)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Pixel Total (output stream)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SCT Total (output stream)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>AUX</td>
<td>8.98</td>
<td>48</td>
</tr>
<tr>
<td>SSB</td>
<td>2.37</td>
<td>6</td>
</tr>
<tr>
<td>Fabric</td>
<td>2.62</td>
<td>10</td>
</tr>
<tr>
<td>Local Bus</td>
<td>7.52</td>
<td>24</td>
</tr>
<tr>
<td>Inter-Crate</td>
<td>5.58</td>
<td>20</td>
</tr>
</tbody>
</table>

[ATL-COM-DAQ-2013-015]
See next talk by Ted Liu
http://www-ppd.fnal.gov/EEDOffice-w/Projects/ATCA/

ACES workshop, March 19th, 2014
A. Annovi for the Fast Tracker group
AM pattern recognition

- AM find track candidates with enough Si hits
- $O(10^9)$ patterns for FTK
- Patterns simultaneously see the silicon hits leaving the detector at full speed.
- Pattern recognition is complete as soon as all data is received! $\Rightarrow$ low latency
- Based on the Associative Memory chip (content-addressable memory) initially developed for the CDF Silicon Vertex Trigger (SVT). [L. Ristori, M. Dell’Orso NIM A 278, 436 (1989)]
FTK Associative Memory (AM) chip R&D

<table>
<thead>
<tr>
<th>AMchip</th>
<th>Technology</th>
<th>Area mm²</th>
<th># patt</th>
<th>MHz</th>
<th>µW/MHz/patt/layer</th>
<th># layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>03 (CDF)</td>
<td>180nm</td>
<td>100</td>
<td>5k</td>
<td>40</td>
<td>1000</td>
<td>6</td>
</tr>
<tr>
<td>04</td>
<td>65nm</td>
<td>14</td>
<td>8k</td>
<td>100</td>
<td>36</td>
<td>8</td>
</tr>
<tr>
<td>06 goal</td>
<td>65nm</td>
<td>~180</td>
<td>128k</td>
<td>100</td>
<td>-(20-40)%</td>
<td>8</td>
</tr>
</tbody>
</table>

Memory density (patterns*layers/area) x 18
Power consumption/pattern/layer/MHz 1/28
AMchip04 met 4W/128k pattern goal!
+ variable resolution: doi:10.1109/ANIMMA.2011.6172856

Parallel LVCMOS IO
8k patterns, 65nm Yield>80%
Tested up to 100MHz
LPNHE Paris, INFN: Frascati, Milano, Pisa

Combined std cells & full-custom
Full custom block 64 half patterns
std cell or mixed Full custom block 64 half patterns

Miniasic (2013)
Test serialized IO at 2Gbps
Test of alternative AM cell
Using a commercial Ser/Des IP

ACES workshop, March 19th, 2014
A. Annovi for the Fast Tracker group
AMchip05 prototype (submitted)

AMchip05 combine all features of final AMchip06
Smaller area: 3k patterns in 12mm² (vs 128k in~180mm²)
AMchip05: reduce power 20-40% (2-3W/128k patterns)
Note: for AMchip06 (128k patterns) memory access at ~2Pbit/s
FTK will use 8192 AMchip06

10 DES (input) 1 SER (output) at 2Gb/s
Processing unit (PU)

Main computing unit:
Number of needed PUs scales with FTK coverage & pileup.
Staged installation.

+ AM board w/ 8M patterns
+ Perform pattern recognition as data flows
  
+ AUX: 4G fits/s/AUX
+ Cluster database
+ Track Fitting
  + \( \chi^2 \) significant fake reduction
+ duplicate removal (partial)

\[ p_i = \sum_j C_{ij} \cdot x_j + q_i \]
AM board & LAMB

Functions:

- Hits distrib. 16-24 Gb/s
- * 64 AM chip (tot 1 Tb/s)
- Collect roads 32 Gb/s

LAMB Local AM board (PI-MI-PV) for AMchip04

LAMB w/ 4 AM miniasics

AMBSLP (VME 9U) for AMchip05/06 (Europe)

Provide up to 160 W @1V
64 AMchip06s
8M patterns

Smaller & simpler
Serialized IO

Parallel IO

LAMBSLP-1
LAMBSLP-2
LAMBSLP-3

ACES workshop, March 19th, 2014

A. Annovi for the Fast Tracker group

ATL-DAQ-PROC-2013-041
The AUX Card

• The Processing Unit has a multifunctional Auxiliary Card
  • VME Control through main board through P2 connector
  • Converts clusters to SuperStrips
  • Receives matched road IDs and fetches full resolution hits
  • Performs 8 layer fit to reject bad roads
  • Sends roads+hits to SSB for 12 layer fit
• Total 220 Gb/s in/out/on board IO
Second Stage board (SSB)

- Extrapolate from 8 to 12 layers
- Retrieve compatible hits
- Perform 12 layer fit
  - $\chi^2$ and helix parameters
  - high RAM b/w for fit constants
  - Low memory usage, High logic use
- Full duplicate removal (Hit Warrior)
  - Low logic usage, High memory usage
- 6 Kintex 7 FPGAs: XC7K325T-1FBG676C
- 24 RLDRAM
  - MT49H16M36BM-25:B
  - 16Mb x 36 Banks (576Mb)
  - 38.4 Gb/s peak bandwidth (x36 at 533 MHz)
  - ~900 Gb/s total RAM b/w on board

U. Illinois at Urbana C.
FTK to L2 Interface Crate (FLIC)

- Collect found tracks
- Fast lookup for global module ID @ 40 MHz
- Assemble events at 100 kHz
- Implement global functions
  - E.g. count tracks above threshold
- 2x (8 S-LINKs input and 8 output)

1 ATCA shelf: 2 Input and 2 output cards

ACES workshop, March 19th, 2014

A. Annovi for the Fast Tracker group
FTK crates

+ 4 ATCA shelves (DF)
+ 8 VME core crates
  + ~5.8kW/crate power
  + AM board 16*~250W
  + AUX 16 * ~90W
  + SSB 4 * ~90W
+ non-standard power distribution
+ non-standard cooling
+ 1 ATCA shelf (FLIC)

Two options to deliver ~5.8kW
70 A on 5 V and A or B
A) 300 A on 12 V and 40 A on 48 V
B) 180 A on 12 V and 70 A on 48 V
Cooling measurements

VME crate filled with “heating” cards and old CDF AM boards. Total power 4.5kW over 15(+2) boards.
> 260W / board (cfr ~250W estimated for AM board)
Cooling measurements

6 temperature sensors

Slots of hyper blow fans < ~70°

6 sensor positions

Temperature (°C)

Board position (slot #)

Upper front

80°

40°

CDF modified fan tray

Wiener standard fan tray

1 line / board

1 line / board

Upper front

40°

80°

INFN Pavia & Pisa

ACES workshop, March 19th, 2014
Summary

+ FTK includes several algorithms
  + Clustering
  + Associative Memory pattern matching
  + Track Fitting (in two steps)
  + Duplicate removal

+ High parallelism
  + 8192 AMchips
  + O(2000) FPGAs (Spartan6, Kintex, Arria V)
  + O(2000) fibers

+ ATCA for high-bandwidth data sharing

+ VME for higher board area & higher # of boards per crate
Thanks for your attention
One flip-flop per layer stores the match results.

Flexible input: position, time, objects (e, µ, γ)

Pattern matching is completed as soon as all hits are loaded.
Data arriving at different times is compared in parallel with all patterns.
Unique to AM chip: look for correlation of data received at different times.
AM technological evolution

- (90’s) Full custom VLSI chip - 0.7µm (INFN-Pisa)
- 128 patterns, 6x12bit words each, 30MHz


Alternative FPGA implementation of SVT AM chip
G Magazzù, 1st std cell project presented @ LHCC (1999)

Standard Cell 0.18 µm → 5000 pattern/AM chip
SVT upgrade total: 6M pattern, 40MHz

AMchip04 ~65nm technology, std cell & full custom, 100MHz
Power/pattern/MHz ~30 times less. Pattern density x12.
First variable resolution implementation!
F. Alberti et al 2013 JINST 8 C01040, doi:10.1088/1748-0221/8/01/C01040
AMCHIP04: VARIABLE RESOLUTION

A new “Variable Resolution Associative Memory” for High Energy Physics

doi:10.1109/ANIMMA.2011.6172856

<table>
<thead>
<tr>
<th>Fixed resolution</th>
<th>Variable resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 pattern</td>
<td>1 pattern</td>
</tr>
<tr>
<td>Low S/N</td>
<td>Good rejection and occupy only one pattern location.</td>
</tr>
<tr>
<td>Volume: Thin x 2^7</td>
<td>Per-pattern choice of optimal resolution.</td>
</tr>
<tr>
<td>3 patterns</td>
<td></td>
</tr>
<tr>
<td>Volume: Thin x 3</td>
<td></td>
</tr>
<tr>
<td>High S/N</td>
<td></td>
</tr>
<tr>
<td>Volume: Thin x 4</td>
<td></td>
</tr>
</tbody>
</table>

Implementes the "don't care" feature: inspired by the Ternary CAMs
- Increases the width of a pattern only when needed (fully programmable)
- Wider patterns can be used in high occupancy regions, smaller patterns in low coverage regions (where the number of trajectories is low, thus reducing the fakes)
- The choice of wider or narrower width patterns is made layer by layer with simulation

Equivalent to ~5x patterns → 1/5 HW size
**FTK efficiency: TP → TDR**

Several improvements since TP. The dominant one for FTK efficiency is:

A new “Variable Resolution Associative Memory” for High Energy Physics

doi:10.1109/ANIMMA.2011.6172856


---

**FTK Technical Proposal (fixed size AM)**

- **Coverage**
- **Efficiency**

Pattern size: 24x20x36

- # Roads$> = 167k*8$
- @ $3*10^{34}$ (~70 pile up)

---

**FTK TDR: with “variable resolution AM”**

Pattern size: 15x16x36

Variable resolution bits:

- Pixel 2/layer
- Strip 1/layer

- # Roads$> = 40k*8$
- @ $3*10^{34}$ (~70 pile up)
**Track fitting** – high quality helix parameters and $\chi^2$

- Over a narrow region in the detector, equations linear in the local silicon hit coordinates give resolution nearly as good as a time-consuming helical fit.

$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

- $p_i$'s are the helix parameters and $\chi^2$ components.
- $x_j$'s are the hit coordinates in the silicon layers.
- $a_{ij}$ & $b_i$ are prestored constants determined from full simulation or real data tracks.
- The range of the linear fit is a “sector” which consists of a single silicon module in each detector layer.
- This is VERY fast in FPGA DSPs.
P. Giannetti
Transceivers

Transmission of 32 bit words.

**Input 1:**
- $4 \times 4$ Gbps QSFP from DF (Pix/SCT Hits)
- $8 \times 2$ Gbps to AMB (SSIDs)
- $8 \times 6$ Gbps to Processor 1 (Hits/SSIDs)

**Input 2:**
- $4 \times 4$ Gbps QSFP from DF (SCT Hits)
- $4 \times 2$ Gbps to AMB (SSIDs)
- $4 \times 6$ Gbps to Processor 1 (Hits/SSIDs)
- $4 \times 2$ Gbps from Processors (Tracks)
- $1 \times 2$ Gbps SFP to SSB (Tracks)

**Processors**
- $12 \times 6$ Gbps between processors (Hits/SSIDs)
- $1 \times 2$ Gbps to Input 2 (Tracks)
- $4 \times 2$ Gbps from AMB (Roads)