ALICE upgrade overview

A. Kluge, March 18, 2014
For the ALICE collaboration
Outline

• Upgrade specifications

• Upgrade overview

• Upgrade architecture

• Slides taken from:
  H. Äppelshauser, J-P. Cachemiche, A. Kluge, G. Martinez,
  P. Moreira, L. Musa, W. Riegler, W. Trzaska
Upgrade strategy

- High precision measurements of rare probes at low $p_t$
- Cannot be selected with a trigger
- Require a large sample of events recorded
- Target
  - Pb-Pb $\rightarrow \geq 10 \text{ nb}^{-1} \rightarrow 8 \times 10^{10}$ events
  - pp (@5.5 TeV) $\rightarrow \geq 6 \text{ pb}^{-1} \rightarrow 1.4 \times 10^{11}$ events
- Gain factor 100 in statistics
Upgrade strategy

• Upgrade ALICE read-out and online systems

  • Read-out all Pb-Pb interactions at
    • 50 kHz (L = 6 x 10^{27} \text{ cm}^{-1}\text{s}^{-1}) with min bias trigger

  • Online data reduction \iff no filtering
    • Reconstruction of clusters and tracks

• Improve vertexing and tracking at low $p_t$
  • New inner tracking system

Upgrade in LS2 2018/19
Inner tracking system
New ITS Layout

η coverage: |η| ≤1.5
r coverage: 22 – 400 mm

Pointing Resolution

Tracking efficiency

Mean X/X₀ = 0.282%
Total weight 1.4 grams

Total weight 1.4 grams

8 layers of MAPS
25 G-pixel camera (~10 m²)

ALICE
Current ITS, Z (Pb-Pb data, 2011)
Upgraded ITS, Z
Current ITS, r (Pb-Pb data, 2011)
Upgraded ITS, r

Efficiency (%)

0 20 40 60 80 100

0 50 100 150 200 250 300 350 400

10⁻¹ 1 10
p_T (GeV/c)

ALICE
Current ITS
Upgraded ITS

= 0.8%
0 = 0.3%; OB: X/X₀
IB: X/X₀

Space Frame
Cold Plate
9 Pixel Chips
Soldering Balls
Flex Printed Circuit

Cooling Ducts
Mechanical Connector

1.4 grams

Efficacy (%)
Monolithic PIXEL chip using Tower/Jazz 0.18 µm technology

- feature size 180 nm
- gate oxide < 4 nm
- metal layers 6
- high resistivity epi-layer
  - thickness 18-40 µm
  - resistivity 1-6 k Ω×cm
- “special” deep p-well layer to shield PMOS transistors (allows in-pixel truly CMOS circuitry)
- Several prototype architectures
  - ALPIDE self-triggered or global shutter
  - MISTRAL/ASTRAL rolling shutter

Power density < 50 mW/cm²
New ITS – pixel prototype chips & experimental results

**ALPIDE**

pALPIDE: sizeable prototype of final chip (digital output)  
Explorer: prototype chip with analogue output

Measurements at DESY test beam (4.4 Gev electron beam) – Sep 2013

**Explorer chip**, performance of pixel chip  
from analogue output, pixel size: 20 x 20 μm²

**pALPIDE chip**, performance of pixel chip  
from digital output, pixel size: 22 x 22 μm²

Threshold / Noise: 20

Detection efficiency: 99.7%

Fake hit rate < 10⁻⁸

Spatial resolution ~ 5μm
Readout – general scheme and data throughput

Schematic representation of the readout path

- PIXEL chips
- FLEX
- power regulator
- 4 m
- 9(8) x e-link PWR cables
- patch panel
- readout unit
- data link (DDL)
- trigger link

SAMTEC twinax “Firefly”

On detector

- 1 Mrad
- $10^{13}$ 1 MeV $n_{eq}$

- 10 krad
- $10^{10}$ 1 MeV $n_{eq}$

Off detector (~200 m)

Central Trigger Processor

Data Acquisition & Online Processing

Detector Control System

no radiation

ITS Module

ITS Module

ITS Module

- Readout Control Unit

electrical (1 Gbit/s)

Trigger and CLK (GBT)

Data and Control (GBT)
TPC upgrade

Replace wire chambers
With quadruple-GEM chambers

Exploded view of a GEM IROC
TPC-present limitation & upgrade

- drift time (electrons) = 100 µs
- after gating grid closed until 280 µs
  - to prevent back drifting ions into drift region
  - and space charge distortion
- → total time 280 µs → 3.5 kHz read-out rate
- avg. interaction rate 50 kHz → 20 µs
- drift time = 100 µs →
- pile-up → continuous trigger-less read-out
multiple GEM principle

- Fast electron signal (polarity!)
- no “ion tail”
- No “coupling to other electrodes”
  → Gas gain about a factor 3 lower than in MWPC

GEMs are made of a copper-kapton-copper sandwich, with holes etched into it

Electron microscope photograph of a GEM foil
4 GEM simulation
TPC front-end card

- ~ 500,000 channels @ 50 kHz read-out rate
- 3400 front-end cards & ~ 17,000 SAMPA ASICs
Muon Forward Tracker - MFT
Silicon pixel tracker in acceptance of Muon Spectrometer between Interaction Point and Hadron Absorber
Extrapolating back to the vertex region degrades the information on the kinematics.
Muon tracks are extrapolated and “matched” to the MFT clusters before the absorber.

High pointing accuracy gained by the muon tracks after matching with the MFT clusters.
• Based on MAPS: common development with ITS
• Read-out based on GBT links
Muon chambers - MCH
Muon chamber

- ~1,000,000 MWPC
- Upgrade to continuous read-out @ 100 kHz hit rate
- Replacement of the front-end by ~ 33,000 SAMPA ASIC
- Replacement of active patch panels (first level of data concentration)
  - Based on GBTs or electrical e-links
- Replacement of data concentrator by CRUs
muon chamber

1 slat

**FEE board**
(each e-link bus
= 3 differential lines
(6 wires))

**E-link bus**

GBTX card

Non-Bending cathode
Bending cathode

40 inputs
80 Mb/s

detector
cavern

GBT link
Optical fiber

CRU

DAQ
HLT

DDL 3
10 Gb/s

Control room
Fast interaction trigger
Fast interaction trigger - FIT
Fast interaction trigger - FIT

Photonis PLANACON® XP85012 or XP85112
Read-out & Trigger
Upgrade architecture
Specifications

• **Interaction rate Pb-Pb:**
  • from 8 kHz → 50 kHz

• **Trigger rate Pb-Pb:**
  • from ~3.5 kHz → 50 kHz

• **All interactions are read AND recorded**

• **Interaction and trigger rate pp:**
  • → 200 kHz

• **Data rate driven by Pb-Pb**

• **TPC is read continuous & trigger less**
Run1 and Run2 architecture

- On-detector electronics
- Front-end links
- Detector specific RO system
- DDL1 or 2
- DAQ
- TTS & busy

- CTP
- LTU

- TTS.. Trigger and Timing Distribution System
- CTP.. Central Trigger Processor
- LTU.. Local Trigger Unit

TOV0, ZDC, ACO, TOF, EMC, PHO, SPD

March 18, 2014
A. Kluge
37
Common read-out unit - CRU & long trigger latency

CRU, common read-out unit
O², Online and Offline Computing System
DCS, Detector Control System
TTS, Trigger and Timing Distribution System
CTP, Central Trigger Processor
LTU, Local Trigger Unit
GBT, Gigabit Transceiver

On-detector electronics

CTP

FIT ZDC ACO TOF EMC PHO

LTU

TRG Dist

CRU CRU CRU CRU

O² & DCS

TTS-GBT & busy
(MCH, MID, ITS*, TPC, TRD)

CRU system with TTS link to CRU
(MCH, MID, TPC)

DDL3

→data &
←configuration

→data &
←trigger &
←configuration

front-end links (GBT)
Common read-out unit - CRU & & short trigger latency

CTP

FIT ZDC ACO TOF EMC PHO

LTU

On-detector electronics

TTS & busy
GBT(ITS*) or TTC (TRD)

front-end links (GBT)
→data & ←configuration

On-detector electronics

*..ITS uses the CRU or connects directly from the on-detector electronics to the O² via DDL3

CRU system with TTS link to FE (ITS*, TRD)

CRU.. common read-out unit
O².. Online and Offline Computing System
DCS.. Detector Control System
TTS.. Trigger and Timing Distribution System
CTP.. Central Trigger Processor
LTU.. Local Trigger Unit
GBT.. Gigabit Transceiver

DDL3 →data & ←configuration

FIT ZDC ACO TOF EMC PHO

LTU

LTU

O² & DCS

CRU

CRU

CRU

CRU

TRG Dist

TRG Dist

TRG Dist

March 18, 2014
Upgrade architecture: det. spec. readout

CTP. Central Trigger Processor
LTU. Local Trigger Unit

FIT, ZDC, ACO, TOF, EMC, PHO

On-detector electronics

Detector specific RO system

TTS, Trigger and Timing Distribution System

O² & DCS

Detector spec. system with TTS based on TTC (HMP, EMC, PHO, ACO) or GBT (TOF, FIT, ITS*)
Upgrade architecture: system components

- **DDL**
  - common
- **Off-detector read-out**
  - common readout unit or custom
- **Front-end links**
  - versatile link (GBT) or custom
- **CTP & LTU & TTS**
  - fast serial trigger link (FTL) & TTC
- **On-detector electronics**
  - SAMPA & custom
Common components

Common Readout Unit – CRU & Detector Data Link - DDL
Read-out architecture

- **Standard interface to DAQ/DCS**
  - Detector Data Links DDL 1, 2 already developed
    - 2.125 and 4.25/5.3125 Gb/s
  - DDL3 based on commercial standard
    - 10 Gb/s GbE or PCIe over cable or PCIe plug-in cards

- **Standard interface to Trigger**
Common readout unit (CRU)

- CTP → LTU
- CRU
- front-end links
- trigger link & busy
- DDL → O²

On detector elec.

- CRU
- FGPA
- memory
- memory
- high speed electrical back plane

- 12 opt. in
- 12 opt. in
- 12 opt. out
- 12 opt. out
- 12 opt. in
- 12 opt. in
- 12 opt. out
- 12 opt. out

- DDL3 0-11
- O² & DCS

CRU: common read-out unit
O²: Online and Offline Computing System
DCS: Detector Control System
TTS: Trigger and Timing Distribution System
Common readout unit (CRU)

CRU.. common read-out unit
O^2.. Online and Offline Computing System
DCS.. Detector Control System
TTS.. Trigger and Timing Distribution System
CTP.. Central Trigger Processor
LTU.. Local Trigger Unit
GBT.. Gigabit Transceiver

FIT
ZDC
ACO
TOF
EMC
PHO

CTP

LTU

TTS-GBT & busy
(MCH, MID, ITS*, TPC, TRD)

TRG Dist

CRU

CRU

CRU

CRU

On-detector electronics

front-end links (GBT)

CRU system with TTS link to CRU
(MCH, MID, TPC)

Trigger & busy distribution

DDL3

O^2

&

DCS
Common readout unit (CRU)

AMC40

- AMC40 (LHCb)

Jean-Pierre Cachemiche
Common readout unit (CRU)

- 4 x AMC40
- 1 x motherboard → 14 motherboards → 1 ATCA crate
- Trigger and timing distribution is via back plane
Common components

Front-end (FE) links & Trigger and Timing Distribution System (TTS) Links
Common components

**Front-end (FE) links & Trigger and Timing Distribution System (TTS) Links**
GBT & Versatile link

On-Detector
Radiation Hard Electronics

Off-Detector
Commercial Off-The-Shelf (COTS)

Timing & Trigger
DAQ
Slow Control

Custom ASICs

GBTX

GBTIA

GBLD

PD

LD

FPGA
GBTx

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**FE Module**

**Phase - Aligners + Ser/Des for E - Ports**

**E - Port**

**E - Port**

**E - Port**

**E - Port**

---

**GBTX**

**Phase - Shifter**

**CLK Reference/xPLL**

**I2C Master**

**I2C Slave**

**Configuration (e-Fuses + reg-Bank)**

**Control Logic**

**ePL**

**LITX**

**ePL**

**ePCR**

**DEC/DSRCR**

**CVR**

**SER**

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**I2C (light)**

**JTAG Port**

**I2C Port**

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**External clock reference**

**Clock[7:0]**

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**GBTIA**

**GBLD**

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**data-up**

**data-down**

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80, 160 and 320 Mb/s ports

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One 80 Mb/s port

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**Control Logic**

Configuration (e-Fuses + reg-Bank)

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**I2C Slave**

---

**JTAG**

---

**I2C Master**

---

**I2C (light)**

---

**I2C Port**

**I2C Port**

---

**GBTX**

---

**GBTX**

---
GBT-SCA: slow control adapter

Timing & Trigger
DAQ Path

GBT

Slow Control

GBT

DAQ Path
Timing & Trigger

User Buses:
- I2C
- Parallel bus
- JTAG
- Memory
- Monitoring 12b ADC
- Experiment Specific Protocol
Versatile link components: VTTx & VTRx

**Singlemode EEL/InGaAs**

- **VTRx**
  - PCB
  - edge-connector
  - GBLD
  - Laser Diode
  - PIN + GBTIA
- **TOSA**
- Optical Fibre and Connectors
- **TRx (SFP+)**

**Multimode VCSEL/GaAs**

- **VTTx**
  - PCB
  - edge-connector
  - GBLD
  - Laser Diode
  - Laser Diode
- **TOSA**
- **DRx12**

50-150m

On-Detector Radiation zone

Off-Detector Radiation-free zone
Versatile link components: VTTx & VTRx
CTP.. Central trigger processor  
CRU.. Common read-out unit  
O².. Online and offline computing system  
TTS.. Trigger and timing distribution system  
DCS.. Detector control System  
VTRx .. Optical transmitter/receiver  
VTTx .. Double optical transmitter  
GBTx .. GBT transmitter receiver ASIC  
SCA.. Slow control adapter ASIC  

Diagram:

- FE  
- SCA  
- GBTx  
- VTRx  
- VTTx  
- CTP  

- Control  
- E-links  
- FE-link  
- TTS-FE & control ink  
- Cavern  
- Control room  
- DDL3  
- O² & DCS
### Links

<table>
<thead>
<tr>
<th>Detector</th>
<th>DDL1 2.125 Gb/s</th>
<th>DDL2 4.25-5.3125 Gb/s</th>
<th>DDL3 10Gb/s</th>
<th>CRU-FE-links 3.2 Gb/s</th>
<th>TTS-FE links 3.2 Gb/s</th>
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<tbody>
<tr>
<td>TPC</td>
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<td>500</td>
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<td>500</td>
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<td>*184</td>
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<td><strong>110</strong></td>
<td><strong>1555</strong></td>
<td><strong>8081</strong></td>
<td><strong>2244</strong></td>
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</table>
Common components

Central Trigger Processor (CTP) & Local Trigger Processor (LTU)
CTP & LTU: based on high performance FPGA processor

Logic combinations fully programmable

CTP & LTU

- CTP: Central Trigger Processor
- LTU: Local Trigger Unit
- GBT: Gigabit Transceiver
- TTC: Trigger and Timing Distribution System
- CRU: common read-out unit
- O²: Online and Offline Computing System
- DCS: Detector Control System

*ITS uses the CRU or connects directly from the on-detector electronics to the O² via DDL3
**System description: Trigger signals**

<table>
<thead>
<tr>
<th>Level</th>
<th>Trigger Input to CTP [ns]</th>
<th>Trigger Output at CTP [ns]</th>
<th>Trigger Decision at detector [ns]</th>
<th>Contributing detectors</th>
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<td>LM</td>
<td>425</td>
<td>525</td>
<td>775</td>
<td>FIT</td>
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<td>L0</td>
<td>1200</td>
<td>1300</td>
<td>1500</td>
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<td>L1</td>
<td>#6100</td>
<td>#6200</td>
<td>#6400</td>
<td>EMC, ZDC</td>
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</table>

- LM .. pretrigger wake up signal for TRD: by FIT only
- L0 .. main trigger signal: by FIT & additional trigger inputs
- L1 .. optional EMC-jet and ZDC contribution: long latency
Common TPC/MCH readout ASIC
SAMPA

- common read-out ASIC
- TPC & muon chambers
• SAMPA is evolution from PASA / ALTRO & S-ALTRO
• Analog specifications are almost identical
SAMPA

- **TPC & muon chambers (MCH)**
  - 32 channel amplifier-shaper-ADC-DSP
  - triggerless/continuous & triggered readout
  - < 600 e @ 25 pF (TPC), < 950 e @ 40 p (MCH)
  - bi-polarity input
  - 10 bit ADC – 10/20 Msamples/s
  - on ASIC base-line correction and zero suppression
  - 4 x 320 Mbit/s serial outputs
  - 130 nm TSMC CMOS process
Detector Summary
<table>
<thead>
<tr>
<th>Det</th>
<th>triggered by</th>
<th>Pb-Pb RO rate [kHz]</th>
<th>TTS</th>
<th>CRU used</th>
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<td>TPC</td>
<td>(L0 or L1)</td>
<td>50</td>
<td>FTL</td>
<td>y</td>
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<tr>
<td>MCH</td>
<td>(L0 or L1)</td>
<td>100</td>
<td>FTL</td>
<td>y</td>
</tr>
<tr>
<td>ITS</td>
<td>L0</td>
<td>100</td>
<td>FTL</td>
<td>*y</td>
</tr>
<tr>
<td>MID</td>
<td>L0 or L1</td>
<td>&gt;100</td>
<td>FTL</td>
<td>y</td>
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<td>y</td>
</tr>
<tr>
<td>TOF</td>
<td>L0 or L1</td>
<td>&gt;100</td>
<td>FTL</td>
<td>n</td>
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<tr>
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<td>L0 or L1</td>
<td>100</td>
<td>FTL</td>
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<td>ACO</td>
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<td>TRD</td>
<td>LM&amp;(L0 or L1)</td>
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<td>FTL&amp;TTC</td>
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<td>EMC</td>
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<td>TTC</td>
<td>n</td>
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<tr>
<td>PHO</td>
<td>#L0&amp;L1</td>
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<td>TTC</td>
<td>n</td>
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<td>HMP</td>
<td>#L0&amp;L1</td>
<td>2.5</td>
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## Sub-detector upgrade effort

<table>
<thead>
<tr>
<th>Det</th>
<th># channels</th>
<th>Run1&amp;2 RO rate [kHz]</th>
<th>upgrade RO rate [kHz]</th>
<th>FE ASIC</th>
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<th>ROC</th>
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<td>TOF</td>
<td>$1.6 \times 10^5$</td>
<td>40</td>
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<td>72 DRM</td>
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<td>upgrade DRM(TOF)</td>
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<tr>
<td>PHO</td>
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<tr>
<td>HMP</td>
<td>$1.6 \times 10^5$</td>
<td>2.5</td>
<td>2.5</td>
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</table>
Summary

• Rate upgrade: 50 kHz
• New ITS & MFT
• TPC GEMs & continuous, trigger-less read-out
• Muon system electronics upgraded
• Common component approach widened
Radiation Levels
**Radiation levels**

<table>
<thead>
<tr>
<th>Element</th>
<th>r (cm)</th>
<th>z (cm)</th>
<th>TID (krad)</th>
<th>1 MeV neq (cm(^{-2}))</th>
<th>&gt;20 MeV had. (kHz/cm(^2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITS L0</td>
<td>2.2</td>
<td>[-13.5, 13.5]</td>
<td>646</td>
<td>9.2 × 10(^{12})</td>
<td>1600</td>
</tr>
<tr>
<td>ITS L1</td>
<td>2.8</td>
<td>[-13.5, 13.5]</td>
<td>387</td>
<td>6.0 × 10(^{12})</td>
<td>1000</td>
</tr>
<tr>
<td>ITS L2</td>
<td>3.6</td>
<td>[-13.5, 13.5]</td>
<td>216</td>
<td>3.8 × 10(^{12})</td>
<td>500</td>
</tr>
<tr>
<td>ITS L3</td>
<td>20</td>
<td>[-42.1, 42.1]</td>
<td>13</td>
<td>5.2 × 10(^{11})</td>
<td>28</td>
</tr>
<tr>
<td>ITS L4</td>
<td>22</td>
<td>[-42.1, 42.1]</td>
<td>9</td>
<td>5.0 × 10(^{11})</td>
<td>24</td>
</tr>
<tr>
<td>ITS L5</td>
<td>41</td>
<td>[-73.7, 73.7]</td>
<td>6</td>
<td>4.6 × 10(^{11})</td>
<td>10</td>
</tr>
<tr>
<td>ITS L6</td>
<td>43</td>
<td>[-73.7, 73.7]</td>
<td>4</td>
<td>4.6 × 10(^{11})</td>
<td>9</td>
</tr>
<tr>
<td>MFT D0</td>
<td>2.5</td>
<td>-50</td>
<td>395</td>
<td>6.7 × 10(^{12})</td>
<td>1100</td>
</tr>
<tr>
<td>MFT D1</td>
<td>2.5</td>
<td>-58</td>
<td>392</td>
<td>6.4 × 10(^{12})</td>
<td>1040</td>
</tr>
<tr>
<td>MFT D2</td>
<td>3.0</td>
<td>-66</td>
<td>767</td>
<td>5.9 × 10(^{12})</td>
<td>760</td>
</tr>
<tr>
<td>MFT D3</td>
<td>3.5</td>
<td>-72</td>
<td>427</td>
<td>4.3 × 10(^{12})</td>
<td>520</td>
</tr>
<tr>
<td>MFT D4</td>
<td>3.5</td>
<td>-76</td>
<td>541</td>
<td>4.8 × 10(^{12})</td>
<td>560</td>
</tr>
<tr>
<td>FIT1</td>
<td>5</td>
<td>-80</td>
<td>181</td>
<td>3.0 × 10(^{12})</td>
<td>280</td>
</tr>
<tr>
<td>FIT2</td>
<td>5</td>
<td>340</td>
<td>103</td>
<td>1.4 × 10(^{12})</td>
<td>200</td>
</tr>
<tr>
<td>TPC In</td>
<td>79</td>
<td>[-260, 260]</td>
<td>2.1</td>
<td>3.4 × 10(^{11})</td>
<td>3.4</td>
</tr>
<tr>
<td>TPC Out</td>
<td>258</td>
<td>[-260, 260]</td>
<td>0.3</td>
<td>5.2 × 10(^{10})</td>
<td>0.7</td>
</tr>
<tr>
<td>TRD</td>
<td>290</td>
<td>[-390, 390]</td>
<td>0.4</td>
<td>4.8 × 10(^{10})</td>
<td>0.54</td>
</tr>
<tr>
<td>TOF</td>
<td>370</td>
<td>[-370, 370]</td>
<td>0.13</td>
<td>2.6 × 10(^{10})</td>
<td>0.26</td>
</tr>
<tr>
<td>EMCAL</td>
<td>430</td>
<td>[-340, 340]</td>
<td>0.06</td>
<td>1.5 × 10(^{10})</td>
<td>0.02</td>
</tr>
<tr>
<td>MCH S1</td>
<td>19</td>
<td>-536</td>
<td>0.42</td>
<td>4.2 × 10(^{11})</td>
<td>3</td>
</tr>
<tr>
<td>MCH S2</td>
<td>24</td>
<td>-686</td>
<td>0.19</td>
<td>1.4 × 10(^{11})</td>
<td>1</td>
</tr>
<tr>
<td>MCH S3</td>
<td>34</td>
<td>-983</td>
<td>0.14</td>
<td>1.6 × 10(^{11})</td>
<td>0.9</td>
</tr>
<tr>
<td>MCH S4</td>
<td>45</td>
<td>-1292</td>
<td>0.18</td>
<td>3.0 × 10(^{11})</td>
<td>1</td>
</tr>
<tr>
<td>MCH S5</td>
<td>50</td>
<td>-1422</td>
<td>0.91</td>
<td>2.5 × 10(^{11})</td>
<td>0.7</td>
</tr>
<tr>
<td>CTP Rack</td>
<td>600</td>
<td>-1295</td>
<td>4.8 × 10(^{-3})</td>
<td>7.8 × 10(^{9})</td>
<td>0.03</td>
</tr>
</tbody>
</table>

**Table 3.1:** Total Ionizing Dose (TID) and 1 MeV neq hadron fluence for 10nb\(^{-1}\) PbPb + 6pb\(^{-1}\) pp + 50nb\(^{-1}\) pPb collisions (including a safety factor 10) as well as high energy hadron fluence for 50kHz PbPb collisions (including a safety factor 2).
Radiation

Dose (krad)

R (cm)

Z (cm)

10^2
10
10^{-1}
10^{-2}
10^{-3}

1
0.1

100
50
0
-400
-300
-200
-100
100
200
300
400
Radiation

1 MeV Neutron Equivalent hadron fluence (cm\(^{-2}\))
High-energetic ($E_{\text{kin}} > 20$ MeV) hadron fluence rate (kHz/cm$^2$)
Detector Summary
Muon identifier

- 21,000 channels (RPC)
- replacement of front-end electronics to slow down aging speed of RPCs
  - by operation in avalanche mode reducing charge produced in the gas
- Front-end ASIC is replaced by FEERIC ASIC
  - with amplification
- Readout out at 100 kHz @ 0 % busy
Muon identifier

- Replacement of 2 levels of data concentrators by 234 new front-end cards and CRUs
- Small scale system with FEERIC will be tested already in run 2
Muon identifier

LOCAL/REGIONAL

128 FE

LVDS buff

e-link bidir buff

+ CERN IP e-link

Trig

+ ACQ

FPGA

def contr

CERN IP optic

2 GBT

GBT@3.2Gb/s

local-μtrig

e-link@320Mb/s

REGIONAL with 128 LVDS inputs, 17 e-link@320Mb/s, 2 GBT, 2 GBT links @3.2Gb/s, 1 FPGA, 1 LVDS output

LOCAL/REGIONAL

LVDS buff

e-link bidir buff

+ CERN IP e-link

Trig

+ ACQ

FPGA

def contr

CERN IP optic

2 GBT

GBT@3.2Gb/s

regional-μtrig

e-link@320Mb/s

CRU

FPGA

Trig

+ CERN IP TDS

Busy?

DDL3

CERN IP DDL

def contr

CERN IP optic

CERN IP GBT

CRU with 32 GBT links @3.2Gb/s, 1 big FPGA, 1 TDS, CDH builder, 1 DDL3

Data MUX

DDL 3

FE-ASIC

FEC

Sensor
• 1.151.000 channels
• rate upgrade from 8 kHz to 50 kHz with 23 % busy
• triggered operation (LM & L0)
• FE electronics unchanged, but data load reduced with firmware change
  • pre-processed data (tracklets) are transferred only or
  • partial read-out based on electron region candidates
• Data MUX is CRU
TOF

- ~160,000 MRPC pads
- rate upgrade from 10s of kHz to 100 kHz PbPb without dead time
  - max limit by HPTDC in FEC is 265 kHz
  - rate limit comes from VME based read-out and data format
- upgrade firmware for data format and VME protocol
- replace 72 2\textsuperscript{nd} level data concentrator boards (DRM)
TOF

Sensor → FE-ASIC → FEC → Data MUX → DDL 2

Diagram:
- HPTDC
- LTM
- TRM
- CTM
- DRM2
- CTP
- O²

32 bit parallel bus
2 token-rings with 15 chips

160 MB/s bi-directional GBT link

hardware upgrade
firmware upgrades

March 18, 2014
A. Kluge
85
Detector developments: ITS

- 25 G pixels
- complete new detector
  - ASIC, sensor, read-out, mechanics cooling
- triggered @ L0
- Detector module sends data 1 Gb/s links
  - base-line electrical
  - close to detector link interface needed
Detector developments: FIT

- **160 MCP-PMT +**
- **64 Scintillators**
- Provides interaction trigger
- timing reference for TOF
- multiplicity measurement
- New detector implementation
  - new front-end
  - RO based on TOF read-out scheme
Detector developments: ZDC

- 22 channels
- outside of radiation zone
- use NIM, VME and commercial electronics
- provides timing trigger
- upgrade from 8 kHz to 16 kHz by introduction of multi-event buffers in firmware (run 2)
- to 100 kHz without dead time
  - commercial digitizers with on board FPGAs
  - TDC model firmware upgrade
  - replacement of data concentrator card (ZRC) and
  - use CRU
Detector developments: EMC

- ~ 18,000 channels
- provides trigger
  - L0 input: sum
  - L1 input: shower and jet
- has already been upgraded to 46 kHz @ 15% busy
  - front end (ALTRO) limits to 50 kHz
  - data reduction by on-line data evaluation
  - replacement of data concentrators by SRU (Scalable Read-out Unit, RD51)
Detector developments: PHO

- ~ 17,000 channels
- provides trigger
  - L0 input: sum
- taking same approach as EMC to 46 kHz @ with busy time
  - front end (ALTRO) limits to 50 kHz
  - data reduction sample number reduction
  - replacement of data concentrators by SRU (Scalable Read-out Unit, RD51)
  - replacement of trigger region units (TRU)
Detector developments: HMP

- ~160,000 channels MWPC
- RO rate to 2,5 kHz
- No detector/electronics change