LHCb Upgrade

Electronics Status & Outlook

on behalf of the LHCb collaboration
Outline

Upgrade philosophy
Electronics Architecture
Review of electronics R&D
LHCb today

~ 3 fb$^{-1}$ collected before LS1

VeLo Si strips

‘Inner’ Tracker Si strips

Outer Tracker Straws Tubes

Muon MWPC

RICH HPDs

Calo PMTs
Existing readout system

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bunch crossing rate</td>
<td>40 MHz *</td>
</tr>
<tr>
<td>L0 trigger rate</td>
<td>1 MHz average</td>
</tr>
<tr>
<td>L0 trigger latency</td>
<td>4 μs fixed (160 BXs)</td>
</tr>
<tr>
<td>Event readout time</td>
<td>900 ns</td>
</tr>
<tr>
<td>Event rate to DAQ</td>
<td>1 MHz</td>
</tr>
</tbody>
</table>

---

**L0 electronics**
- L0 Latency buffer
- L0 derandomiser
- L0 trigger

**L1 electronics**
- Input buffer
- Zero Suppress
- Formatting
- GB Ethernet to DAQ

**Hence**
- Muons
- Calorimeter
Upgrade architecture

No ‘front-end’ trigger, Event rate to DAQ nominally 40 MHz

Current

Upgrade

50 Tb/s
Can we do it?

……. actually, can we afford it?

Trends in high speed optical data transmission

1Gbit/s  10Gbit/s  40Gbit/s

….. and strong programme for rad-tolerance

….. and trends in embedded links in FPGAs

Upgrade installation in LS2
Architectural choices

Data compression on front-end driven by cost:

- no compression ~ 80,000 links (4.8 Gb/s) 20 MCHF
- compression ~ 12,500 links (cf 8,000 today) 3.1 MCHF

NB: Compression (zero-suppression) currently done in off-detector FPGAs:

careful balance of complexity vs robustness
needed a few iterations get it right!

=> Aim for flexibility + scale-ability in upgrade
Architectural choices

New compact link offers combined Data, TFC, ECS

Need UP bandwidth >> DOWN bandwidth
=> Combine TFC+ECS; Separate Data

TFC
ECS
Data

UP 4.8 Gb/s

TFC
ECS
Data

DOWN 4.8 Gb/s

TFC
ECS
Data
LHCb tomorrow

VeLo Si pixels

Upstream Tracker Si strips

Downstream Tracker Sci-Fibres

Muon MWPC

RICH MAPMTs

Calo PMTs
Review of electronics R&D
(non-exhaustive)
VeLo (Si pixels)

26 planes of sensor tiles
5.1mm to beam

FE Electronics in VeloPIX chip:
55 μm pixels, 256 x 256 array
130 nm CMOS
Binary readout
Development of TimePIX3
Matrix = 128 x 64 super-pixels

Data packet

Hottest chip: 16 Gbit/s of data

Four serialisers per chip @ 5.12 Gbit/s
Upstream Tracker (Si strips)

4 planes of 16 staves

SALT chip in 130nm CMOS

Prototype 6-bit SAR, 0.35 mW @ 40 MS/s
SciFi Tracker (SiPMs)

Mats of 2.5m, 250μm fibres

SiPM array

PACIFIC chip in 130nm CMOS

Digital processing in FPGA (SRAM or FLASH)

Signals arriving at SiPM
- Top
- Middle
- Bottom

128 channels
RICH (MAPMTs)

4,500 64-channel PMTs

CLARO chip in 0.35 μm

FPGA for digital processing (SRAM)

Low occ. regions => Zero Suppression
High occ. regions => no Zero Suppression
Calorimeter (PMTs)

8000 PMTs

ICECAL chip in 0.35 μm

FPGA for digital processing (FLASH)
Muons (MWPCs)

Re-use front-end ASICs on chambers (CARIOCA + DIALOG)

New ‘Off-detector’ cards with new chip nSYNC
Detector Links, optical: 4.8 Gbit/s

Generic Link: GBT chips + Versatile Link + commercial components

Duplex Master Control Link (2,500)

Simplex Data Link (12,500)

Ken Wyllie, CERN
GOAL: Generic FPGA-based hardware for many tasks:

- TELL40 for Data
- SOL40 for ECS/TFC
- TRIG40 for LLT

Each with different firmware flavours

1st developments focussed on ATCA + AMC

R&D close to completion

Small production made for lab systems
Example: TELL40

- 24 inputs @ 4.8 Gb
- GBT format
- 12 outputs/inputs @ 10Gb ethernet
- 96 inputs @ 4.8 Gb → processing in FPGA → 48 10G ethernet ports
Move to PCIe?

Use PC memory & processors for event building

Choose network interface at last moment (cheapest)
TELL40 firmware

- Project across many groups
- Centrally coordinated
- Common interfaces
- User code for data processing
Long distance transmission?

4.8 Gbit/s
10/40 Gbit/s Ethernet or Infiniband
100 Gbit/s Ethernet or Infiniband

Ken Wyllie, CERN
Long distance transmission?

Short fibre

400m OM4 fibre
All data in a box

sponsored by . . . ?
Conclusions & Outlook

Clear architecture concept with many common items

R&D for sub-detectors is moving well

We rely on new generic developments (GBT, Versatile Link, DC-DC)

Manpower is improving

Aggressive but feasible schedule........
Shift of LS2 helps!
Motivation for upgrade

At $L = 2(+) \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$, beyond 5 fb$^{-1}$, statistics don’t improve much.

Big statistical improvement if:
- increase $L$ to $2 \times 10^{33}$, \textbf{AND}
- improve efficiency of trigger algorithms

\textbf{BUT}..... with current L0 trigger:
rate & latency limited by electronics (1 MHz, 4 $\mu$s) $\rightarrow$ saturation
BUT…. efficient trigger decisions require:

- long latencies (>> 4 μs)
- computational power
- data from many (all) sub-detectors (momentum, impact parameter .....

\[ \Rightarrow \text{Trigger in software} \]
\[ \Rightarrow \text{Use data from every bunch crossing} \]
\[ \Rightarrow \text{Upgrade electronics + DAQ for LS2} \]
Architecture: more detail

Global Experimental Control System (ECS)
Architecture: more detail
Triggering doesn’t completely disappear

40 MHz
Calorimeters
Muon

LLT
\( p_T \) of \( h, \mu, e/\gamma \)

1 – 40 MHz
All detectors information

HLT
tracking and vertexing
\( p_T \) and impact parameter cuts

20 kHz

Hardware

Software
Control & Synchronisation

Control with synchronised fast commands
eg bunch-counter reset

Latencies will be measured => pre-scaling of commands by S-ODIN

Absolute measurement with:
- pulsed laser
- cosmics
- low intensity LHC beam collisions
Can allow a small rate of errors
BUT
No loss of synch

100% robust