ACES 2014

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CMS upgrades overview

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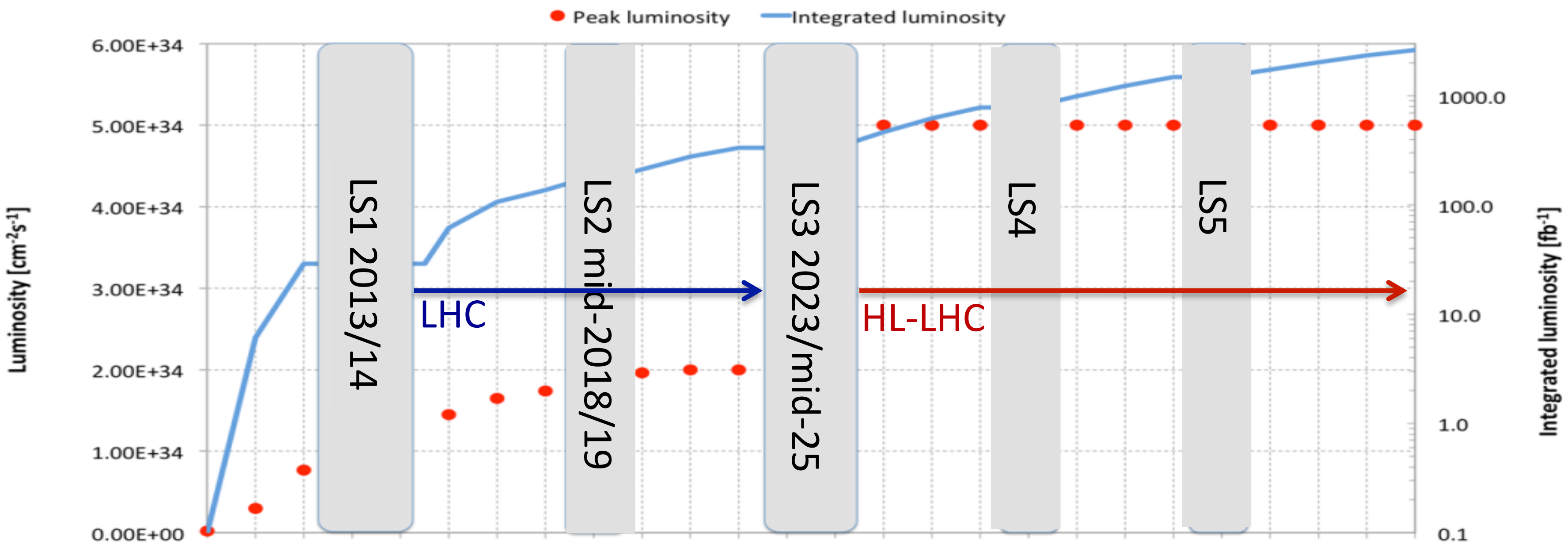
CMS upgrades program

Phase 1: Complete LHC physics program at luminosity up to ≥ 2 x 10^{34} $cm^{-2}s^{-1}$
Prepare for 50 PU, through LS3, with margin up to 70 PU
Detectors can sustain up to 500 fb^{-1}



Phase 2: HL-LHC program for 3000fb^{-1} integrated luminosity
Solve detector aging, high occupancy and radiation hardness issues, target performance at 5 x 10^{34} $cm^{-2}s^{-1}$ (with leveling) for ~125-140 pile-up with operation margin up to ~200 for higher luminosity if performance allows

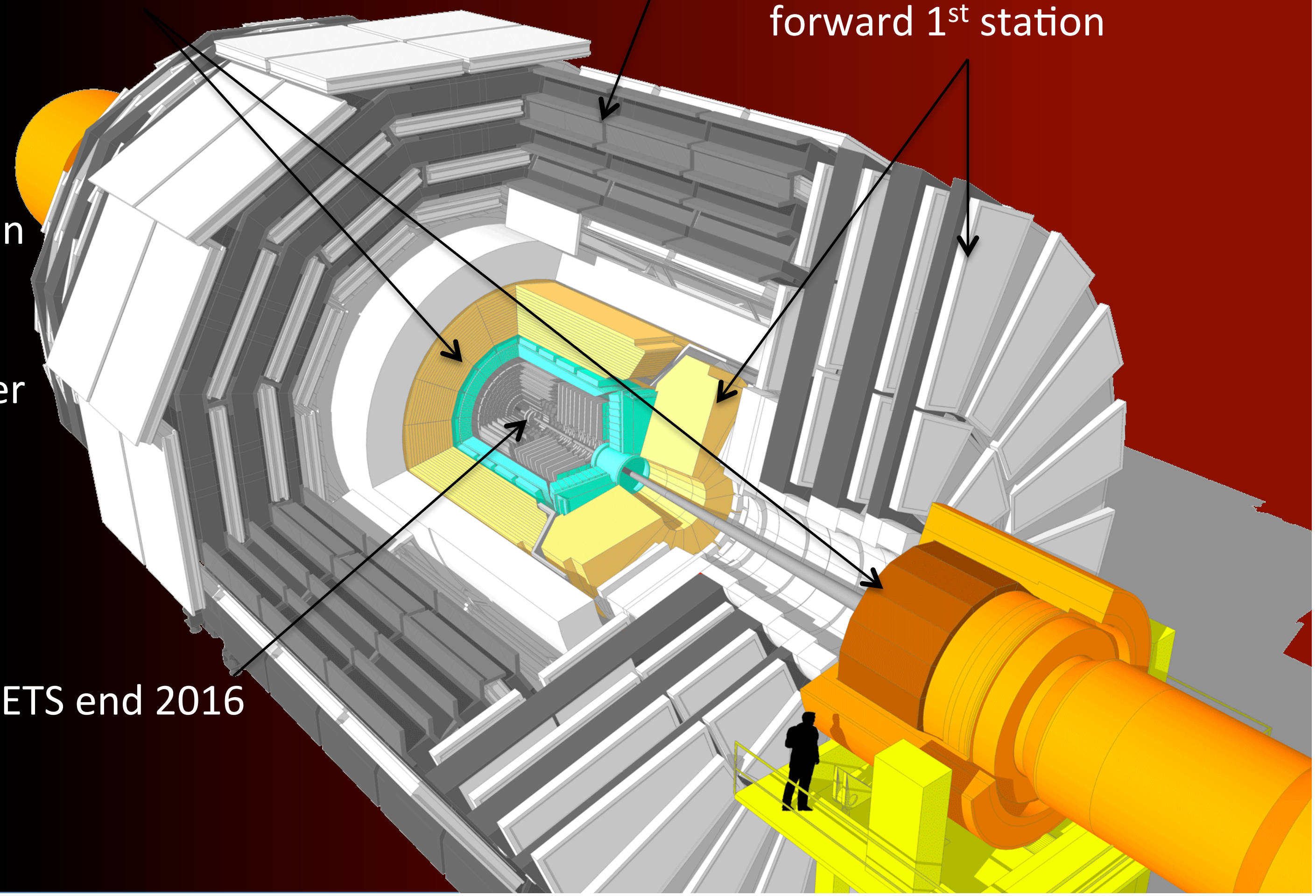
CMS Phase 1 Upgrades

Muons in LS1
- Consolidate DT read-out
- Complete CSC and RPC in forward - 4th station
- Increase granularity in CSC forward 1st station

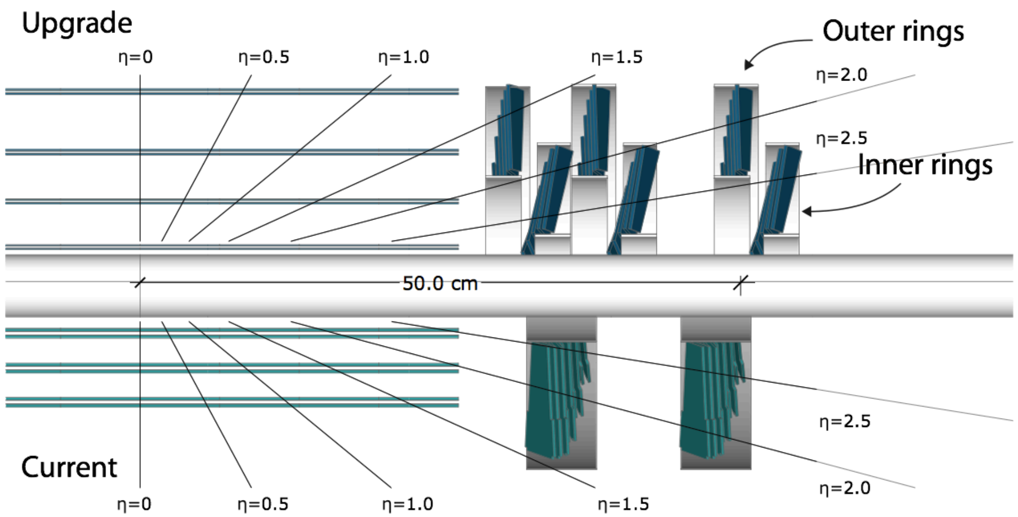
Endcap Calorimeters staged from LS1 to LS2
- New HF and HCAL Frontend and Backend

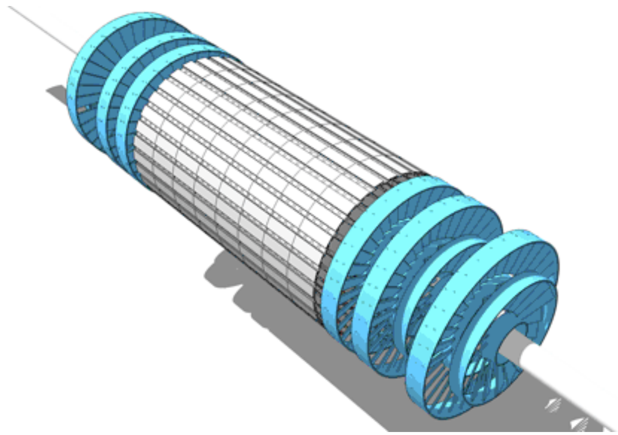
Trigger commissioning in parallel to operation in 2015
- High processing power and bandwidth

New Pixel installed in YETS end 2016

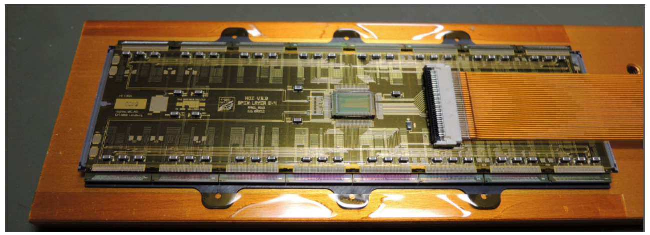


CMS Phase 1 Pixel detector





- **4 layers/3 disks** (1 more space-point - extended range from lower to larger radius)
  - 3 cm to 16 cm radius
- **New readout chip** (no data loss)
  - Tolerate rates up to PU 100
- **Less material:** CO_2 cooling, new cabling & DC/DC powering
  - Weight divided by a factor 2.5 in barrel
- **Similar technology as current detector for sensors and FE chip**
  - Survive Integrated Luminosity of 500 fb^{-1} (5x 10^{15} neq/cm^2) with layer 1 exchange after 250 fb^{-1}



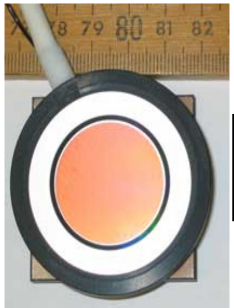
→ Reduced γ conversion - higher efficiency, lower fake rate - improved IP resolution

Pixel TDR http://cds.cern.ch/record/1481838?ln=en

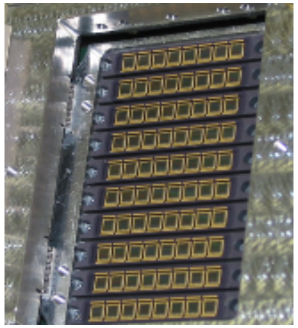
CMS Phase 1 HCAL upgrade

- **New PMTs** multi-anode for HF (3<η<5)
- **Replace HPDs with SiPMs** in HO/HB/HE improved S/N
- **Replace Front-End and BackEnd electronics**
  - ➢ Improved background rejection using timing with new FE chip
  - ➢ Higher granularity allows depth segmentation to access the longitudinal shower development
    - ➢ Improved calibration - improved shower reconstruction for neutral energy, improved isolation in trigger and offline analyses

HPDs

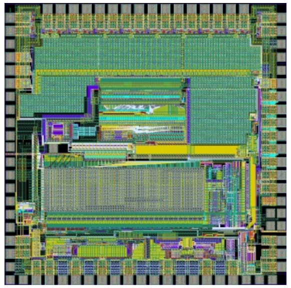


SiPMs

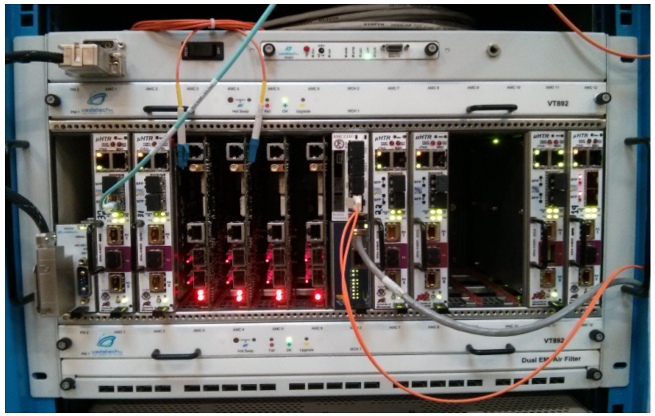


Single to dual readout PMTs

QIE10 (HF)
QIE11 (HBHE)



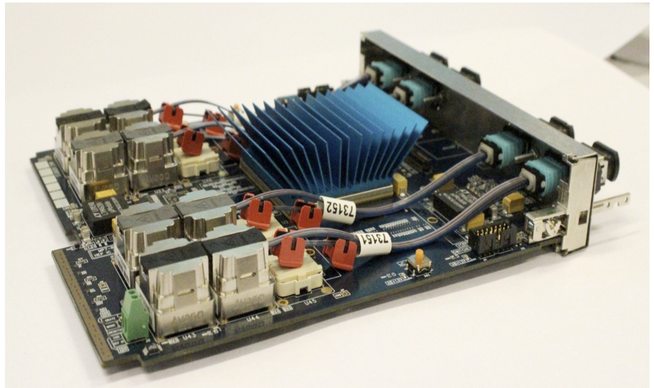
New µTCA Back-end



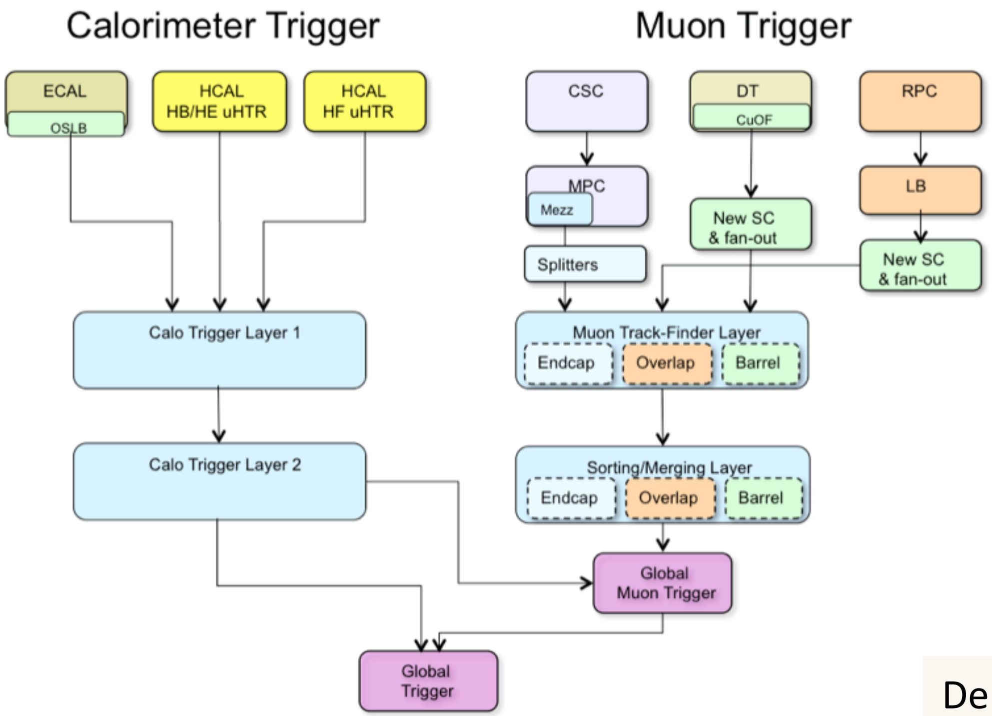
HCAL TDR http://cds.cern.ch/record/1481837?ln=en

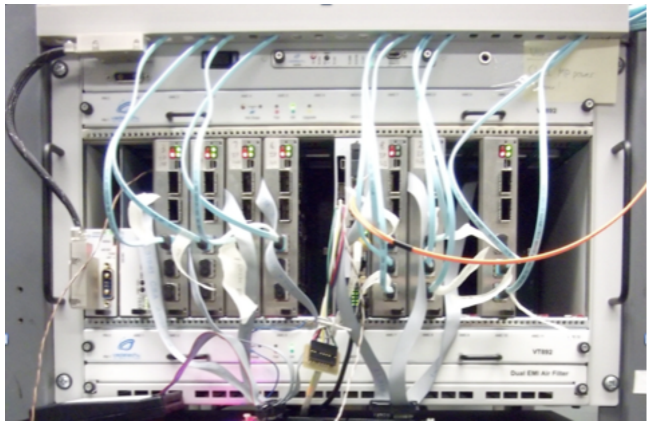
CMS Phase 1 L1-Trigger upgrade

- **Modern FPGAs and µTCA backplane technology for high bandwidth and processing power**
- **New architecture for calorimeter with a full event in one processor**
  - Higher calorimeter granularity, earlier combination of muon systems and improved algorithms
    - e, γ and µ isolation with PU subtraction
    - Jet finding with PU subtraction
    - Tau finding with much narrower cone
  - Global trigger with more inputs and algorithms correlated quantities (e.g. invariant mass)



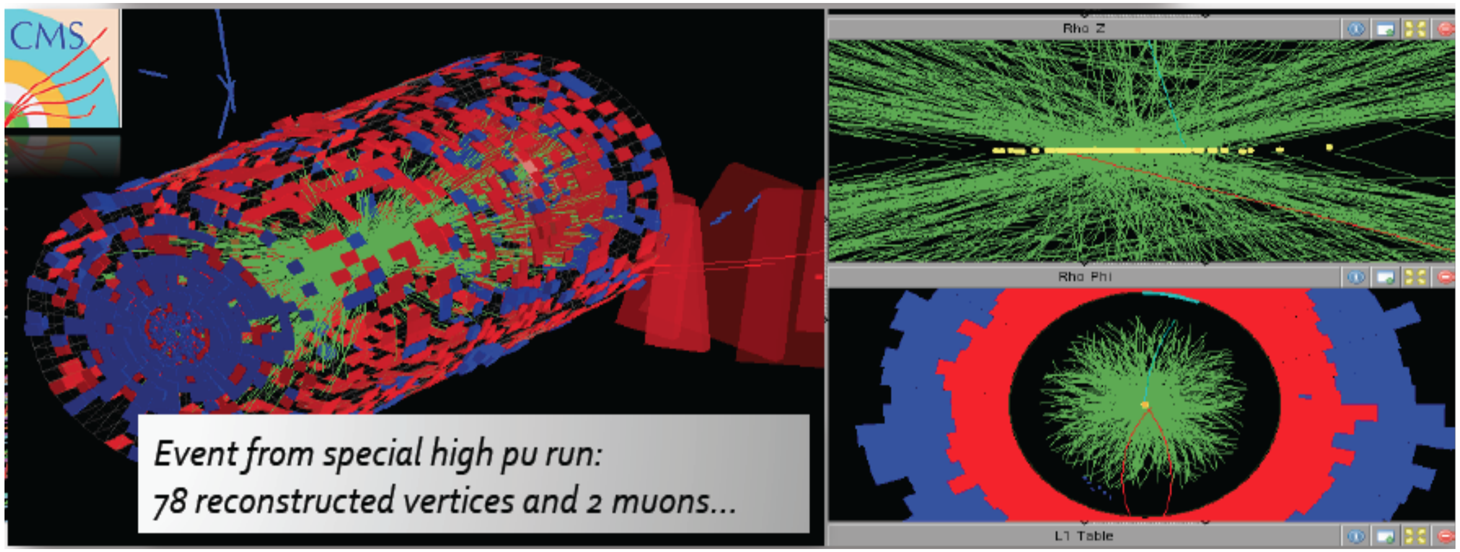
MP7 board Virtex 7 and 72 I/O links at 10Gpbs





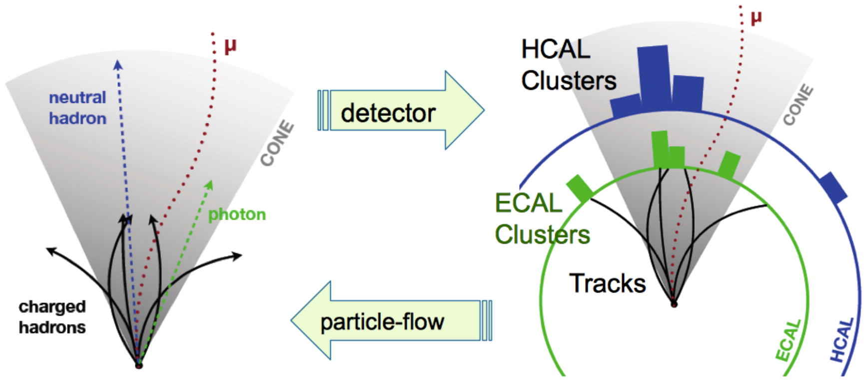
Demonstrator of Calorimeter trigger in µTCA crate

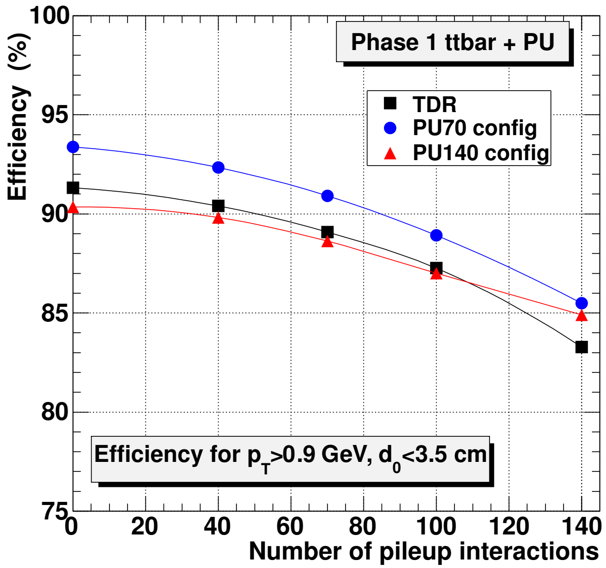
CMS upgrades for HL-LHC (Phase 2)

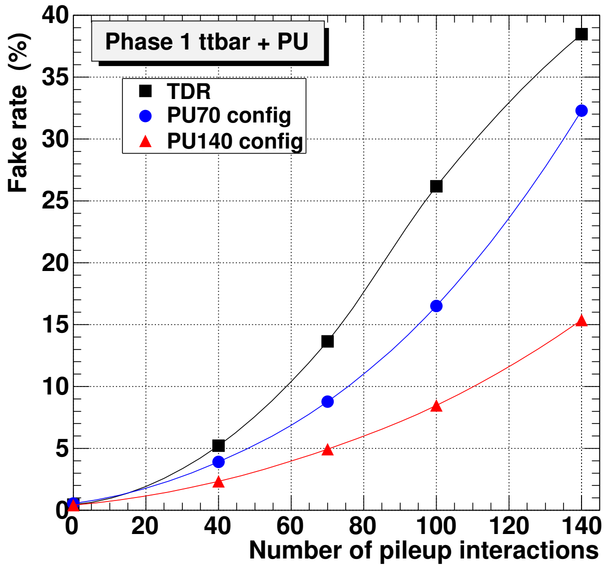


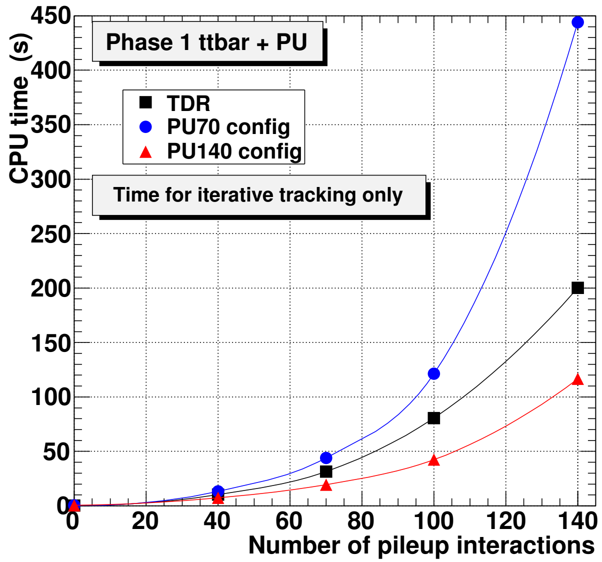
Driving requirements for upgrades at HL-LHC

- Performance aspects
  - Mitigation of PU effect - critical to fully exploit High Luminosity potential:
  - ➢ Need high granularity and precision
    - Tracker performance is critical





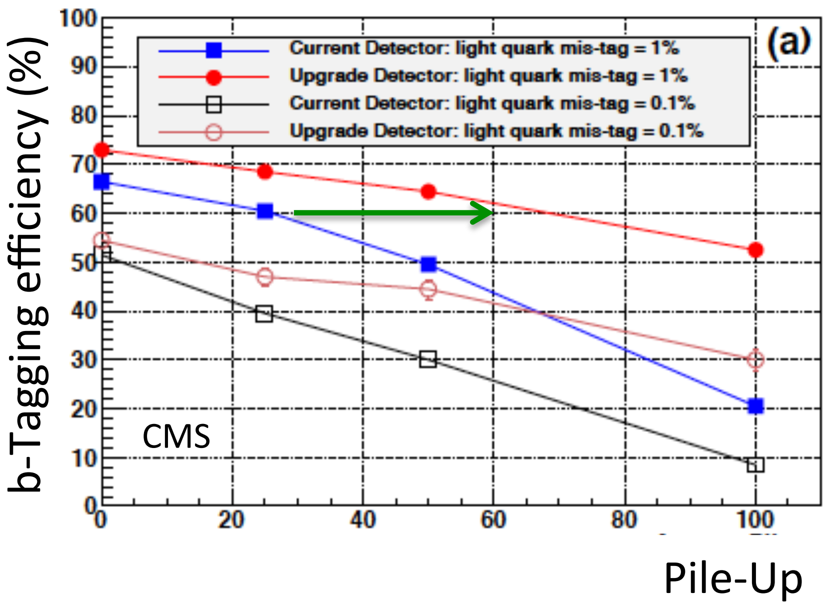


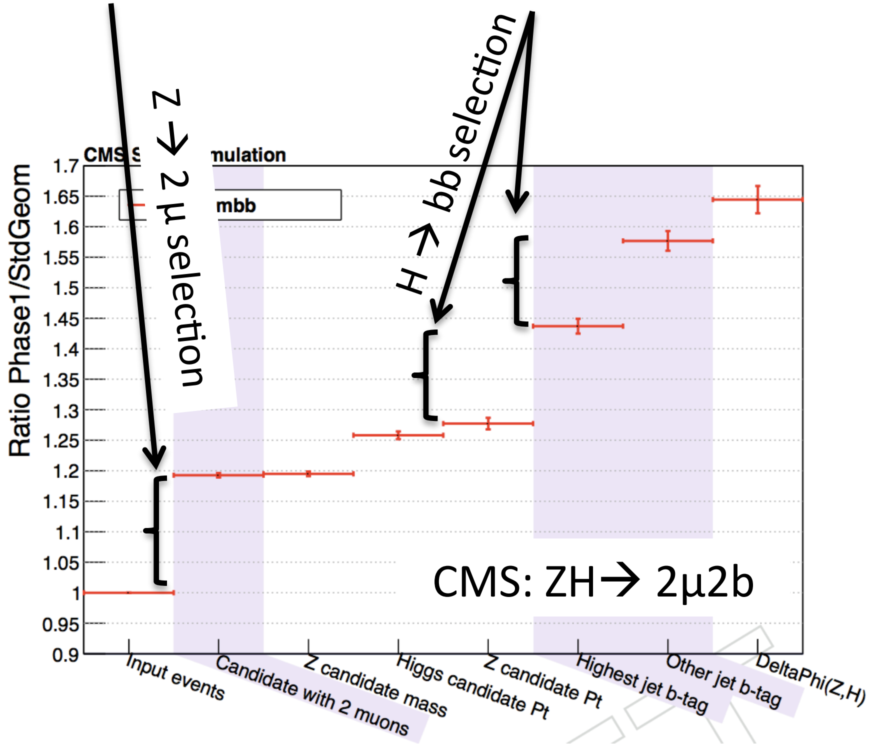


Example of tracking performance degradation with Phase 1 detector when increasing PU

Example of CMS Phase 1 Pixel performance benefit

- Need to maintain/improve the performance at high pile-up
  - → Improves track reconstruction efficiency and resolution on track origin
  - → Improves association of tracks at primary vertex and secondary vertices



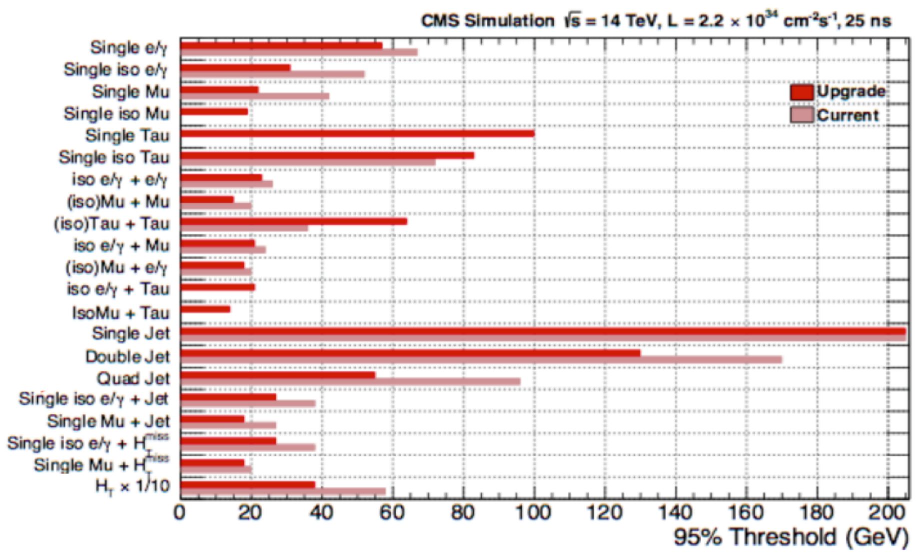


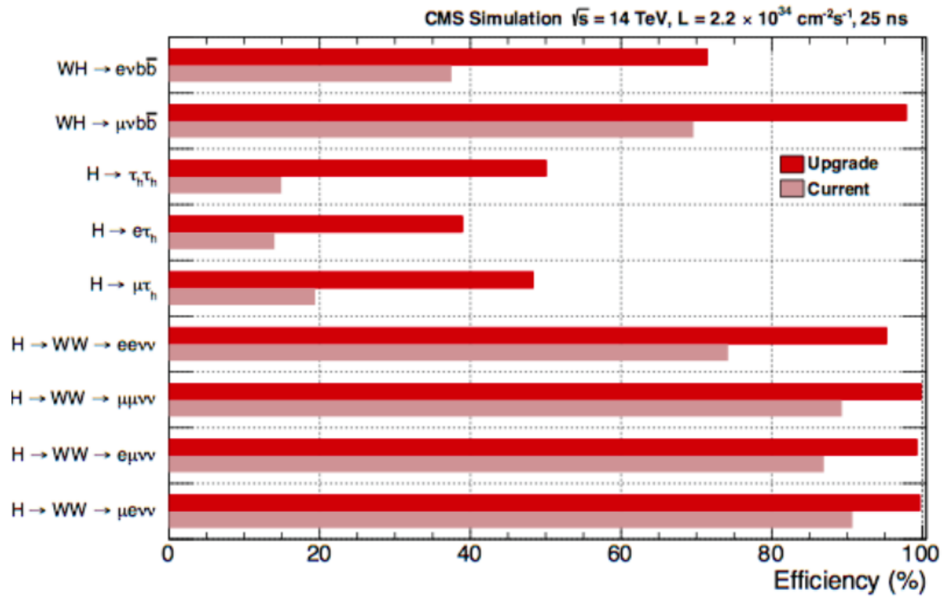
Current performance is maintained up to ~ 70 PU

~ 65% gain in statistics

Driving requirements for upgrades at HL-LHC

- Performance aspects
  - Physics events acceptance - critical to measure rare processes:
    - Need improved trigger: increased bandwidth - precision of inputs - sophisticated algorithms





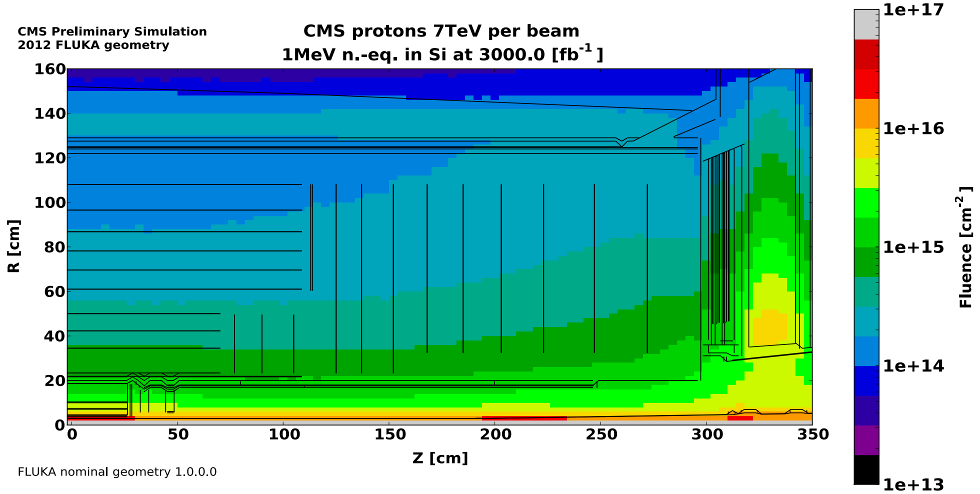
Example of the thresholds improvements with the CMS hardware trigger level upgrade for 50 PU (Phase 1) and impact on physics channel acceptance

→ These levels of thresholds must be maintained at HL-LHC despite rate and PU increase

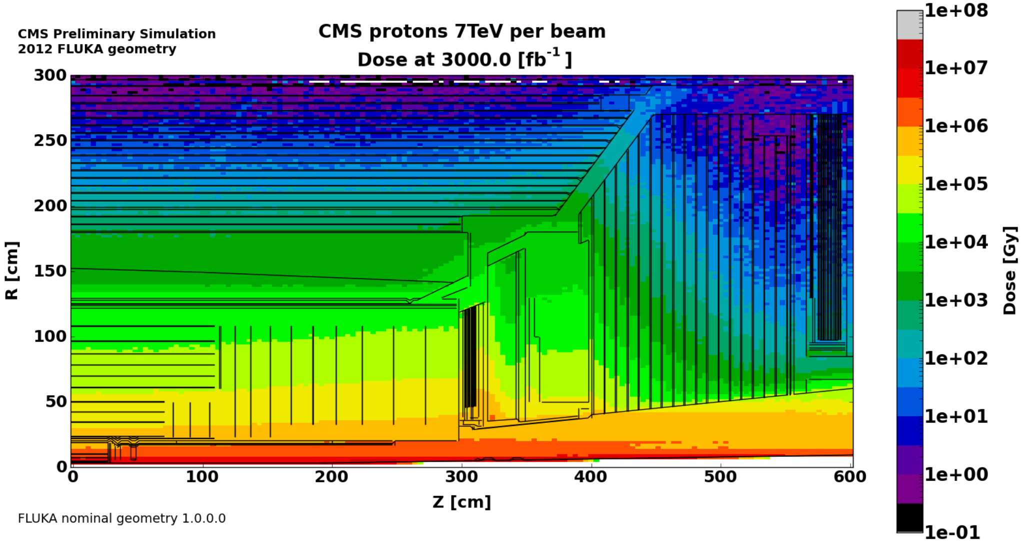
Driving requirements for upgrades at HL-LHC

- Operation aspects
  - Longevity of detector components and radiation tolerance:
    - ➢ Replace detectors as needed with new technologies - an opportunity to improve performance
  - Data flow:
    - ➢ Need high readout bandwidth and fast processing - replace fraction of read-out

- And constraints
  - Integration in present CMS
  - Duration and logistics of work in LS
  - Radiation levels in LS
  - Schedule and cost
  - Collaboration involved in Phase 1 upgrades, data taking and analyses



Preliminary study of fluence in CMS tracker after 3/ab

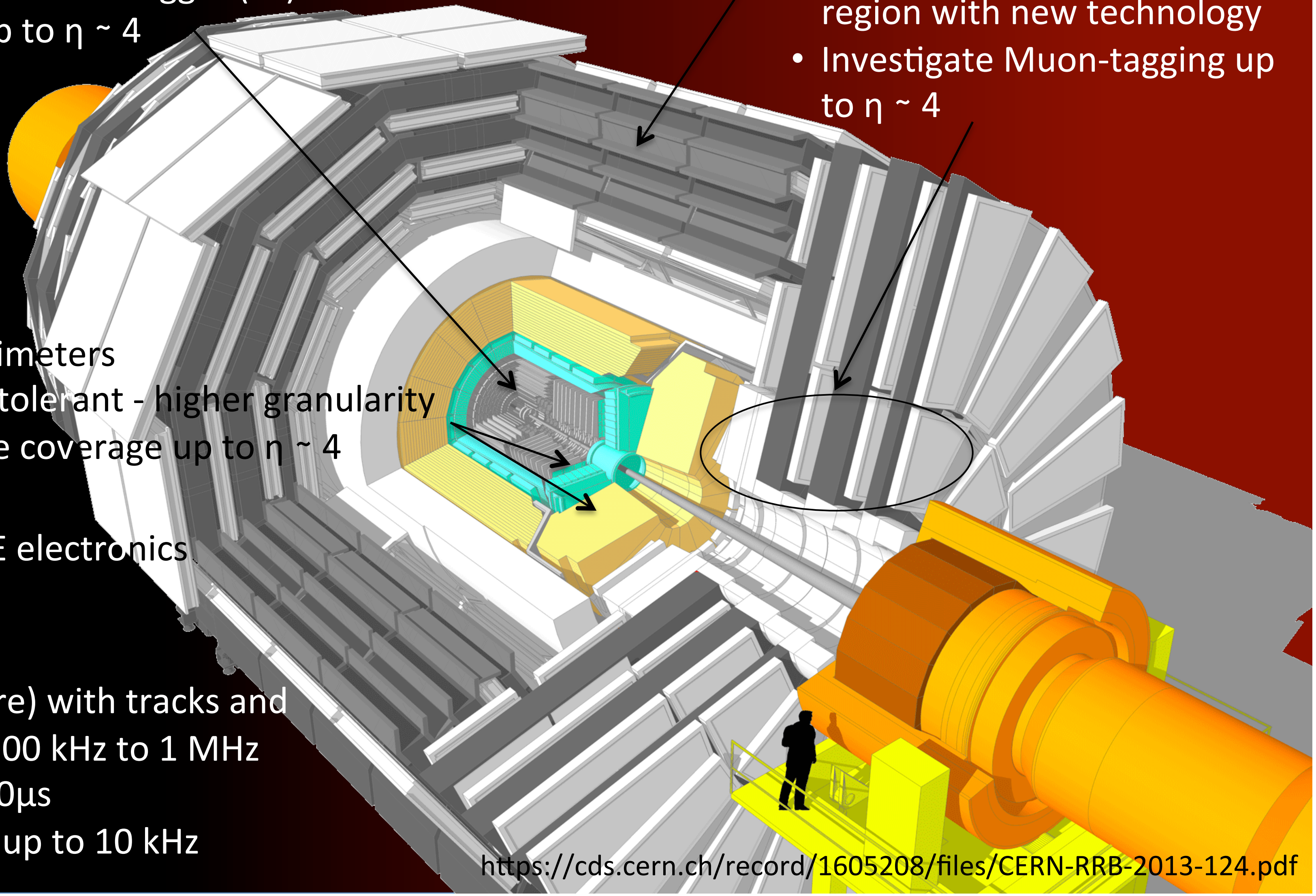


Preliminary study of dose in CMS tracker and Endcap calorimeters after 3/ab

CMS Phase 2 Upgrades

Tracker
- Radiation tolerant - high granularity - less material
- Tracks in hardware trigger (L1)
- Coverage up to η ~ 4

Muons
- Replace DT FE electronics
- Complete RPC in forward region with new technology
- Investigate Muon-tagging up to η ~ 4



Endcap Calorimeters
- Radiation tolerant - higher granularity
- Investigate coverage up to η ~ 4

Barrel ECAL
- Replace FE electronics

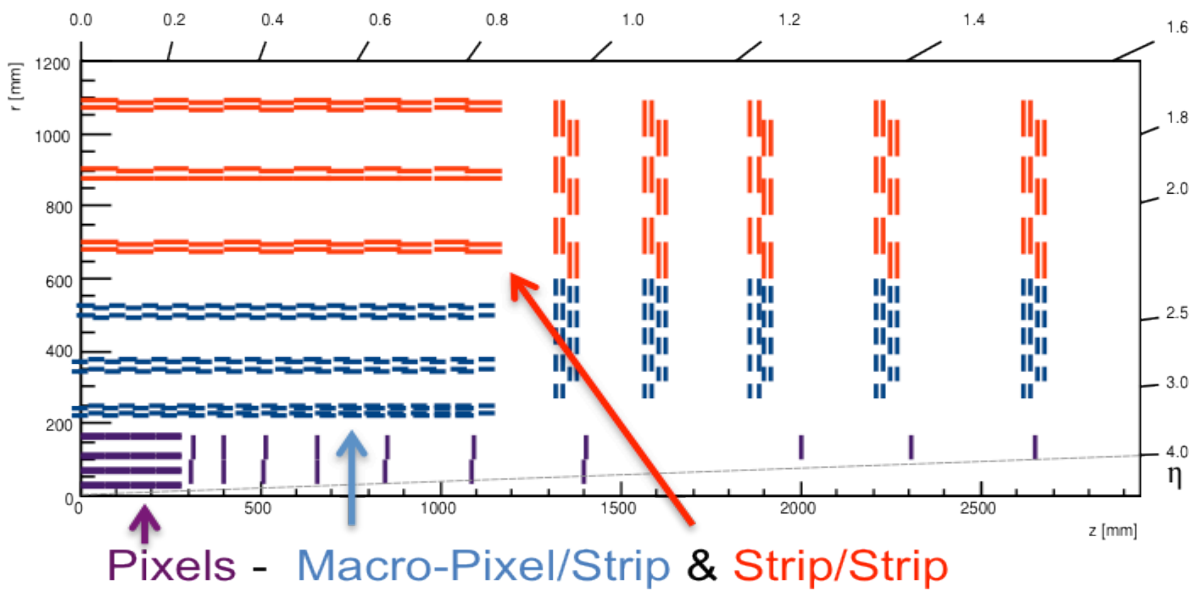
Trigger/DAQ
- L1 (hardware) with tracks and rate up ~ 500 kHz to 1 MHz
- Latency ≥ 10μs
- HLT output up to 10 kHz

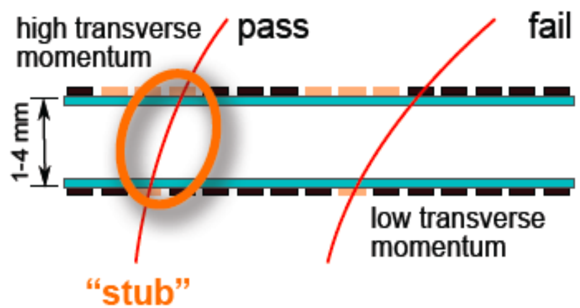
https://cds.cern.ch/record/1605208/files/CERN-RRB-2013-124.pdf

CMS Phase 2 Tracker

CMS Phase 2 Tracker main features

- High Granularity with short strips and small pixels
  - Strip pitch ~ 80-90 µm & length ~ 2.5 to 5 cm
  - Pixel pitch ~ 25-30 µm and ~ 100 µm length
- Light detector with DC/DC powering, CO2 cooling, light module assembly
- Powerful concept to implement tracks in hardware trigger
  - 2 sensor modules to select track "stubs" of Pt≥2GeV for trigger readout (40MHz) Strip-Strip (SS) in outer layers and Macro Pixel-Strip (PS) in inner (z meas.)
- Extension of Pixel coverage up to |η| ~ 4
  - Reduce rate of fake jets due to PU for VBF/VBS physics



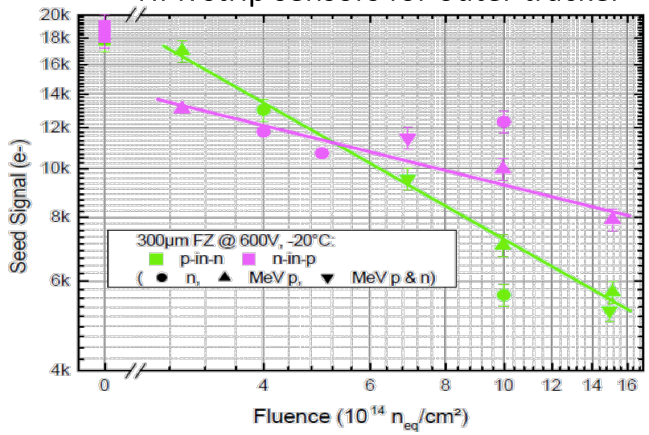


Concept for on detector selective data readout

Silicon-Strip Outer Tracker

- Silicon sensors
  - Sizable campaign of irradiation test - selected n-in-p type sensors (also ATLAS)
  - Optimizing material, thickness, layout & evaluating production on 8" wafers

HPK strip sensors for outer tracker



- Readout
  - Architecture defined - Optimizing data format/BW
  - CBC 130 nm (SS-module) - full size version
  - SSA/MPA 65 nm (PS-module) being designed
  - Concentrator 130 and/or 65 nm (SS/PS module) - FPGA emulation of SS module is implemented
  - GBT (OL ASIC) - need 65 nm low power
  - Versatile Link (OL) - need small size packaging
  - DC-DC powering - based on phase 1 upgrades
  - High Density Hybrid - commercial approach started - first prototypes in hand

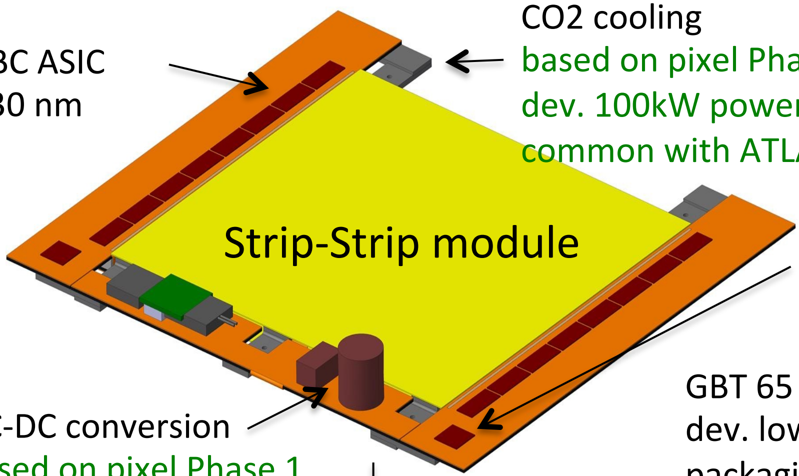
Based on common LHC experiments developments

Silicon-Strip Outer Tracker

- Light module assembly - validated with FEA - building mock-up

CBC ASIC
130 nm

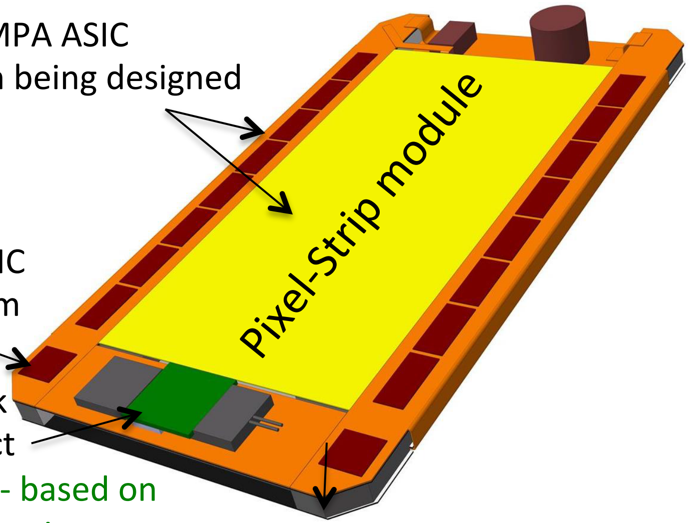
CO2 cooling
based on pixel Phase 1
dev. 100kW power -
common with ATLAS



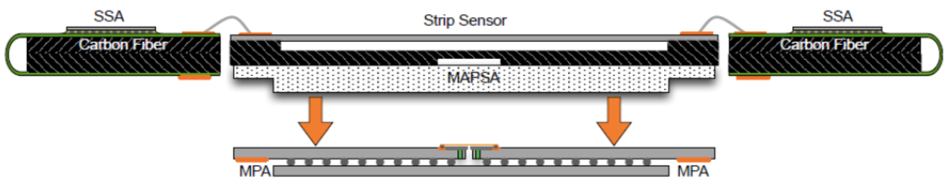
DC-DC conversion
based on pixel Phase 1
common dev. with ATLAS

SSA/MPA ASIC
65 nm being designed

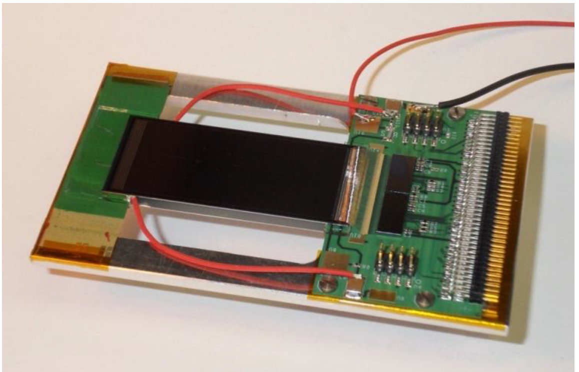
Concentrator ASIC
130 and/or 65 nm

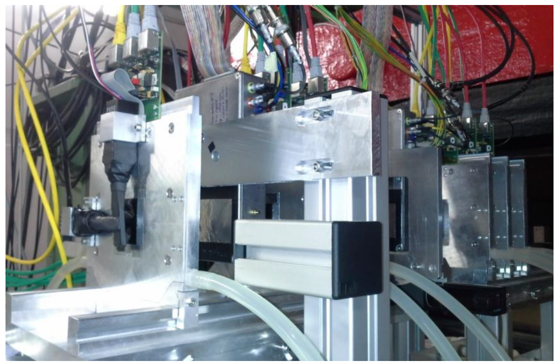


GBT 65 nm & Optical Link
dev. low power - compact
packaging wo connector - based on
common dev. for LHC experiments



Flex hybrid - Flip-Chip assembly - possibly TSV for inter-chip connection

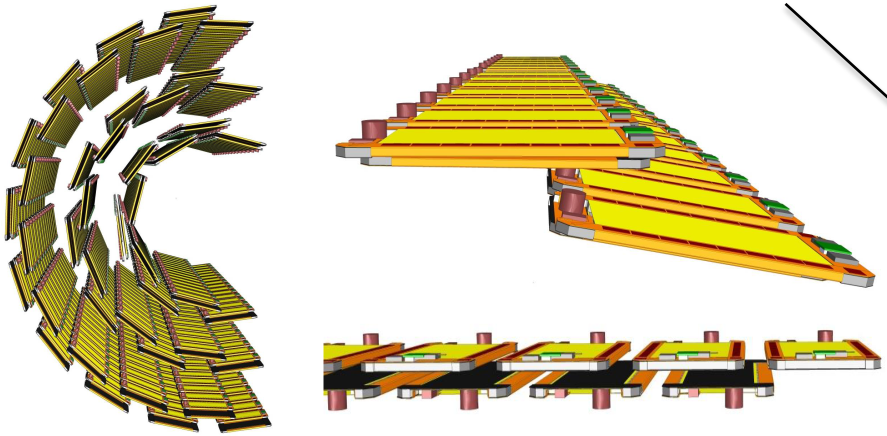


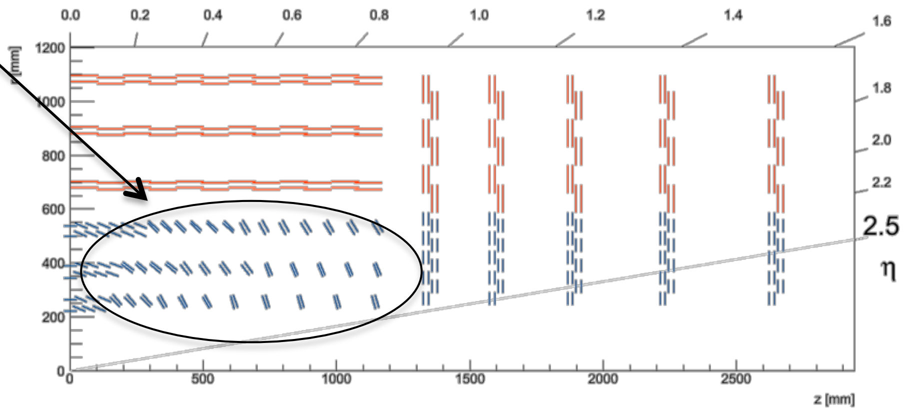


2 prototypes tested at DESY - 2 CBC chips - FPGA emulation of concentrator and of GBT on GLIB prototype DAQ board - validate concept of selective RO

Silicon-Strip Outer Tracker

- Mechanical structures
  - Concept for outer barrel and endcap is selected
  - Decide inner barrel concept in 2014

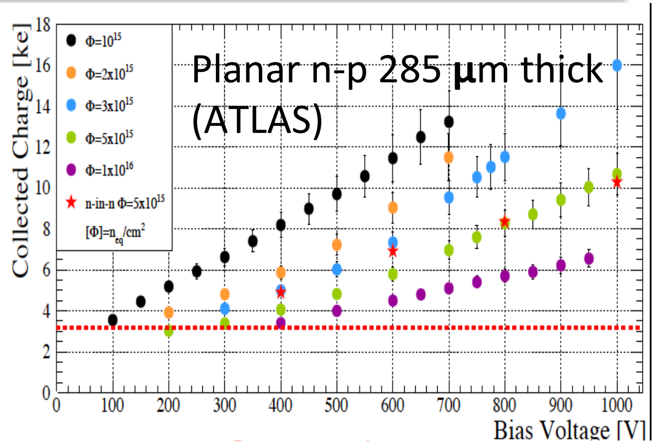


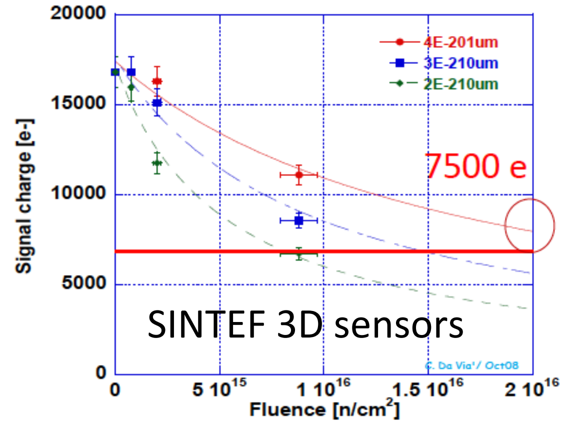


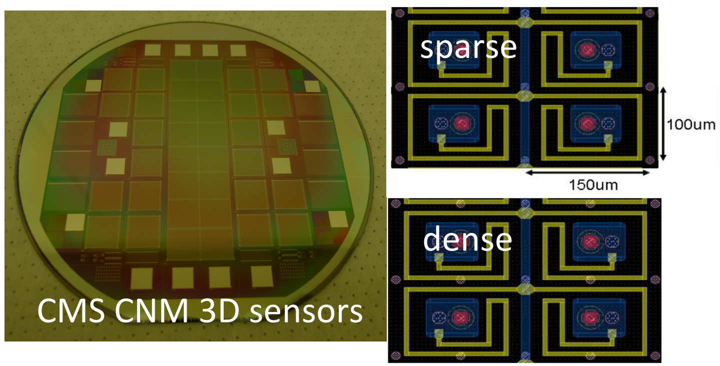
- CO2 cooling
  - Need 100kW - build on pixel Phase 1 - common development with ATLAS
- Back-end electronics for trigger track reconstruction
  - Pattern recognition with Associative Memories or propagation from layer to layer in FPGA followed by fit in FPGA
    - demonstrators being developed - build on ATLAS FTK - existing high BW/ processing boards - generic R&D on custom AM ASICs
  - DAQ building on Phase 1 board developments for Pixel and Trigger

Pixel detector

- Silicon sensor
  - Planar n-in-n or n-in-p and 3D technologies are good candidates to sustain radiation
  - Need design optimization and compare performance
- Readout
  - Pixel ASIC 65 nm - RD53 common project with ATLAS starting - qualify radiation tolerance - develop chip blocks and final architecture
  - High BW low mass electrical link needed for inner pixel layers





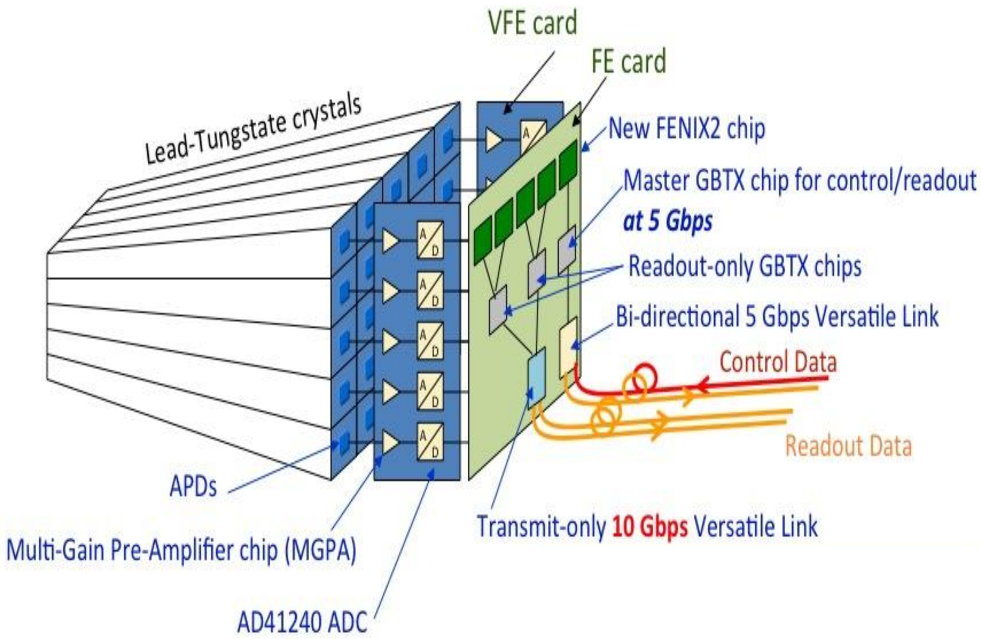


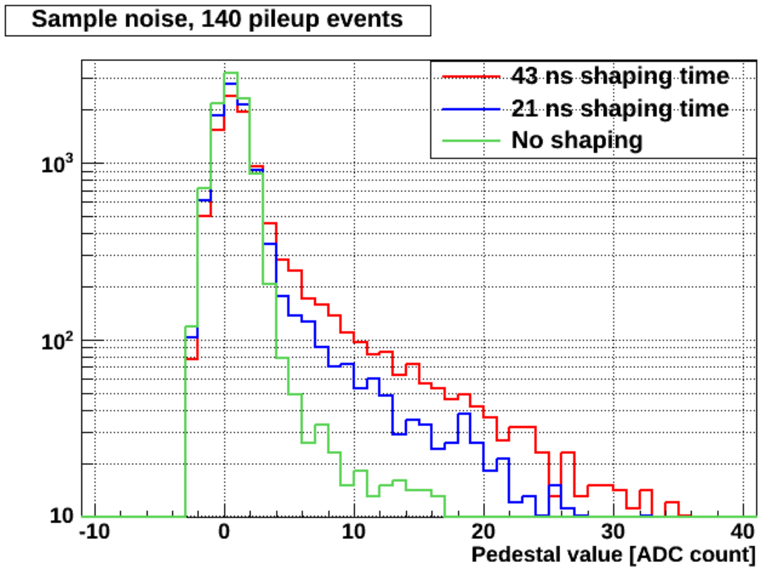
CMS Phase 2 Calorimeter upgrades

- New ECAL barrel FE electronics
- New Endcap Calorimetry - presently three concepts considered:
  - Shashlik EE + HE-rebuild tower geometry as present CMS
  - Combined Forward CALorimeter (CFCAL) based on DREAM/RD52 concept
  - High Granulaity CALorimeter (HGCAL) based on CALICE concept
- Investigating benefit of precise timing & following generic R&D

Phase 2 ECAL Barrel FE electronics

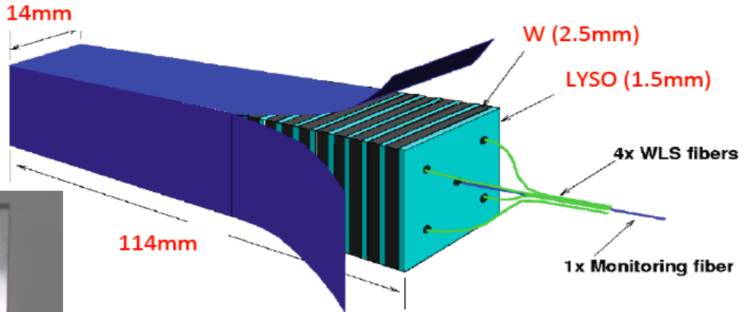
- VFE board with improved shaping - noise/PU mitigation, spike rejection
- FE board with data transfer at 40 MHz and crystal granularity for trigger
    - Investigating commercial versus custom design
    - Need to develop 10Gbps GBTx to minimize cost



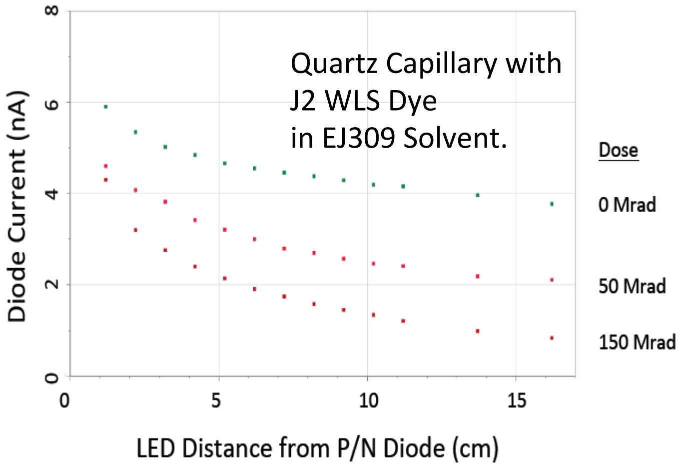


Replacement of Electromagnetic calorimeter with Shashlik

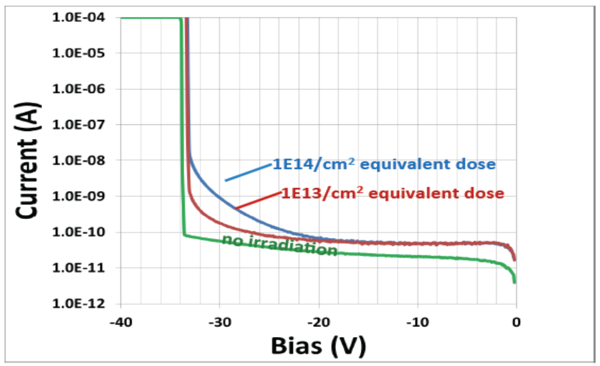
- EE Shashlik provides a similar structure to the current electromagnetic calorimeters
  - With more compact design - higher granularity



- R&D to demonstrate radiation tolerance
  - Crystals - LYSO/CeF3
  - Wave-Length Shifter solutions
    - Quartz capillaries…
  - Photo-detector technology - GaInP/SiPM
  - Readout chip - based on HCAL Phase 1 QIE10 developments



Planar GaInP SPAD results (2013)

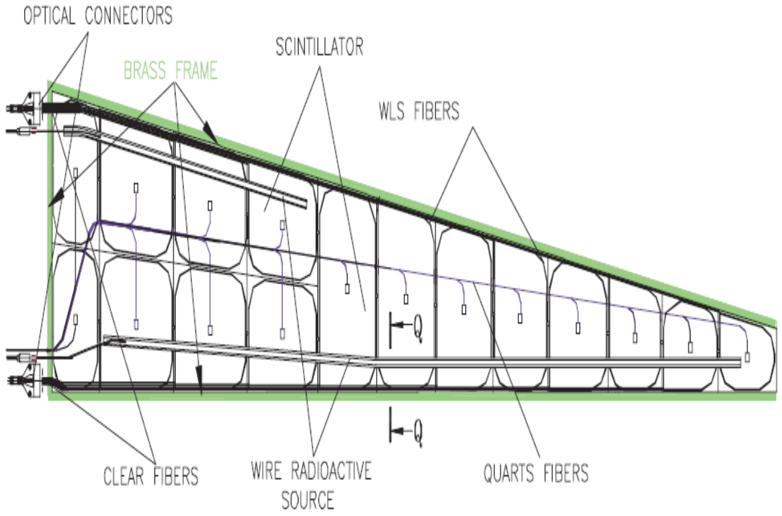


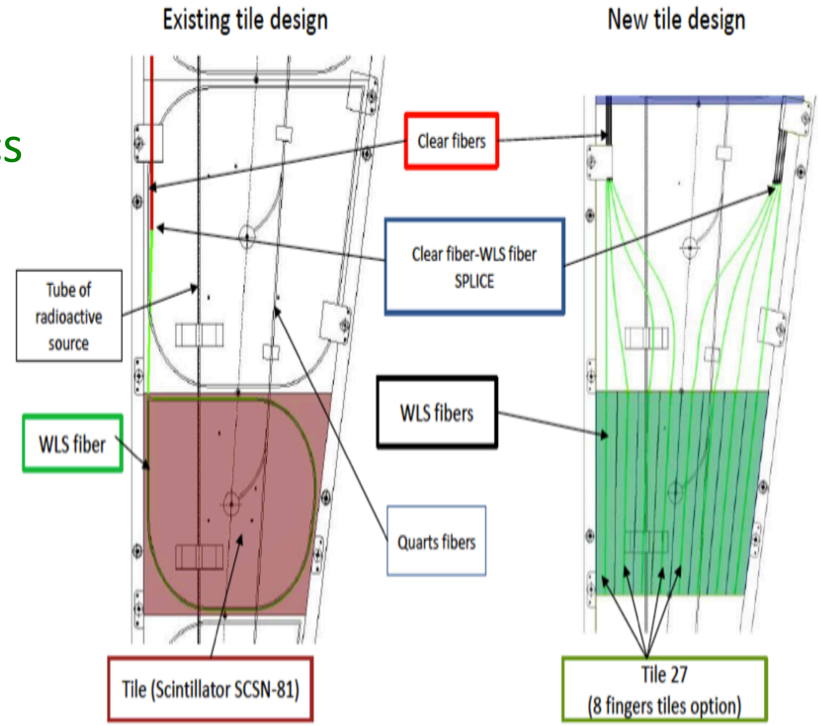
12 MeV electron source

- A 3x3 prototype is being built for beam test in June

Rebuild of Hadronic Calorimeter

- Rebuild HE with:
  - Radiation tolerant material
  - Higher granularity (η/ϕ - longitudinal)
  - Closer to IP behind EE Shashlik or HGCAL
- R&D to demonstrate radiation
  - Different geometry (finger tiles)
  - And different materials - liquid scintillator and other options (fibers for inner region as for CFCAL)
  - Readout with Phase 1 upgrade electronics

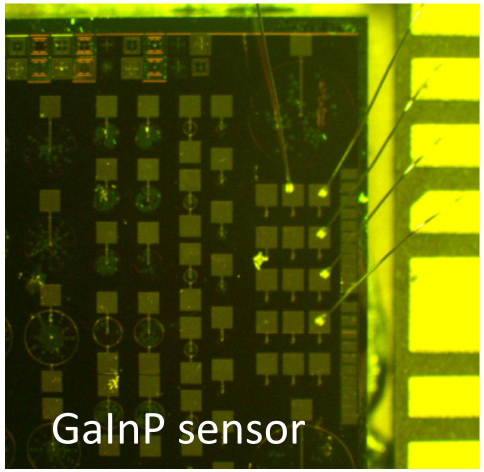


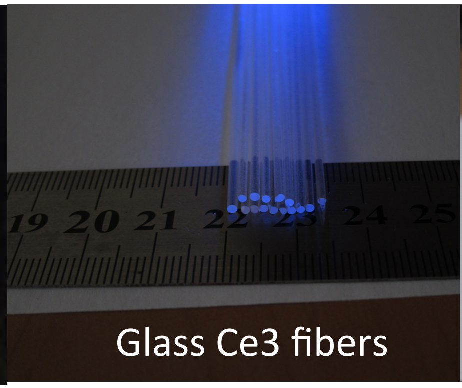


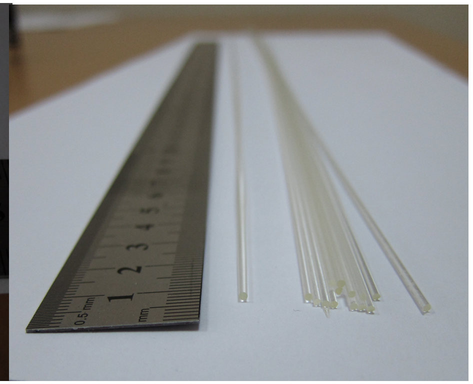
- Ongoing irradiation campaign of scintillating yields and transmission damage with present tiles and various scintillators
- Prepare megatile with fingers for irradiation test at PS late 2014

Combined Forward Calorimeter (CFCAL)

- Combined Forward CALorimeter integrates ECAL & HCAL, based on readout of Cherenkov and scintillating fibers which run full-depth of calorimeter
  - e/γ/hadron identified from Cherenkov/scintillator ratio, and pulse shape sampling at 5 GHz
- R&D to demonstrate radiation tolerance
  - Scintillating fibers - Quartz/Glass/Crystal Ce3 doped
  - Photo-detectors - as for Shashlik EE
  - Readout chip - need high speed digitizer

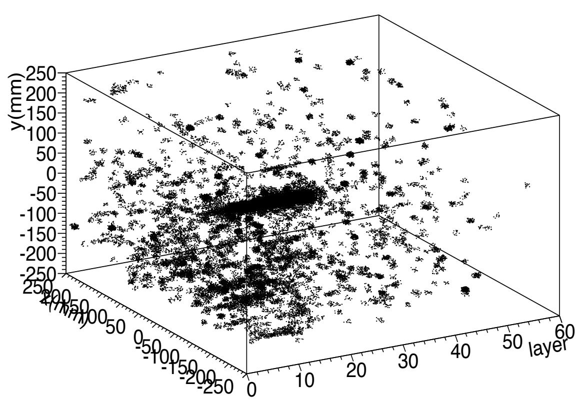






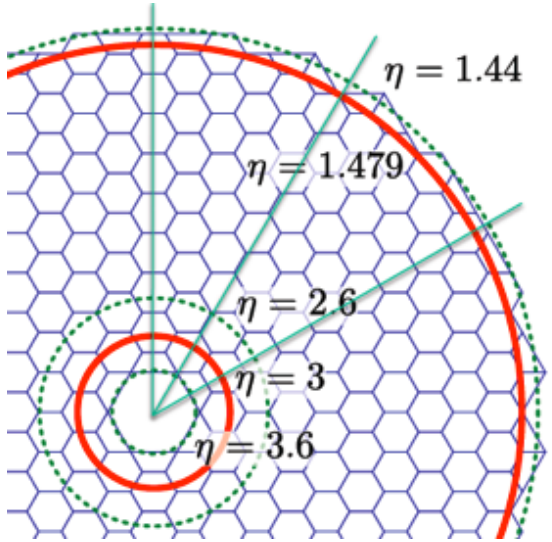
High-Granularity Calorimeter (HGCAL)

- Silicon-lead ECAL & 4λ silicon-brass shower-max HCAL
  - Fine-grained pads from 0.9 cm² to 1.8 cm² in ECAL
  - Fine depth segmentation ~ 31/12 planes in ECAL/SiHCAL
  - Full shower topology to mitigate PU effects
- Back HCAL as HE-rebuild (lower radiation level)



50 GeV hadron and 140 pileup
With threshold of 10 mips

- R&D sensors, cooling, reconstruction & electronics
  - Build on ILC/CLIC & CALICE developments
  - Many common areas of R&D with tracker and other systems upgrades
    - Si sensors 320µm 8" wafers with 200µm & 100µm depletion
    - Readout chain - service

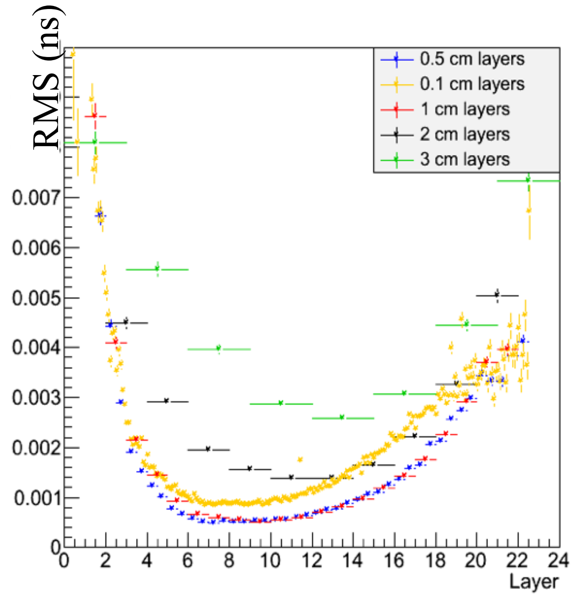


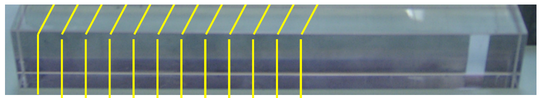
Tiling of 8" hexagonal Si-sensors modules

Precision timing

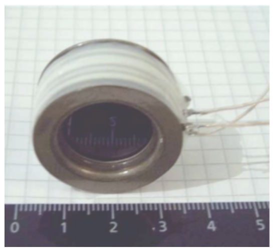
- Time of flight measurement could provide PU mitigation for neutrals
  - precision of ~ 10 ps allows energy deposit association to vertex in the range of ~ 1 cm
- Generic R&D on
  - PMT-MCP or "Ionization-MCP"
  - Silicon sensors : highly doped Si sensor
  - SiPM, HAPD

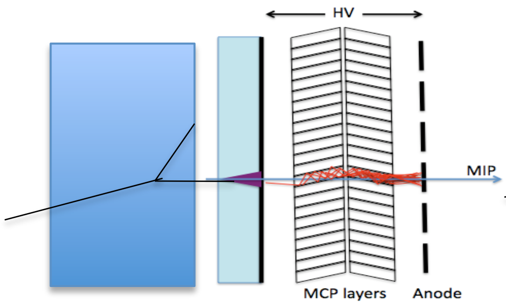
  Could allow implementation in preshower or embedded layer or full calorimeter signal
- Current ECAL barrel timing performance (~ 100 ps with APD and 40 ns shaping) can be optimized with new VFE electronics



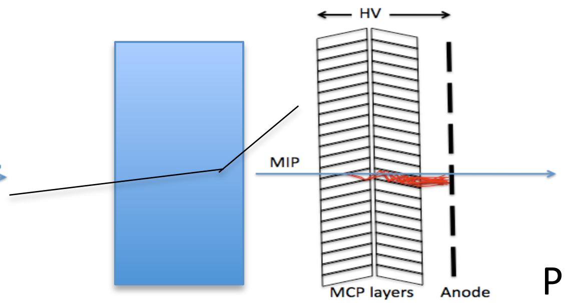


GEANT4 simulation crystals 1cm slices

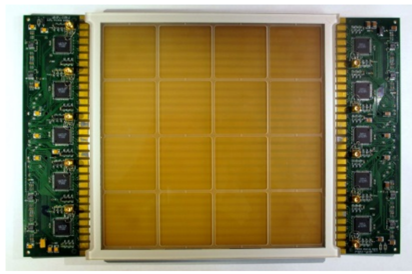




Classical PMT-MCP



"Ionization-MCP"



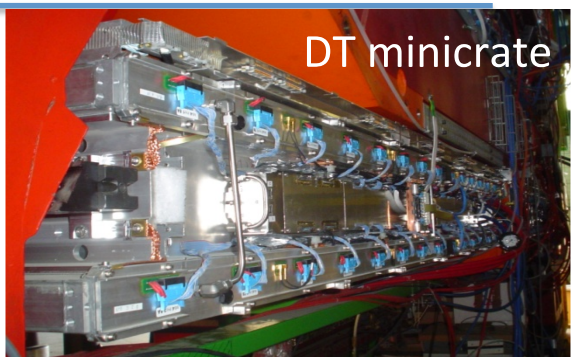
Prototype waveform digitizer on a LAPPD mockup, 15 GSa/s

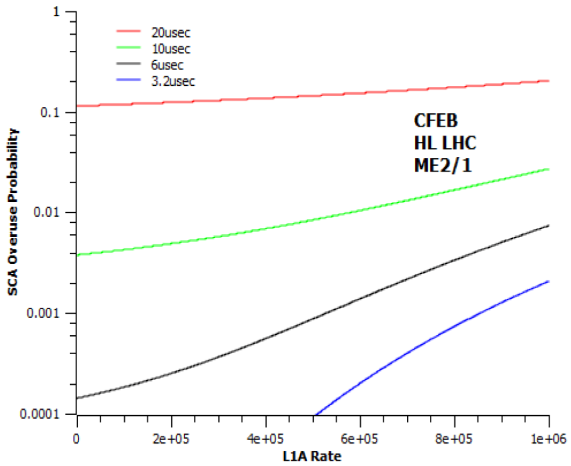
CMS Phase 2 Muon upgrades

- Current detectors are expected to survive 3000 fb^{-1}
  - Studies on long term operation & aging mitigations are ongoing
  - DT new FE electronics resistant to SEU & 40MHz read-out for trigger
- New Forward Muon Detectors
  - GEM - RPC bakelite/glass with low resistivity

Existing muon detectors - longevity & readout

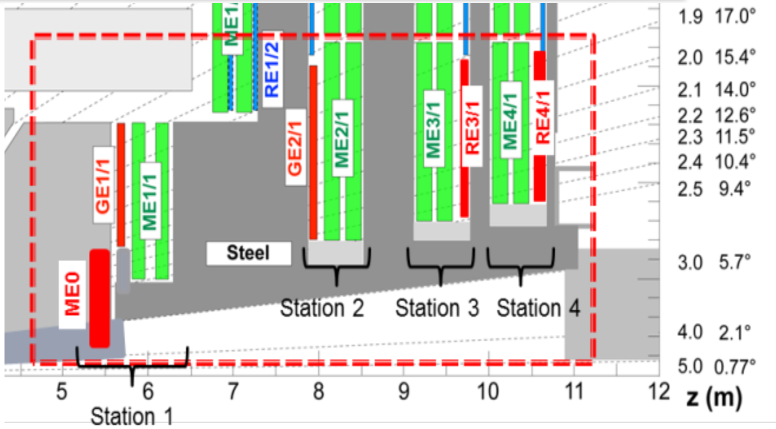
- Common plans (DT, CSC, RPC):
  - Detector and electronics radiation tests at GIF++ (source and beam) late-2014
  - Neutron and/or proton beams for electronics SEU
- Specific plans:
  - DT replacement of FE electronics
  - CSC verify FEB rate capabilities at various latencies with data
  - RPC R&D on freon-less gas mixtures (LHC- and CERN-wide project) includes tests at GIF++

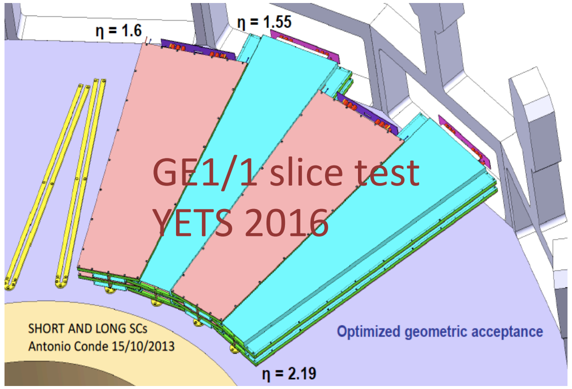




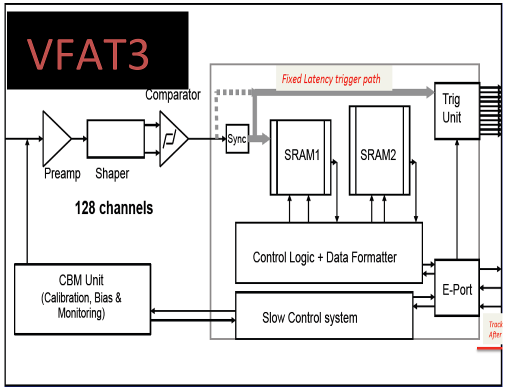
New Forward Muon Detector

- GEM detectors
  - Assembly technique is optimized GE1/1
    - GE2/1 but 2x larger, ME0 same size more layers
  - FE: VFAT3 (analog/digital) - being designed
  - Back-end, DAQ, & trigger electronics - being prepared for slice test installed in 2016 YETS





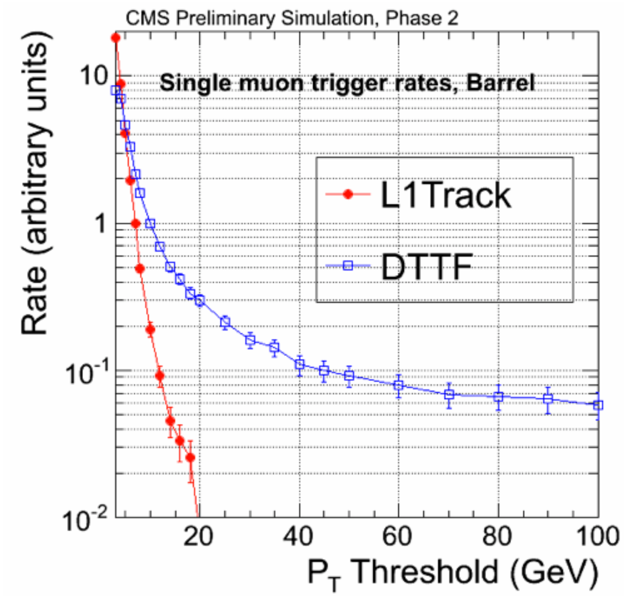
- Improved RPC detectors
  - Glass:
    - Production of low resistivity glass
    - Large size chamber assembly - 6 prototypes at GIF++ late 2014
  - Bakelite:
    - Low resistivity - smaller gap for low HV CMS-ATLAS-ALICE 2014-16
  - New electronics - improved timing

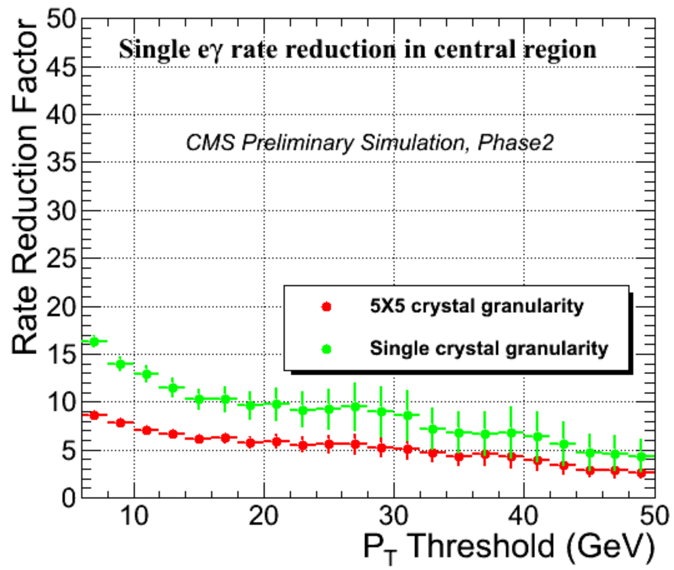


CMS Phase 2 Trigger/DAQ upgrade

Trigger/DAQ upgrades for HL-LHC

- L1-trigger, Hardware
  - Tracker information (Pt≥2) at 40 MHz - Crystal granularity in ECAL
    - Pattern recognition with Custom ASIC Associative Memory chip (as developed for ATLAS FTK in phase 1) or track propagation using FPGA followed by a track fit in a FPGA for precision & cleaning of multiple tracks
  - Level 1 in ≥ 10 µs - up to ~1 MHz input to computing level (HLT)
- Computing trigger level
  - HLT input ~32 Tb/s - output up to ~10 kHz similar rejection as present syst.





Lepton trigger rate reduction by a factor 5 to 10 with track at L1

Summary

- CMS Phase 1 upgrades construction for Pixels, HCAL and Trigger is making good progress and proceeding within the expected schedule

- The CMS collaboration is preparing a Technical Proposal for Phase 2 for the September 2014 LHCC meeting - it will include supporting performance simulation studies

- Critical R&D for Phase 2 are well identified and the effort is ramping-up with good progress in selecting technologies and preparing prototypes