ATLAS Level-1 Calorimeter Upgrade for Phase 1

ACES 2014 – CERN

David Sankey, Thursday, 20 March 2014

with special thanks to Ian Brawn
Overview

A personal canter through the Phase 1 L1Calo system

History
  • Run 1, Run 2

Phase 1 overview

eFEX – $e, \gamma$ and $\tau$

New algorithms
  • lateral $R_\eta$ – relating central core to immediate surroundings
  • depth $f_3$ – relating back sampling to whole

jFEX – jets, $\Sigma E_T$, $\Sigma E_T^{\text{miss}}$

Link speed

Beyond Phase 1
Run 1 system

Analogue towers from calorimeters
  - tower granularity $0.1 \times 0.1$ in $\eta$ and $\phi$ for $e$, $\gamma$ and $\tau$
  - $0.2 \times 0.2$ for jets, $\Sigma E_T$, $\Sigma E_T^{\text{miss}}$

Trigger decision formed in CTP on basis of hit counts
  - total Level 1 latency $\sim 2.5\mu$s to get decision back to detectors

Tuned and tweaked over the years
  - for example adding missing $E_T$ significance, $XS$
Run 2 system

Same granularity as Run 1

Upgraded digitisation and digital filtering

- reduce sensitivity to pileup and bunch structure, lower noise

Trigger decisions based on trigger objects

(new systems in green)
Selection of new Run 2 modules

New CMX (custom 9U module)
  • merges trigger objects from existing processor modules

L1Topo ATCA module
  • all objects on single module
Phase 1 (Run 3) system

**Same latency for trigger decision**

Higher granularity and segmentation in depth from Liquid Argon
- granularity $0.025 \times 0.1$ in $\eta$ and $\phi$ for $e$, $\gamma$ and $\tau$ in middle layers in depth

![Diagram of calorimeter layers](image)

Allows shower shape cuts for $e$, $\gamma$ and $\tau$
- lateral $R_\eta$ - relating central core to immediate surroundings
- depth $f_3$ - relating back sampling to whole

$0.1 \times 0.1$ granularity higher precision energies for jets, $\Sigma E_T$, $\Sigma E^\text{miss}_T$
- improved noise rejection and allows Gaussian weighting *etc.*
Phase 1 Liquid Argon upgrades

(new components in red)
Phase 1 system (initial)

(new systems in yellow and orange)

Run 2 system initially continues in parallel
  • then gracefully retired, removing CP system and old inputs to L1Topo
New systems

Inputs from 124 LTDB in Liquid Argon (maximum of 124 DPS AMCs) and 32 JEMs
  • too many links for all data in a single FPGA...

eFEX

Processes $e$, $\gamma$ and $\tau$ in window size of $0.3 \times 0.3$

Digital Super Cells from Liquid Argon and hadronic Towers via original L1Calo
  • $\sim$34000 Super Cells @ 10 bit precision, $\sim$3000 Towers @ 10 bit
  • over $1/3$ Mbit/event before duplication

jFEX

Processes jets, $\Sigma E_T$, $\Sigma E_T^{\text{miss}}$

0.1 $\times$ 0.1 granularity, jets up to 0.9 $\times$ 0.9

(gFEX)

0.2 $\times$ 0.2 granularity
  • jets up to 1.8 $\times$ 1.8
  • $\eta$ rings for improved pileup subtraction

Under consideration as separate modules or as equivalent functionality in jFEX)
eFEX overview

Diagram showing the eFEX module with various components and connections:
- MTP to 4x48
- Op Rx to 12x12
- Fanout to 144
- 4 Processor FPGAs
- De-serialiser to e/τ extractor
- Results Merger
- Serialiser to 36 Op Tx
- 3x12 to LITopo
- To/from Hub
- Configuration Controller FPGA
- Configuration IPbus
- Control FPGA
- LAPP Card
- IPMC
- From TTC interface on Hub
- To ROD on Hub
- Rolling Memory
- Derandomiser
- L1A (L0A)
- Readout Interface FPGA
- TTC Interface

Caption:
Ian Brawn, on behalf of L1Calo
7 November 2013

Caption:
eFEX overview

Caption:
ATLAS Level-1 Calorimeter Upgrade for Phase 1 Page 10 of 22
David Sankey, March 20, 2014
Data input to eFEX

**ECAL fibres**
- 1-4-4-1 Super Cells per 0.1 \( \times \) 0.1 (\( \eta \times \phi \)) Tower
- BCMUX \( \Rightarrow \) 2 \( \times \) 1 (\( \eta \times \phi \)) Towers / fibre

**HCAL fibres**
- Towers of 0.1 \( \times \) 0.1 summed in depth
- 4 \( \times \) 2 (\( \eta \times \phi \)) towers/fibre

*Overlapping windows \( \Rightarrow \) data sharing…*

**Fan out between modules and crates**
- 2–1 fan out at source (ECAL DPS + HCAL solution)
- 4–1 fan out via 2–1 passive optical splitting

**Fan out between FPGAs**
- 2–1 fan out via PMA loopback in FPGA transceivers, retransmitted after equalisation, before decoding
- 4–1 fan out via discrete high-speed buffers – improved signal quality & latency
- *use latter for all on-board fan out if density allows*
Chapter 2: Physics Requirements and Expected Performance

To optimize the physics reach at each phase of the accelerator complex upgrades, ATLAS has devised a staged program in three phases, corresponding to the three long shutdowns.

The LHC will undergo a major upgrade of its components (e.g. low-pileup electronics (a) and by the proposed upgraded trigger electronics (b). Installation of a fourth (inner) layer for the pixel detector requiring a new, smaller radius central (Be) and more neutron shielding in the muon endcap toroids.

ATLAS upgrade plans up to 2030 and beyond, i.e. up to an annual integrated luminosity of \(\mathcal{L} = 500 \text{ fb}^{-1}\) for Phase-I operation and an annual integrated luminosity of \(\mathcal{L} = 3000 \text{ fb}^{-1}\) for Phase-II operation and an annual integrated luminosity of \(\mathcal{L} = 34 \text{ fb}^{-1}\) (Phase-II operation) and an annual integrated luminosity of \(\mathcal{L} = 34 \text{ fb}^{-1}\) per year for Phase-II operation.

An electron (with \(\mathbf{p}_T > 20 \text{ GeV}\)) in the Level-1 Calorimeter trigger has a narrow distribution for electrons, close to unity. In contrast, the hadronic distribution is normalized to unit area.

Lateral \(R_\eta\) and depth \(f_3\) discriminants for electrons and jets with \(p_T > 20 \text{ GeV}\) is defined as the transverse energy deposited in a calorimeter hit, and in many cases, the energy is integrated over a volume.

\[ R_\eta = \sqrt{\eta^2 + \phi^2} \]

\[ f_3 = \frac{\text{Sigma E}_T}{\text{Sigma E}_\text{res}} \]

\[ f_3 \propto \frac{\text{Sigma E}_T}{\text{Sigma E}_\text{res}} \]

where the sums run over the Super Cells.

\[ R_\eta \] and \( f_3 \) are used to discriminate between electrons and jets.
eFEX processes maximum core area of $1.6 - 1.7 \times 0.8 \ (\eta \times \phi)$

- window size of $0.3 \times 0.3 \Rightarrow$ module environment of $1.8 \times 1.0$
- $2 \times 1 \ (\eta \times \phi)$ ECAL towers/fibre: 100 fibres from ECAL = 9 Minipods
- $4 \times 2 \ (\eta \times \phi)$ HCAL towers/fibre: 36 fibres from HCAL = 3 Minipods

4 FPGAs, each processing environment of $0.6 \times 1.0 \ (\eta \times \phi)$

- per FPGA: 40 ECAL fibres + 18 HCAL fibres + 2 spares = 60
- spares: extra resources for regions where input mapping more complex

*Target device = XC7VX550T-FFG1927: 80 GTH*

Fan out between FPGAs

- $60 \rightarrow 1$ FPGA (including 8 spares)
- $72 \rightarrow 2$ FPGAs
- $12 \rightarrow 3$ FPGAs

*230 multi-Gb/s input tracks on PCB*
Link speed

Ideally all links should be run as fast as possible
- link speed directly affects input mapping

Constraint comes from the many fan-out tracks on PCB
- hence baseline input link speed of 6.4 Gb/s

High Speed Demonstrator with many SMA connectors built to allow structured investigation into high-speed design
- compare simulation with measurements

Results suggest that higher input link speeds will be possible
- but must be verified in hardware

*System tests of first prototypes scheduled in latter half of 2015*

Decision on link speed only possible after this
**efEX output to L1Topo**

Merging ⇒ prioritisation & sorting of data
- complexity to be defined
- *latency constraint*

Ensure efEX can populate full bandwidth to L1Topo with useful data
- merge all data in single location
- allow all data to be provided by any 1 FPGA

Speed of FPGA—FPGA links is compromise between latency and number of links
- most demanding case considered:
  2 fibres → L1Topo FPGA @ 11.2 Gb/s

Upgrade path: 2 spare fibres from second FPGA
- too demanding for single FPGA
- dual star network on board
jFEX overview
jFEX algorithms

Calculate energy sums: $E_T$, $E_T^{\text{miss}}$

Identify jet and fat $\tau$ candidates

Compared to current JEP system

- increased dynamic range
- granularity $\times 4$
- allows flexibility in jet definition (non-square, Gaussian filter, ...)

Increased jet environment

$\leq 0.9 \times 0.9 (\eta \times \phi)$

- increases with higher bandwidth or pre-clustering in jFEX, large jets at L1Topo
jFEX module processes full $\phi$ strips ($\eta$ rings in ‘gFEX mode’) with large overlap area

- window size $0.9 \times 0.9 \Rightarrow$ environment of $9.8 \times 1.6$ ($\eta \times \phi$)
- fan-out between modules at source
- fan-out within module between FPGAs using PMA loopback

8 towers/fibre from ECAL + HCAL: $72 \times 16 \times 2 / 8 = 288$ fibres

- $24 \times 12$-way Micropods
- $4 \times 72$-way MPO/MTP optical connectors

6 FPGAs, each processing core of $1.2 \times 0.8$ ($\eta \times \phi$), environment of $2.0 \times 1.6$ ($\eta \times \phi$)

- Per FPGA: 40 ECAL fibres + 40 HCAL fibres = 80

Target devices = XC7VX690T (4) + XC7VX1140T (2 for overlap region)
jFEX high speed option

Advantages of increasing bandwidth

- larger environment: $\pm 0.4 \rightarrow \pm 0.8 \eta/\phi$
- larger jets: $1.7 \times 1.7 (\eta \times \phi)$

@ 10Gb/s: 16 towers/fibre and DPS fan-out → 3 jFEX

Simplification in jFEX hardware

- 288 Incoming fibres: $\rightarrow 186$
- 24 Micropods $\rightarrow 16$
- MPO/MTP: $4 \rightarrow 3 \times 72$-way

4 large FPGAs per module

- XC7VX1140T
- $\leq 96$ high speed links
- core of $1.6 \times 0.8 (\eta \times \phi)$ (central region)
- environment $\rightarrow 2.4 \times 1.6 (\eta \times \phi)$

Higher transmission rate strongly favoured by jFEX team

Also strongly preferred for jFEX in gFEX $\phi$-ring mode
ATLAS Level-1 Calorimeter Upgrade for Phase 1

ATCA shelf infrastructure

Hub module providing distributed clock and TTC and aggregated read-out
  - custom network on Fabric Interface
  - ethernet on Base Interface for module control using IPbus
Run 4 and beyond

L1Calo becomes L0Calo

- final parts of original system are retired
- all inputs become digital...

Diagram:
- L0Calo
  - supercells
  - Optical Plant
  - ECAL (digital)
  - HCAL (digital)
  - 6.4 Gb/s
- Jet Feature Extractor
  - Hub ROD
- e/Γ, τ
- Jets, τ, ΣE, E_{miss}
- L0Topo
- L0CTP
- L1
  - L0A
  - L1Muon
  - L1Topo
  - L1CTP
  - L1Track
- R3
- To DAQ
- RoI
- ~3 μs?
- 20 μs?
Round up

Upgrades to Pre-Phase 1 systems proceeding apace

Specification of eFEX and jFEX is in process
  • eFEX prototype PDR last month

Module design for eFEX maturing

Design for jFEX strongly affected by link speed
  • and whether $\phi$ strips or $\eta$ rings
  • Xilinx UltraScale vs V7

Investigation of optimal pile-up correction using jFEX + L1Topo is in progress

Desire for link speeds $\sim 10$ Gb/s
  • bandwidth $\rightarrow$ L1Topo
  • jets up to $1.8 \times 1.8$ in jFEX
  • $\eta$ rings for improved pileup subtraction in jFEX

But baseline is 6.4 Gb/s
  • These are complex boards and we need to prove prototypes

Prototypes ready for system tests mid 2015