ATLAS Level-1 Calorimeter Upgrade for Phase 1

ACES 2014 – CERN

David Sankey, Thursday, 20 March 2014

with special thanks to Ian Brawn

Overview

A personal canter through the Phase 1 L1Calo system

History

- Run 1, Run 2

Phase 1 overview

eFEX – e, γ and τ

New algorithms

- lateral R_η – relating central core to immediate surroundings
- depth f_3 – relating back sampling to whole

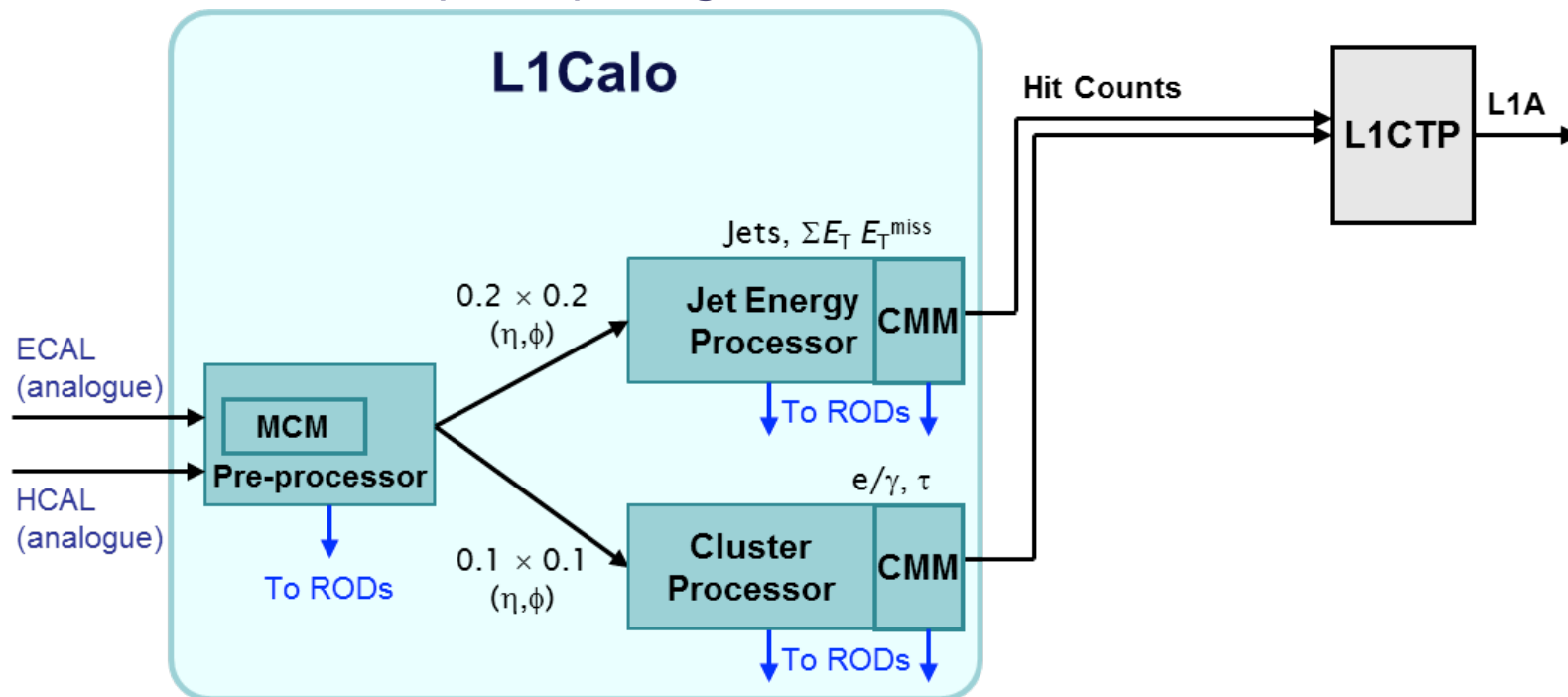jFEX – jets, ΣE_T, ΣE_T^{miss}

Link speed

Beyond Phase 1

Run 1 system

Analogue towers from calorimeters

- tower granularity 0.1×0.1 in η and ϕ for e, γ and τ
- 0.2×0.2 for jets, ΣE_T, ΣE_T^{miss}

Trigger decision formed in CTP on basis of hit counts

- total Level 1 latency ~2.5μs to get decision back to detectors

Tuned and tweaked over the years

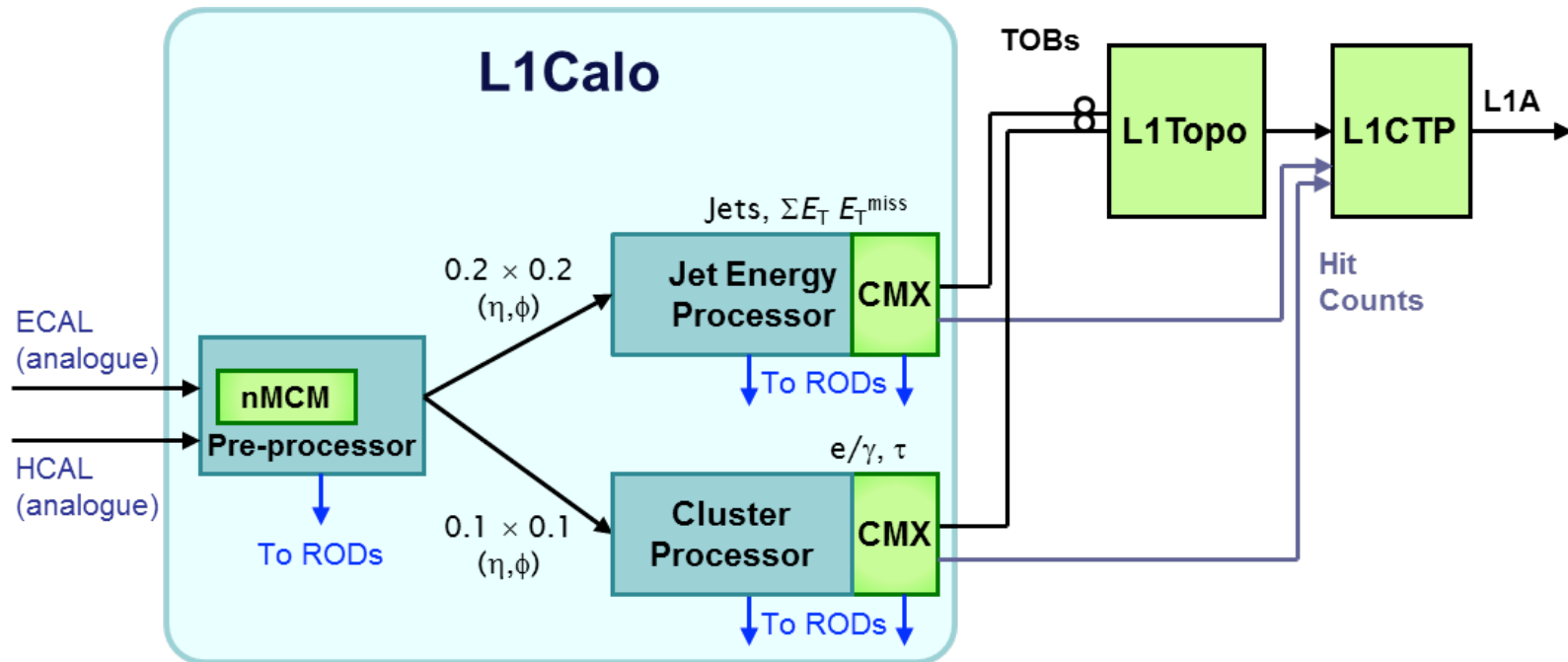- for example adding missing E_T significance, *XS*

Run 2 system

Same granularity as Run 1

Upgraded digitisation and digital filtering
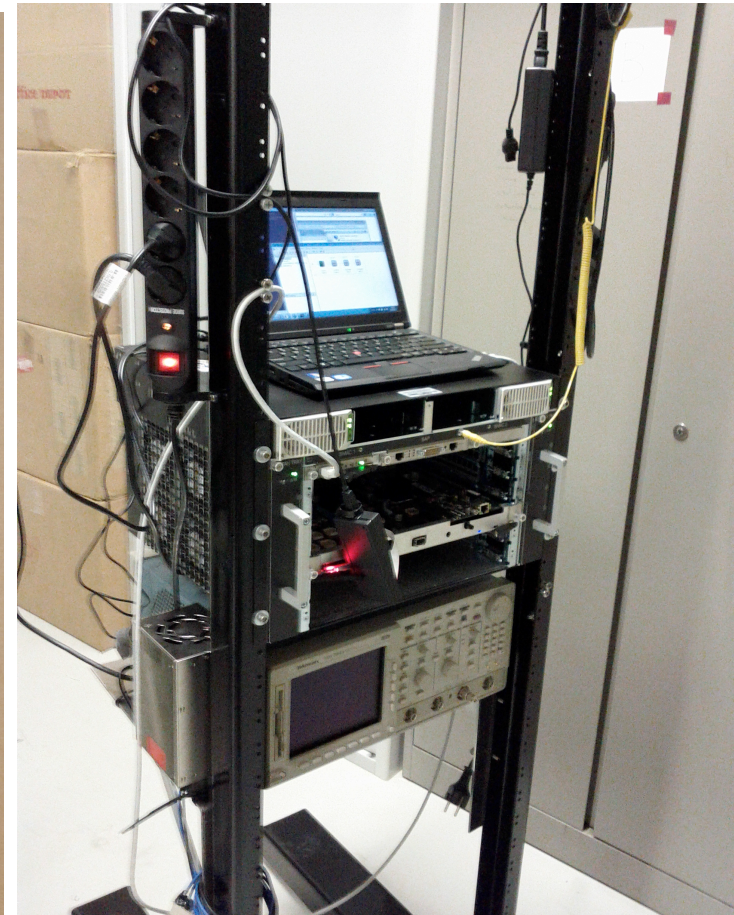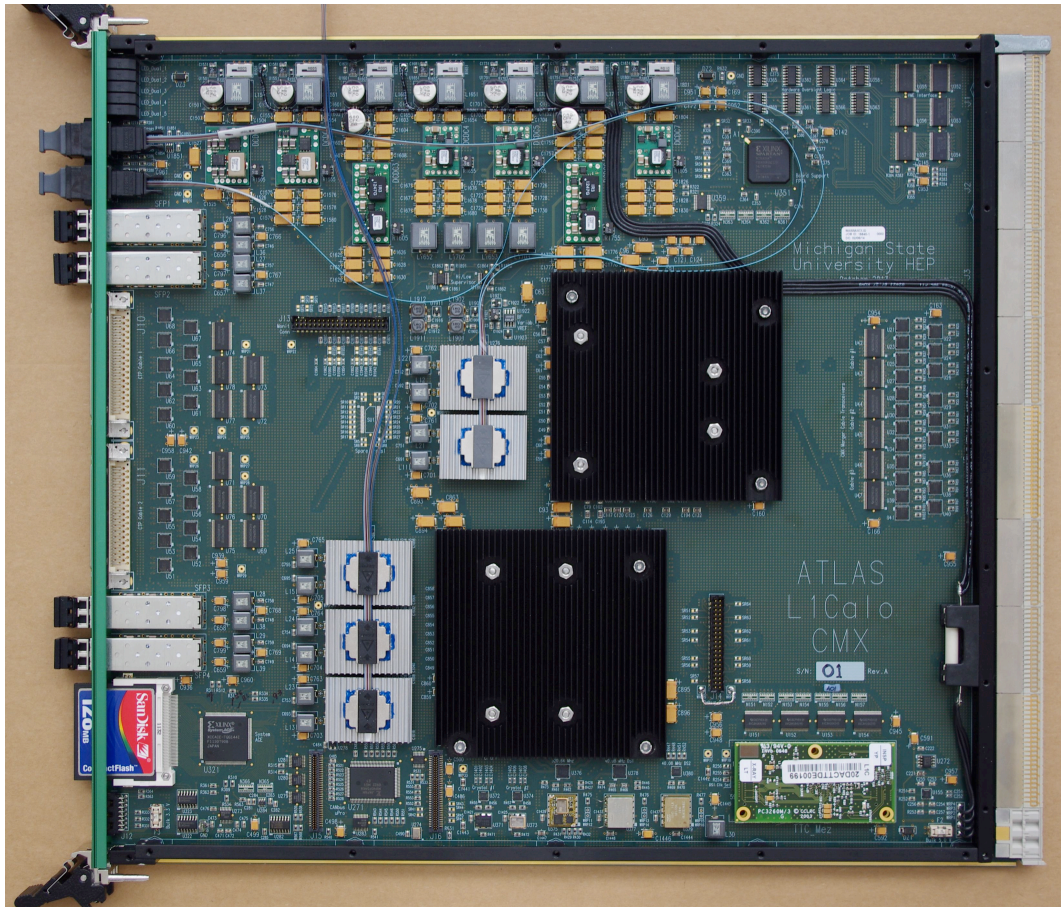
- · reduce sensitivity to pileup and bunch structure, lower noise

Trigger decisions based on trigger objects

(new systems in green)

Selection of new Run 2 modules

New CMX (custom 9U module)

·   merges trigger objects from existing processor modules
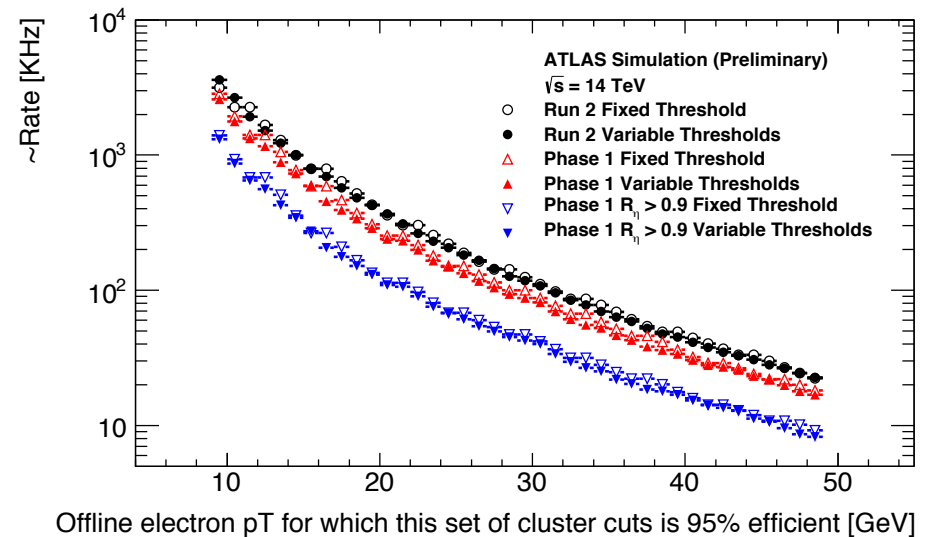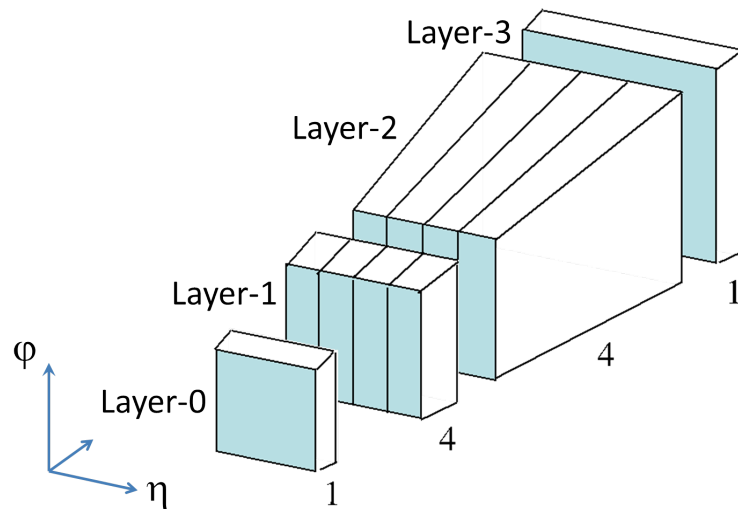
L1Topo ATCA module

·   all objects on single module

Phase 1 (Run 3) system

Same latency for trigger decision

Higher granularity information and segmentation in depth from Liquid Argon

- granularity 0.025×0.1 in η and ϕ for e, γ and τ in middle layers in depth

Allows shower shape cuts for e, γ and τ

- lateral R_η – relating central core to immediate surroundings
- depth f_3 – relating back sampling to whole

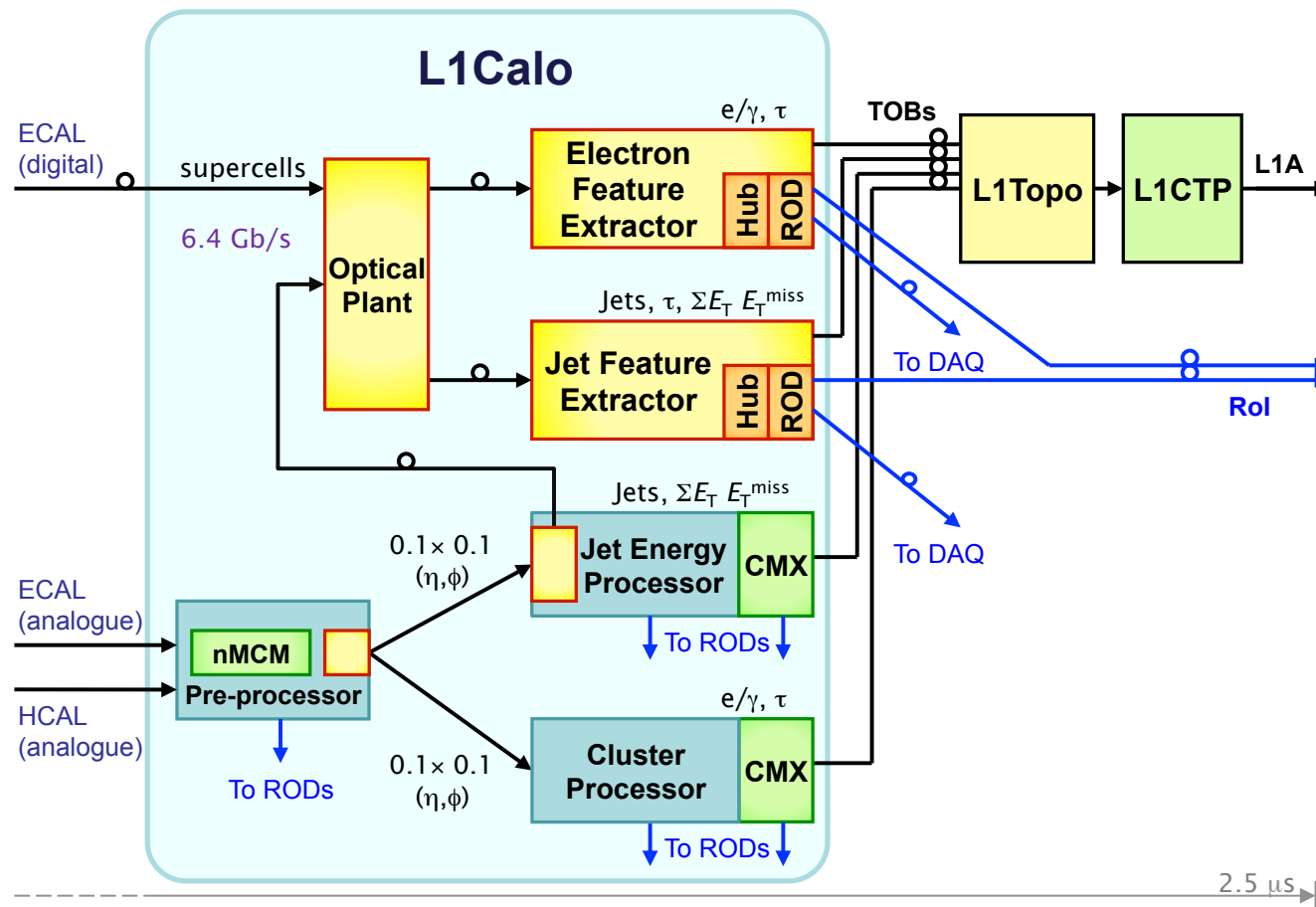0.1×0.1 granularity higher precision energies for jets, ΣE_T, ΣE_T^{miss}

- improved noise rejection and allows Gaussian weighting *etc.*

Phase 1 Liquid Argon upgrades
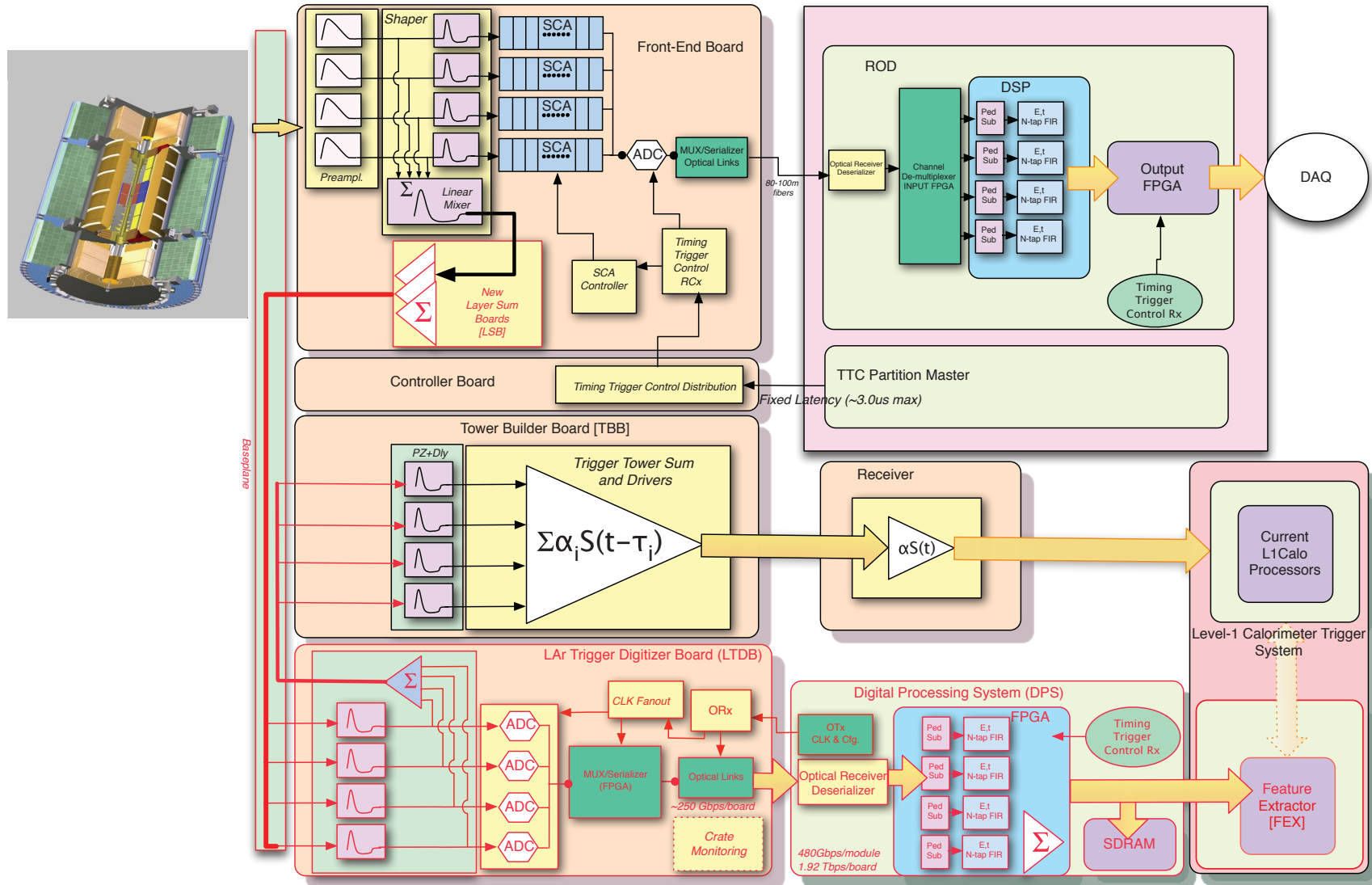
(new components in red)

Phase 1 system (initial)

L1Calo

ECAL (digital) — supercells — 6.4 Gb/s — **Optical Plant**

Electron Feature Extractor — Hub — ROD — e/γ, τ — TOBs

Jet Feature Extractor — Hub — ROD — Jets, τ, ΣE_T E_T^{miss}

L1Topo — **L1CTP** — L1A

To DAQ — RoI — To DAQ

ECAL (analogue) — **nMCM** — **Pre-processor**

HCAL (analogue)

To RODs

0.1×0.1 (η, ϕ) — **Jet Energy Processor** — CMX — Jets, ΣE_T E_T^{miss} — To RODs

0.1×0.1 (η, ϕ) — **Cluster Processor** — CMX — e/γ, τ — To RODs

2.5 μs

(new systems in yellow and orange)

Run 2 system initially continues in parallel

· then gracefully retired, removing CP system and old inputs to L1Topo

New systems

Inputs from 124 LTDB in Liquid Argon (maximum of 124 DPS AMCs) and 32 JEMs

- too many links for all data in a single FPGA…

eFEX

Processes e, γ and τ in window size of 0.3×0.3

Digital Super Cells from Liquid Argon and hadronic Towers via original L1Calo

- ~34000 Super Cells @ 10 bit precision, ~3000 Towers @ 10 bit
- over 1/3 Mbit/event before duplication

jFEX

Processes jets, ΣE_T, ΣE_T^{miss}

0.1×0.1 granularity, jets up to 0.9×0.9
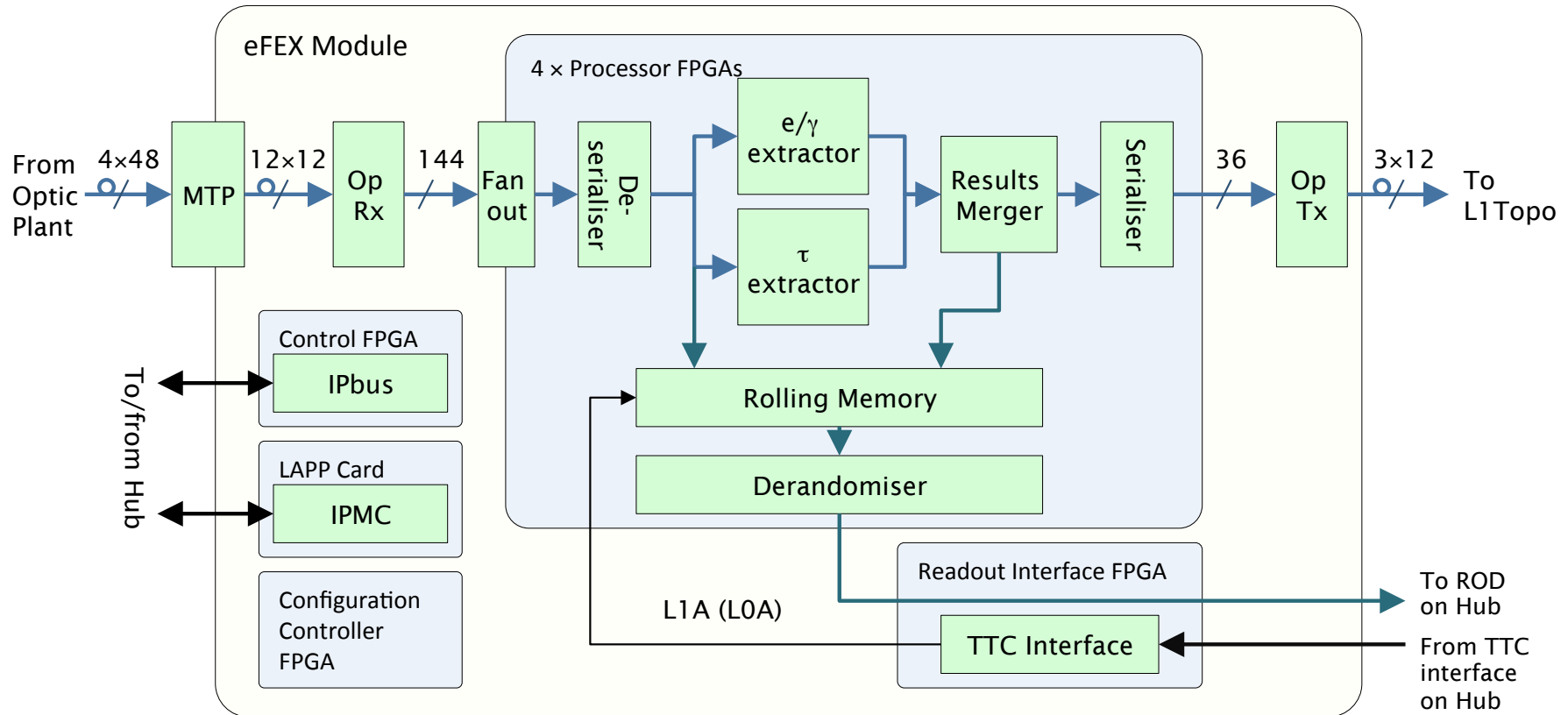
(gFEX

0.2×0.2 granularity

- jets up to 1.8×1.8
- η rings for improved pileup subtraction

Under consideration as separate modules or as equivalent functionality in jFEX)

eFEX overview

Data input to eFEX

ECAL fibres

- 1-4-4-1 Super Cells per 0.1×0.1 ($\eta \times \phi$) Tower
- BCMUX $\Rightarrow 2 \times 1$ ($\eta \times \phi$) Towers / fibre

HCAL fibres

- Towers of 0.1×0.1 summed in depth
- 4×2 ($\eta \times \phi$) towers/fibre

Overlapping windows $\Rightarrow$ data sharing…

Fan out between modules and crates

- 2–1 fan out at source (ECAL DPS + HCAL solution)
- 4–1 fan out via 2–1 passive optical splitting

Fan out between FPGAs

- 2–1 fan out via PMA loopback in FPGA transceivers, retransmitted after equalisation, before decoding
- 4–1 fan out via discrete high-speed buffers – improved signal quality & latency
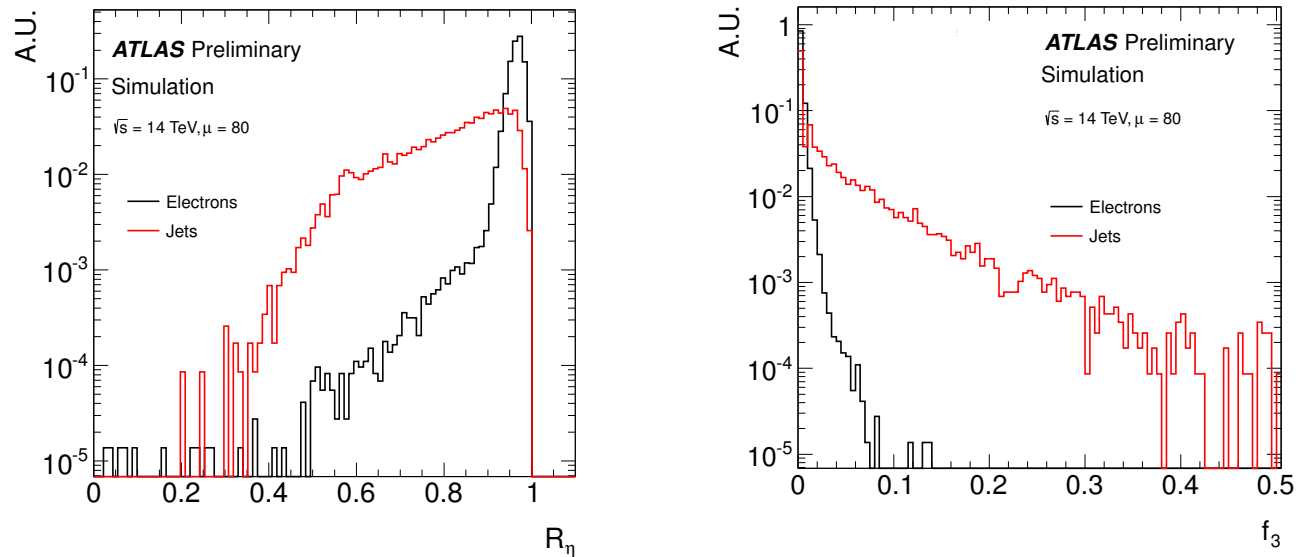- *use latter for all on-board fan out if density allows*
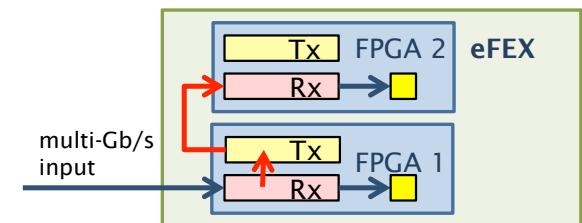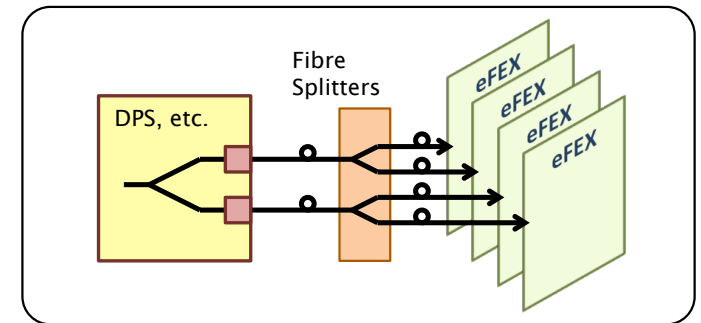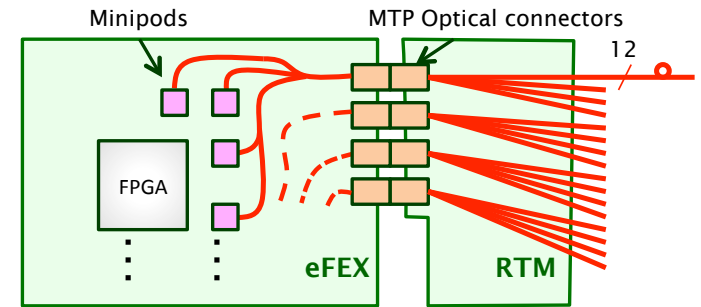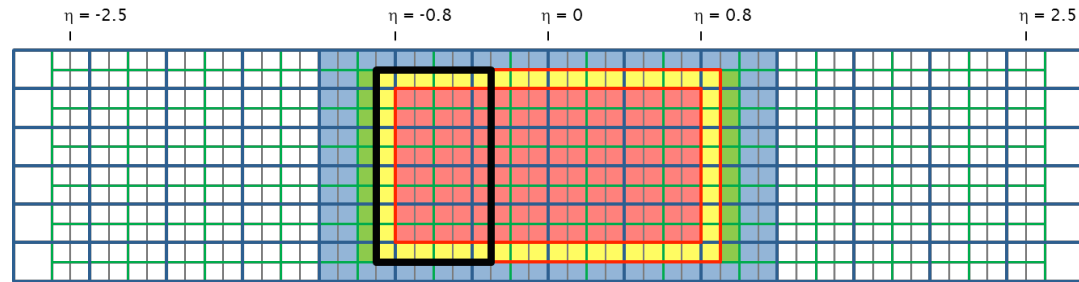
eFEX algorithms

70 GeV electron hitting a single Tower in current L1Calo and in Phase 1 L1Calo
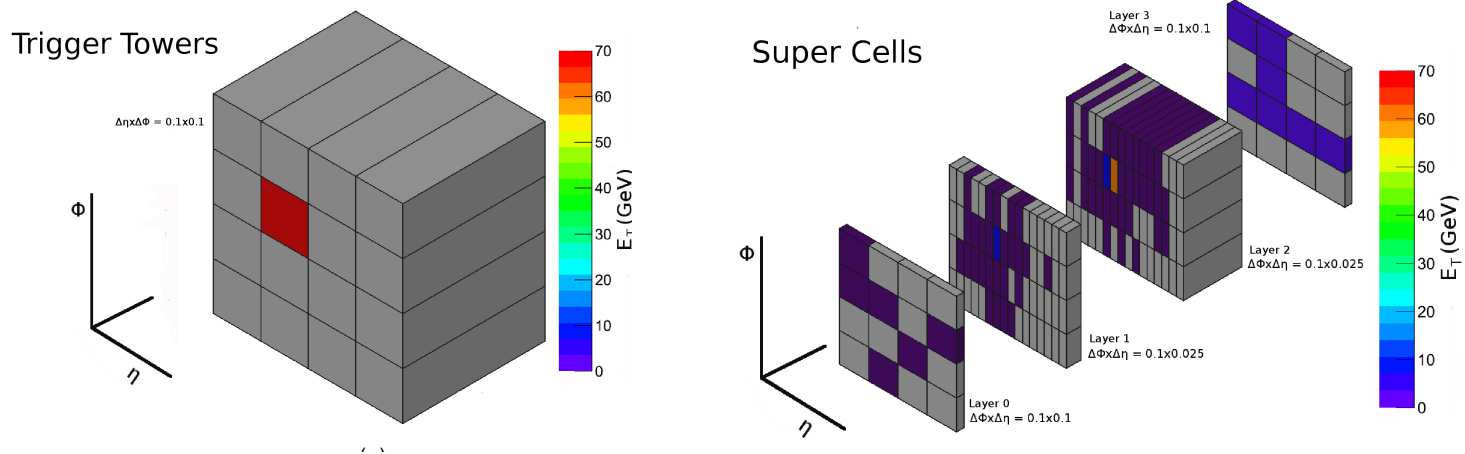
Lateral R_η and depth f_3 discriminants for electrons and jets with $p_T > 20$ GeV

eFEX processing area

eFEX processes maximum core area of 1.6–1.7 × 0.8 ($\eta \times \phi$)

- window size of 0.3 × 0.3 ⇒ module environment of 1.8 × 1.0
- 2 × 1 ($\eta \times \phi$) ECAL towers/fibre: 100 fibres from ECAL = 9 Minipods
- 4 × 2 ($\eta \times \phi$) HCAL towers/fibre: 36 fibres from HCAL = 3 Minipods

4 FPGAs, each processing environment of 0.6 × 1.0 ($\eta \times \phi$)

- per FPGA: 40 ECAL fibres + 18 HCAL fibres + 2 spares = 60
- spares: extra resources for regions where input mapping more complex

Target device = XC7VX550T-FFG1927: 80 GTH

Fan out between FPGAs

60 → 1 FPGA (including 8 spares)

72 → 2 FPGAs

12 → 3 FPGAs

230 multi-Gb/s input tracks on PCB

Link speed

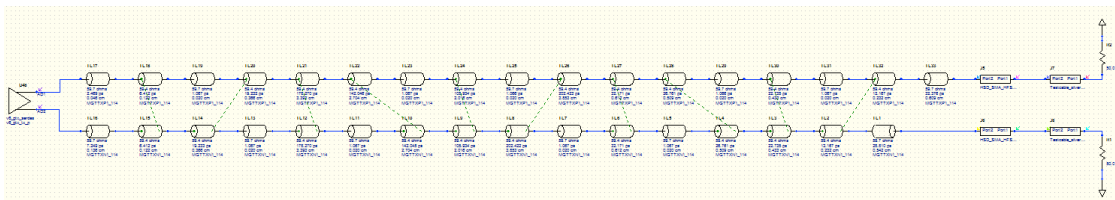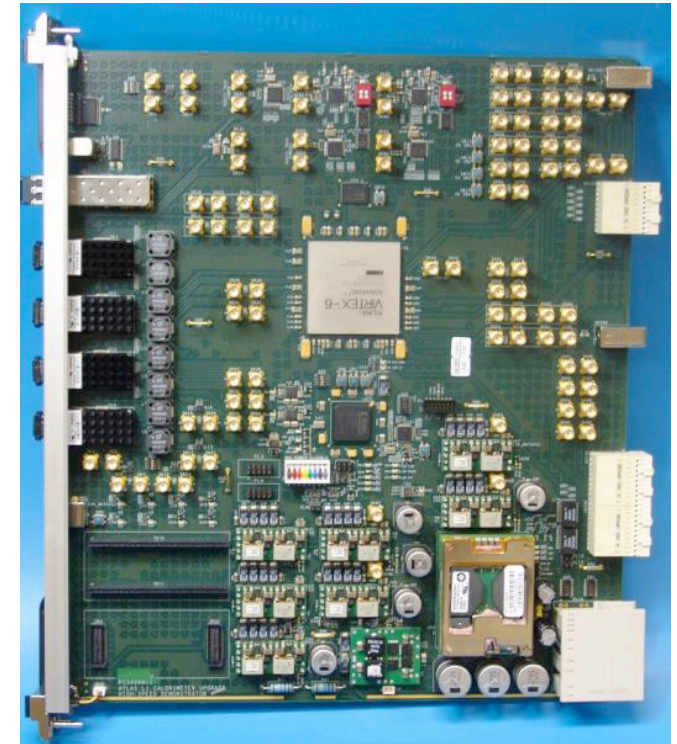Ideally all links should be run as fast as possible

- · link speed directly affects input mapping

Constraint comes from the many fan-out tracks on PCB

- · hence baseline input link speed of 6.4 Gb/s

High Speed Demonstrator with many SMA connectors built to allow structured investigation into high-speed design

- · compare simulation with measurements

Results suggest that higher input link speeds will be possible

- · but must be verified in hardware

System tests of first prototypes scheduled in latter half of 2015

Decision on link speed only possible after this

eFEX output to L1Topo

Merging $\Rightarrow$ prioritisation & sorting of data

- complexity to be defined
- *latency constraint*

Ensure eFEX can populate full bandwidth to L1Topo with useful data
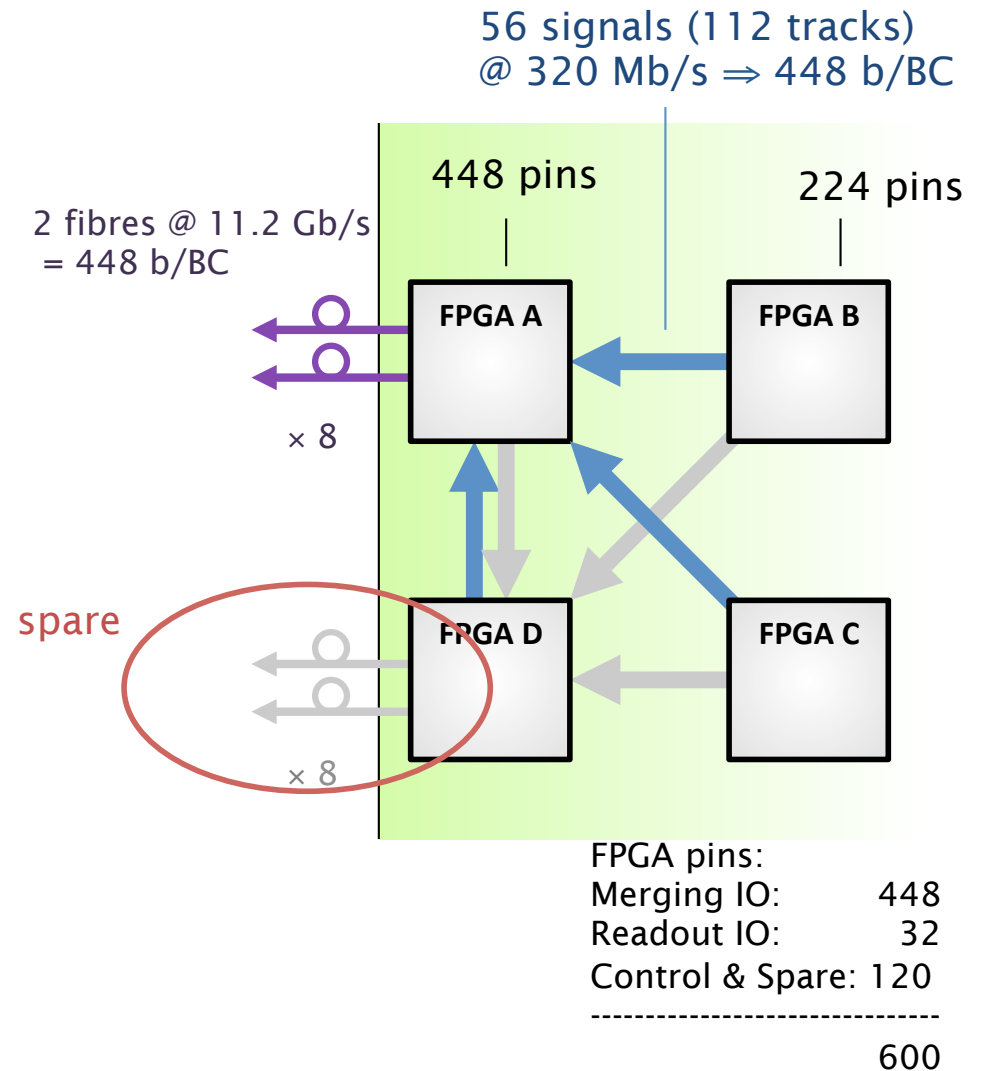
- merge all data in single location
- allow all data to be provided by any 1 FPGA

Speed of FPGA–FPGA links is compromise between latency and number of links
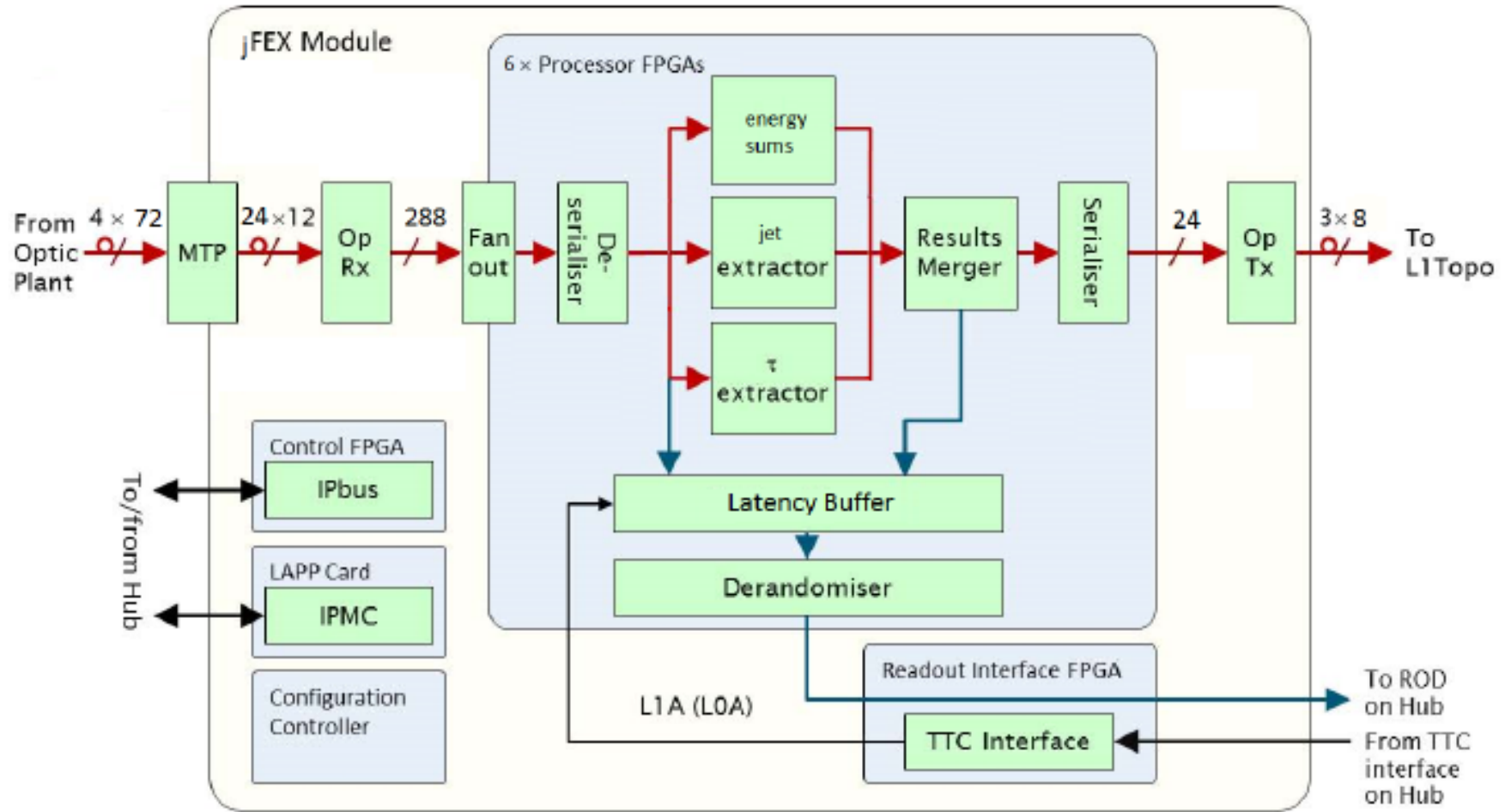
- most demanding case considered: 2 fibres → L1Topo FPGA @ 11.2 Gb/s

Upgrade path: 2 spare fibres from second FPGA

- too demanding for single FPGA
- dual star network on board

56 signals (112 tracks) @ 320 Mb/s $\Rightarrow$ 448 b/BC

448 pins

224 pins

2 fibres @ 11.2 Gb/s = 448 b/BC

FPGA A   FPGA B

× 8

spare

FPGA D   FPGA C

× 8

FPGA pins:
Merging IO: 448
Readout IO: 32
Control & Spare: 120

                   600

jFEX overview

jFEX algorithms

Calculate energy sums: E_T, E_t^{miss}
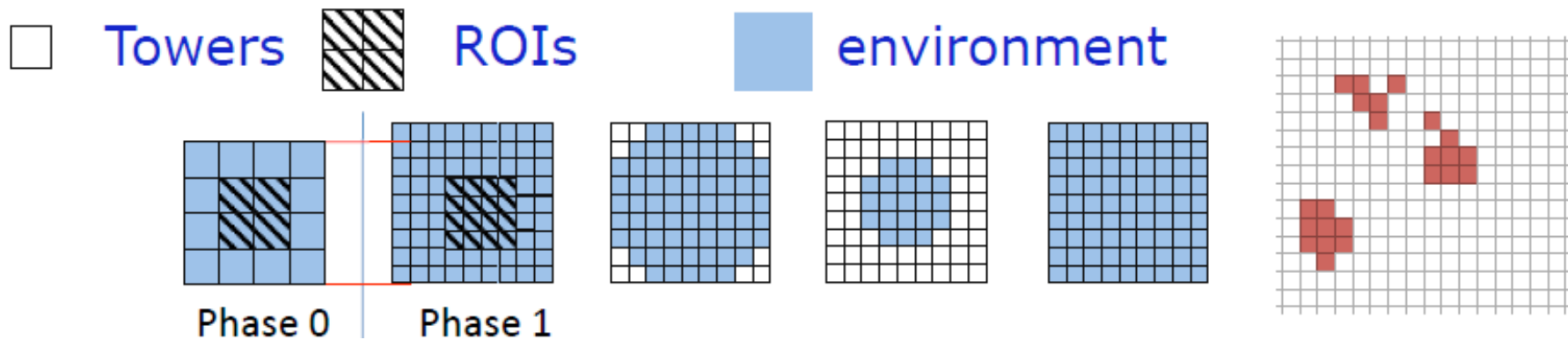
Identify jet and fat τ candidates

Compared to current JEP system

- increased dynamic range
- granularity $\times$ 4
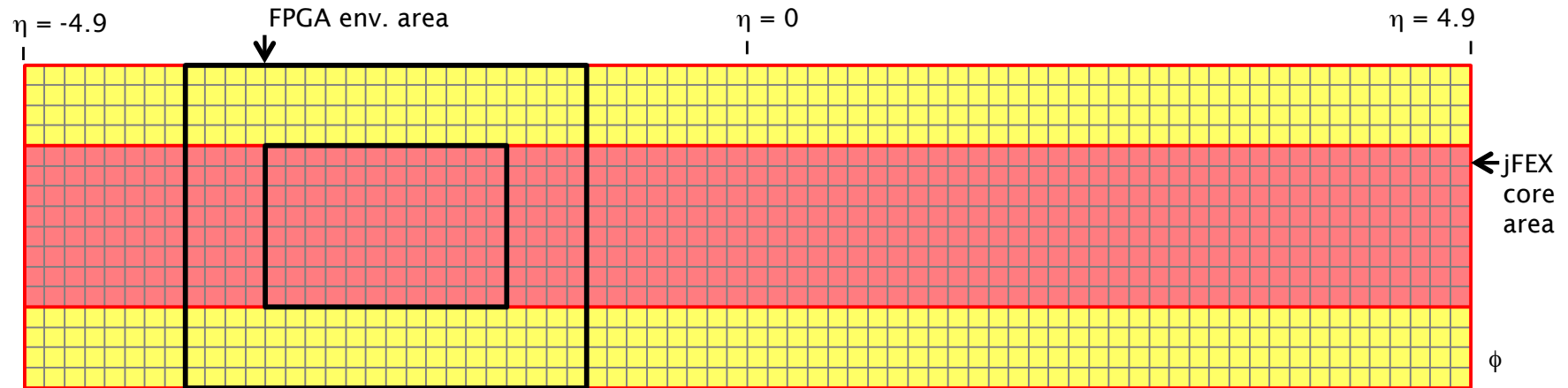- allows flexibility in jet definition (non-square, Gaussian filter, ...)

Increased jet environment

$\leq 0.9 \times 0.9$ ($\eta \times \phi$)

- increases with higher bandwidth or pre-clustering in jFEX, large jets at L1Topo

Towers   ROIs   environment

Phase 0   Phase 1

jFEX processing area

jFEX module processes full ϕ strips (η rings in 'gFEX mode') with large overlap area

- window size $0.9 \times 0.9 \Rightarrow$ environment of 9.8×1.6 ($\eta \times \phi$)
- fan-out between modules at source
- fan-out within module between FPGAs using PMA loopback

8 towers/fibre from ECAL + HCAL: $72 \times 16 \times 2 / 8 = 288$ fibres

- 24×12-way Micropods
- 4×72-way MPO/MTP optical connectors

6 FPGAs, each processing core of 1.2×0.8 ($\eta \times \phi$), environment of 2.0×1.6 ($\eta \times \phi$)

- Per FPGA: 40 ECAL fibres + 40 HCAL fibres = 80

Target devices = XC7VX690T (4) + XC7VX1140T (2 for overlap region)

jFEX high speed option

Advantages of increasing bandwidth

- larger environment: $\pm\ 0.4 \rightarrow \pm\ 0.8\ \eta/\phi$
- larger jets: 1.7 x 1.7 ($\eta \times \phi$)

@ 10Gb/s: 16 towers/fibre and DPS fan-out $\rightarrow$ 3 jFEX

Simplification in jFEX hardware

- 288 Incoming fibres: $\rightarrow$ 186
- 24 Micropods $\rightarrow$ 16
- MPO/MTP: 4 $\rightarrow$ 3 $\times$ 72-way

4 large FPGAs per module

- XC7VX1140T
- $\leq$ 96 high speed links
- core of 1.6 $\times$ 0.8 ($\eta \times \phi$) (central region)
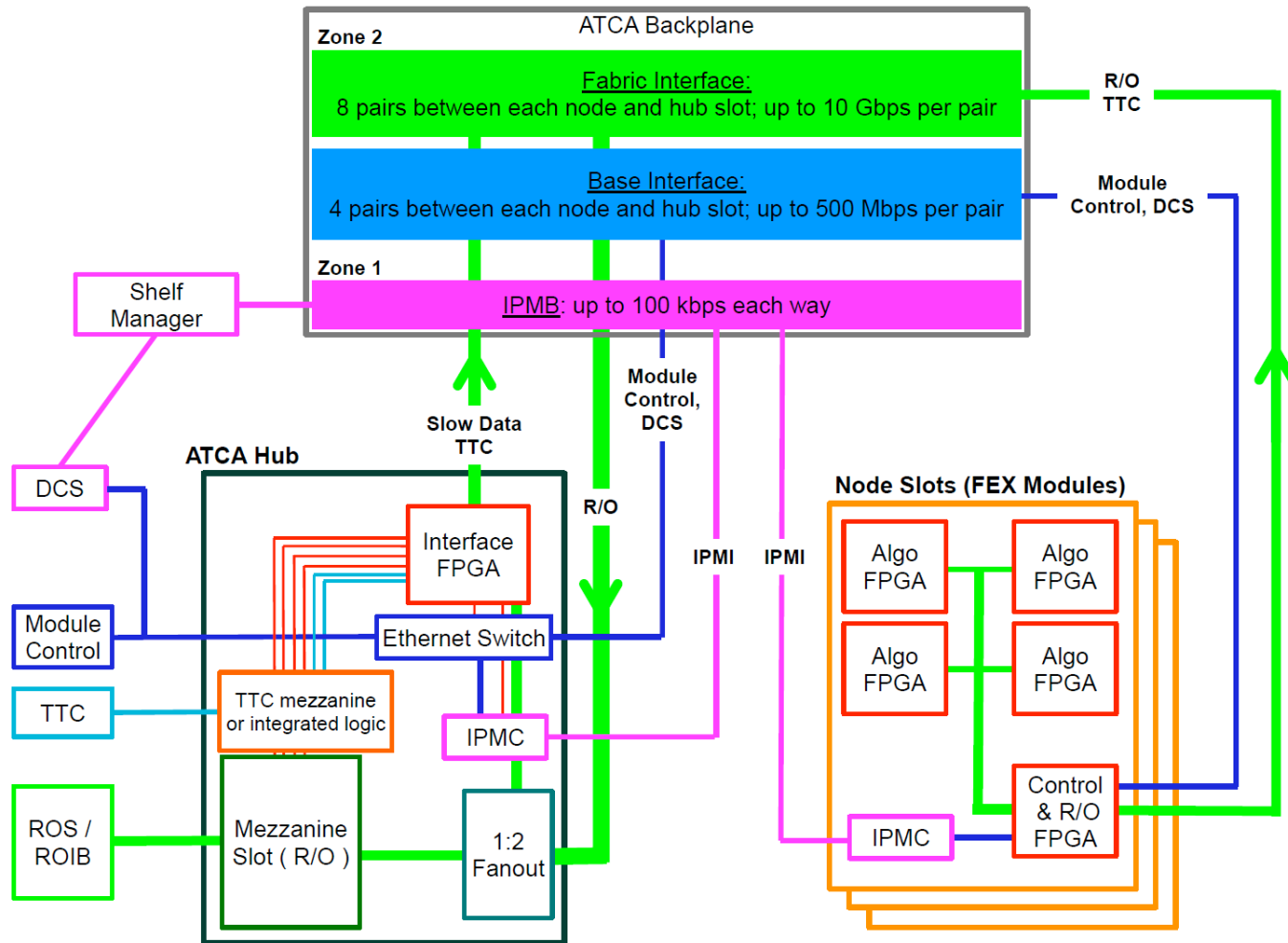- environment $\rightarrow$ 2.4 $\times$ 1.6 ($\eta \times \phi$)

Higher transmission rate strongly favoured by jFEX team

Also strongly preferred for jFEX in gFEX ϕ–ring mode

ATCA shelf infrastructure

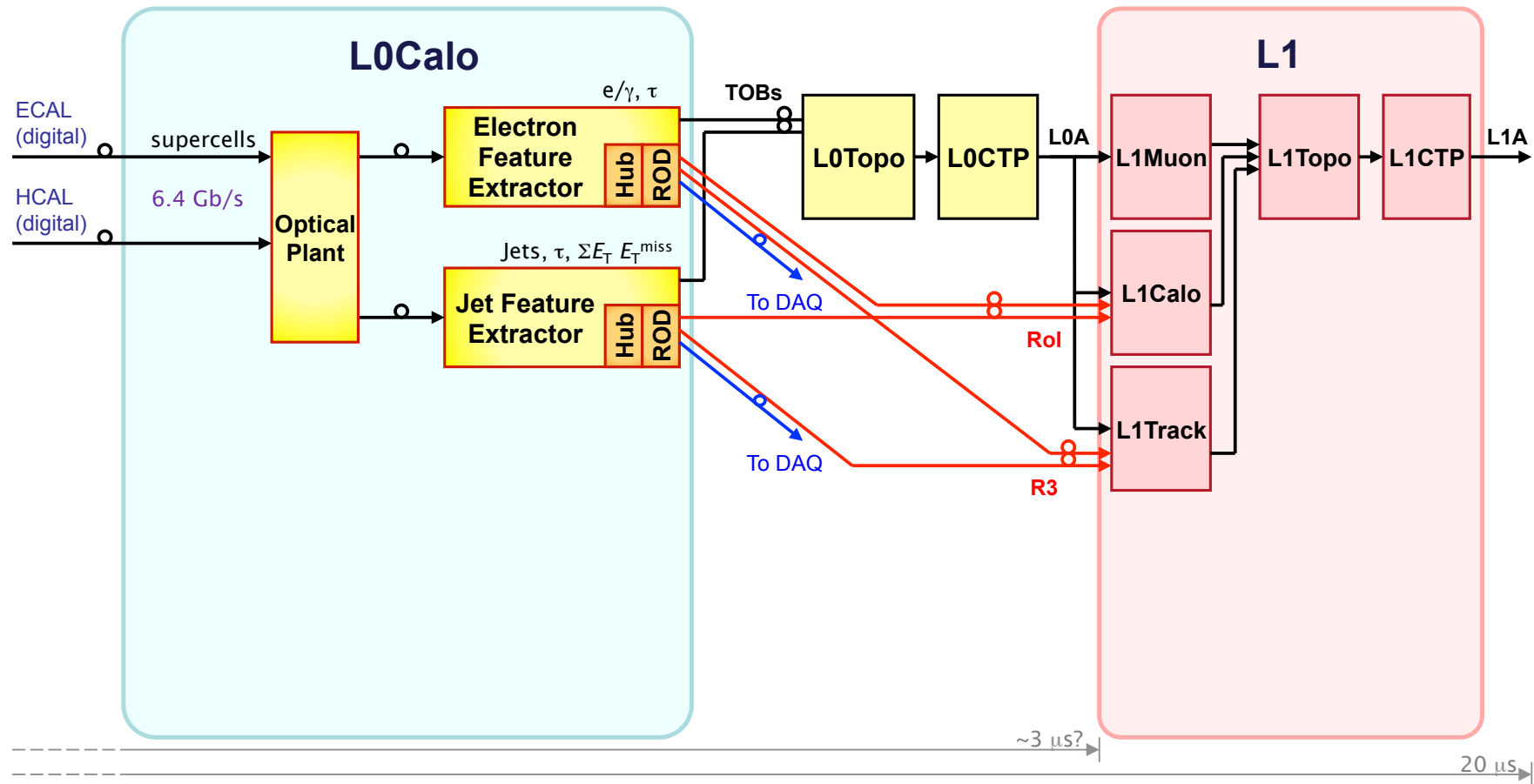## Hub module providing distributed clock and TTC and aggregated read-out

- custom network on Fabric Interface
- ethernet on Base Interface for module control using IPbus

- final parts of original system are retired
- all inputs become digital…

Round up

Upgrades to Pre-Phase 1 systems proceeding apace

Specification of eFEX and jFEX is in process

- · eFEX prototype PDR last month

Module design for eFEX maturing

Design for jFEX strongly affected by link speed

- · and whether ϕ strips or η rings
- · Xilinx UltraScale *vs* V7

Investigation of optimal pile-up correction using jFEX + L1Topo is in progress

Desire for link speeds ~ 10 Gb/s

- · bandwidth $\rightarrow$ L1Topo
- · jets up to 1.8×1.8 in jFEX
- · η rings for improved pileup subtraction in jFEX

But baseline is 6.4 Gb/s

These are complex boards and we need to prove prototypes

Prototypes ready for system tests mid 2015