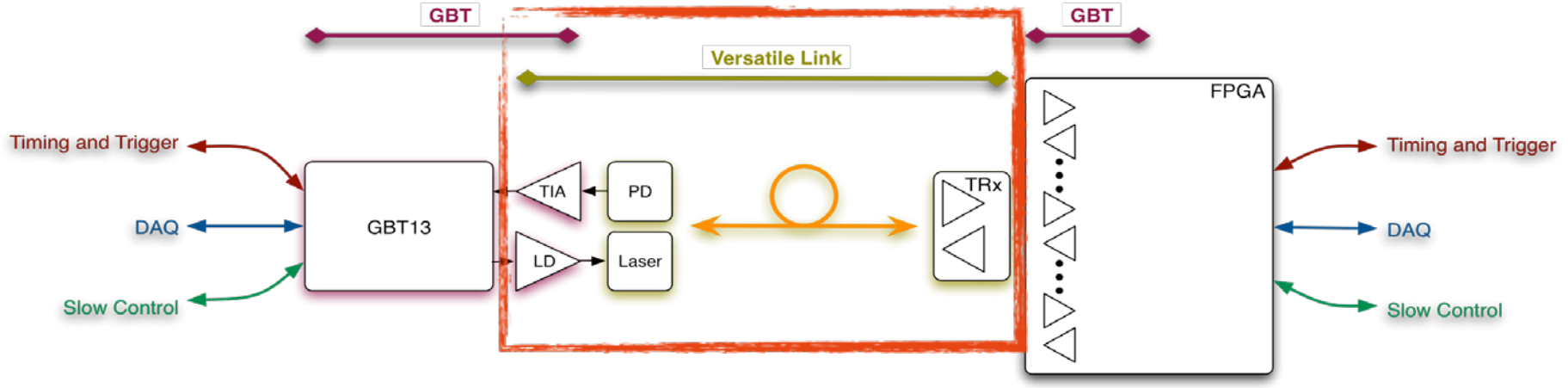
The Versatile Link Project
Present & Future

Francois Vasey, on behalf of the Versatile Link Team

Versatile Link (VL) Project

- Optical Physical layer linking front- to back-end
- Bidirectional, ~5Gbps
- Versatile
  - Multimode (850nm) and Singlemode (1310nm) versions
- Front-end pluggable module

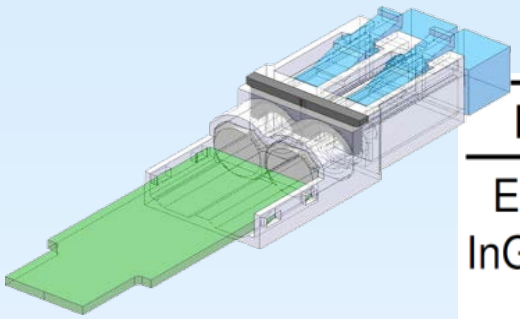
- Joint Project Proposal submitted to ATLAS & CMS upgrade steering groups in 2007 and endorsed in 2008
- Project Kick-off: April 2008
  - ✓ Phase I: Proof of Concept *(18mo)*
  - ✓ Phase II: Feasibility Study *(18mo)*
  - ✓ Phase II: Consolidation *(6mo)*
  - ✓ Phase III: Pre-production readiness *(18mo)*



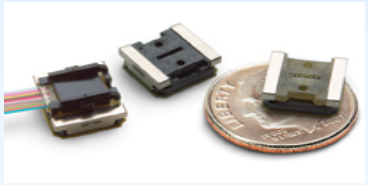
On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

VL Versatility



Front-end VTRx	Fiber	Back-end TRx
EE Laser, 1310 nm InGaAs PIN, 1310 nm	SM G.652a G.652b	LR-SFP+ TRx Board-edge Tx, Rx, TRx Mid-board Rx
VCSEL, 850 nm GaAs PIN, 850 nm	MM OM3 OM4	SR-SFP+ TRx Board-edge Tx, Rx, TRx Mid-board Tx, Rx, TRx



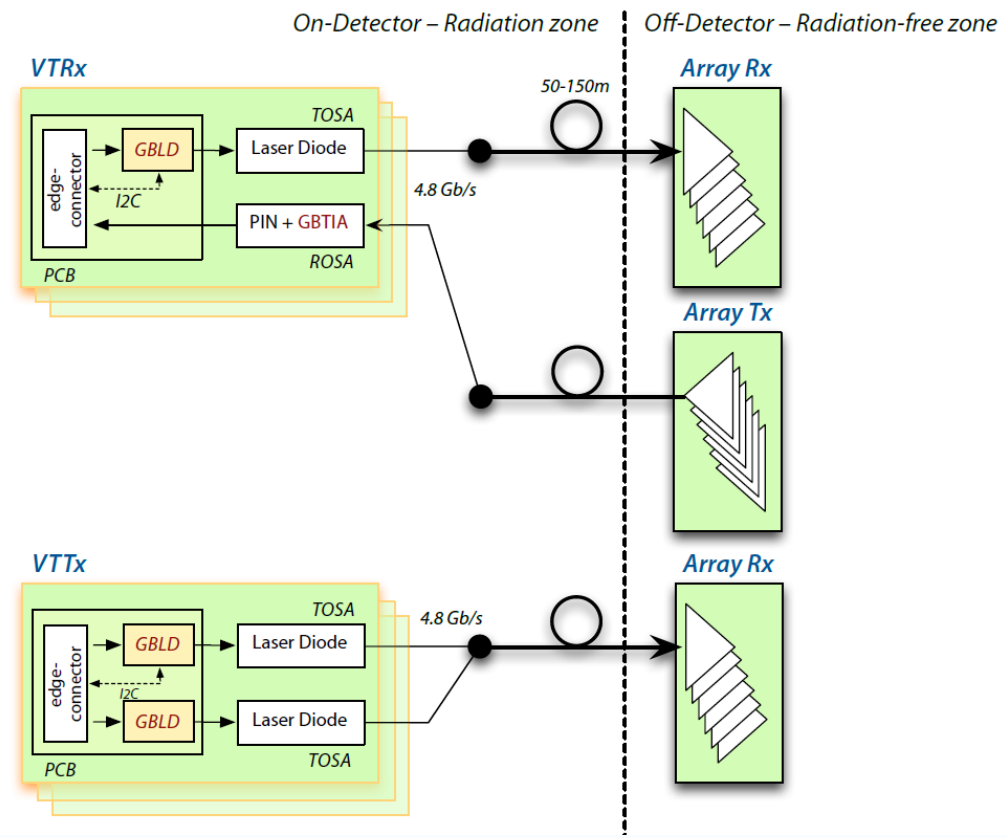
- 2 fiber types
- ~~2~~ 1 rad tol grades
- TRx or TTx FE

Fibre Type	Radiation Tolerance Grade	
	Calorimeter-grade	Tracker-grade
	10 kGy, $5x10^{14}$ n/cm^2	500 kGy, $2x10^{15}$n/cm^2, $1x10^{15}$ h/cm^2
SM	✓	VL+
MM	✓	VL+

francois.vasey@cern.ch on behalf of Versatile Link team

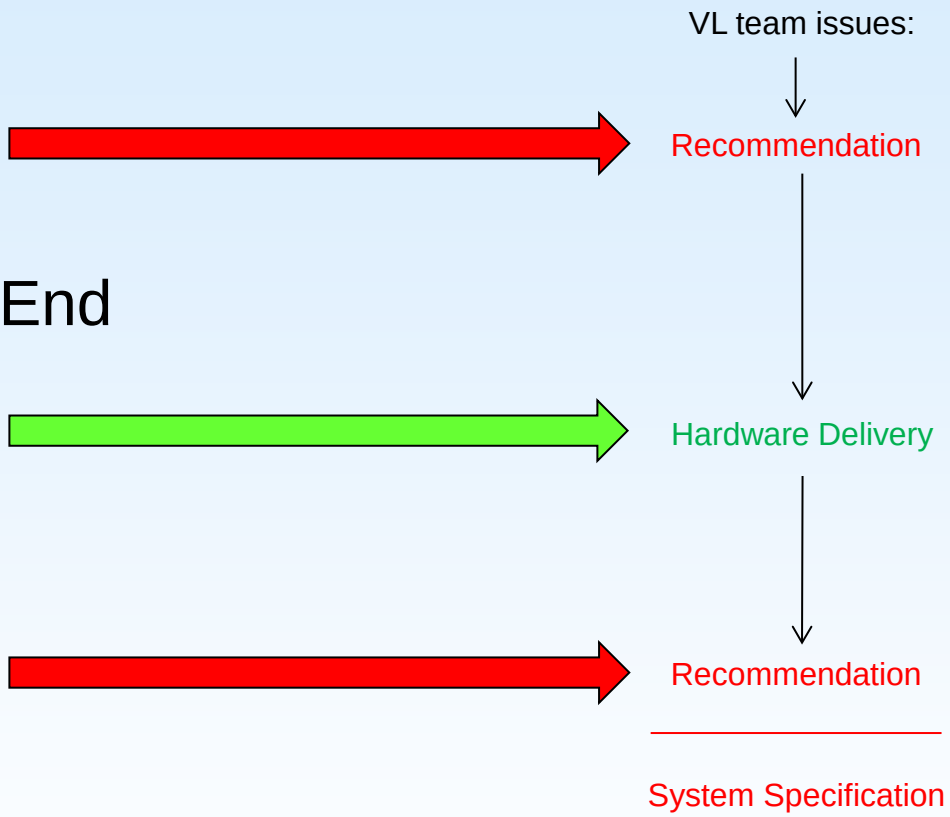
VL Selection Menu

1. Select fibre type
   - SM if legacy SM plant
   - MM otherwise
2. Select directionality of Front-End component
   - Bi-directional: VTRx
   - Uni-directional: VTTx
3. Select Back-End
   - Single or Multi-channel
   - Board-edge or Mid-board



VL Selection Menu (2)

1. Select fibre type
   - SM if legacy SM plant
   - MM otherwise
2. Select directionality of Front-End component
   - Bi-directional: VTRx
   - Uni-directional: VTTx
3. Select Back-End
   - Single or Multi-channel
   - Board-edge or Mid-board



How to build a VL-based optical link

- VL provides:
  - A set of system level and component level specifications

https://edms.cern.ch/nav/P:CERN-0000076379:V0/P:CERN-0000090391:V0/TAB3

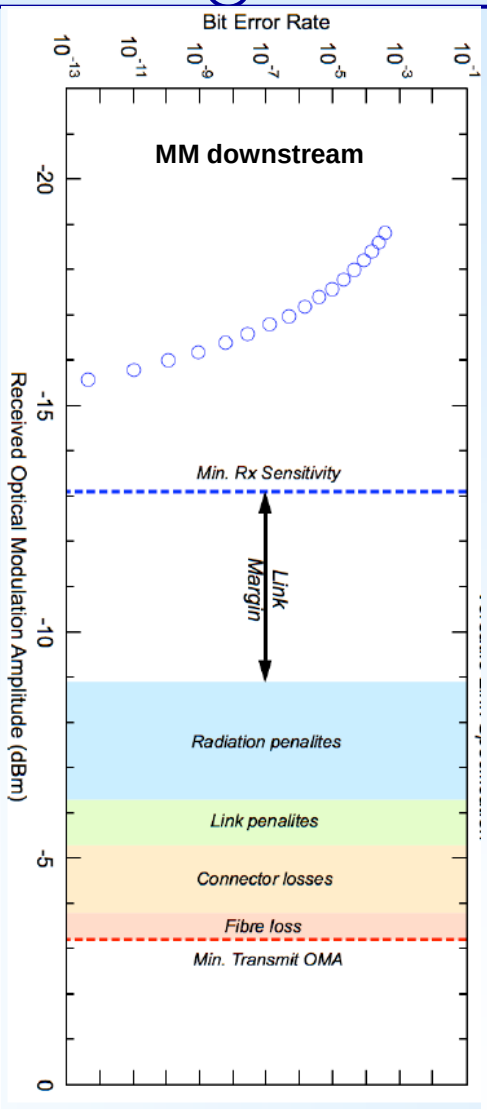
  - A fully qualified and tested VTRx module
  - A recommendation for:
    - Backend Rx module
      - Other choices may be possible but experiments must ensure compatibility with system spec
    - Optical fibre type
      - Other choices may be possible but experiments must ensure compatibility with system spec and radiation tolerance
  - An Application note

https://espace.cern.ch/project-versatile-link/public/Versatile%20Link%20Public%20Documents/Forms/AllItems.aspx

- Experiment provides:
  - Everything except the VTRx/VTTx modules

Versatile Link Power Budget Guideline

	MM up VTx>Rx	MM down Tx>VRx	SM up VTx>Rx	SMdown Tx>VRx
Min. Tx OMA	-5.2 dBm	-3.2 dBm	-5.2 dBm	-5.2 dBm
Max Rx sensitivity	-11.1 dBm	-13.1 dBm	-12.6 dBm	-15.4 dBm
Power budget	**5.9 dB**	**9.9 dB**	**7.4 dB**	**10.2 dB**
Fiber attenuation	0.6 dB	0.6 dB	0.1 dB	0.1 dB
Insertion loss	1.5 dB	1.5 dB	2.0 dB	2.0 dB
Link penalties	1.0 dB	1.0 dB	1.5 dB	1.5 dB
VTx rad. penalty	0 dB	-	0 dB	-
VRx rad. penalty	-	2.5 dB	-	2.5 dB
Fiber rad penalty	0.1 dB	0.1 dB	0 dB	0 dB
Margin	**2.7 dB**	**4.2 dB**	**3.8 dB**	**4.1 dB**



VTRx fixed spec

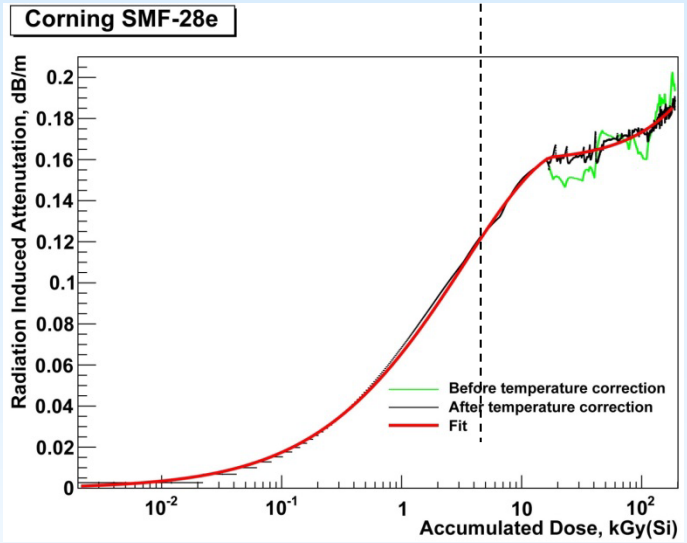
VL Radiation Tolerant Fibre Recommendation

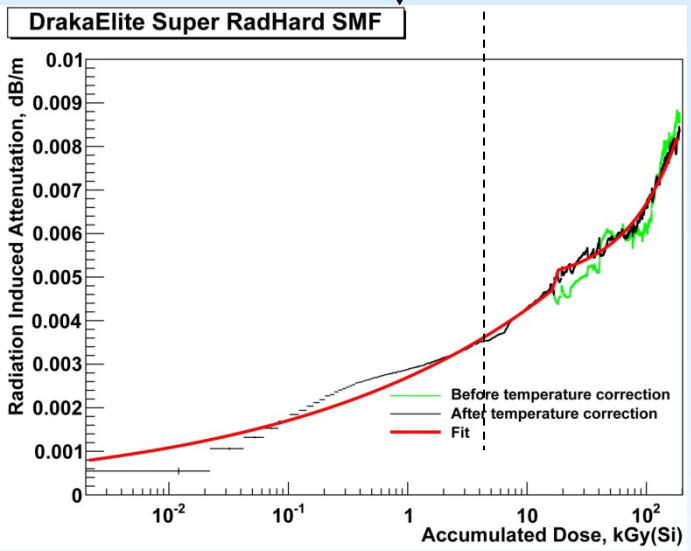
Versatile Link

COTS

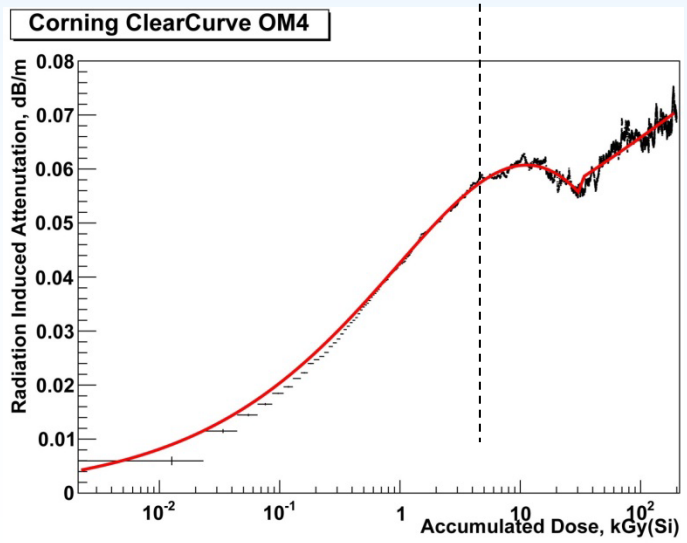
RadHard

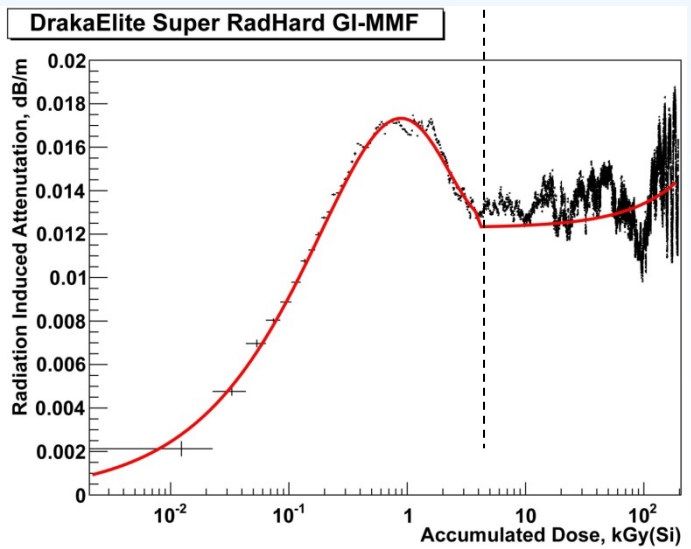
SM





MM





- 0.7 kGy(Si)/hr
- -25 degC
- No annealing shown

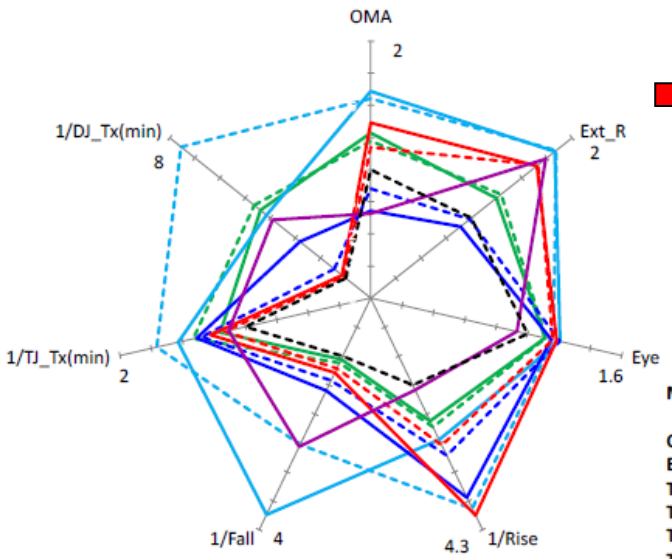
- VL spec: 0.1dB MM
  0 dB SM

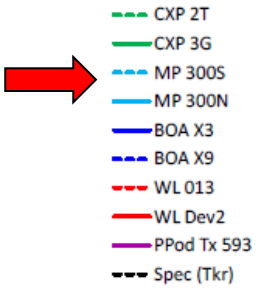
- COTS fibre to be qualified at preform level
- Radhard fibre can be procured as is

VL Backend mid-board Engine Recommendation

Versatile Link

Parallel Optics Transmitter Radar Plot



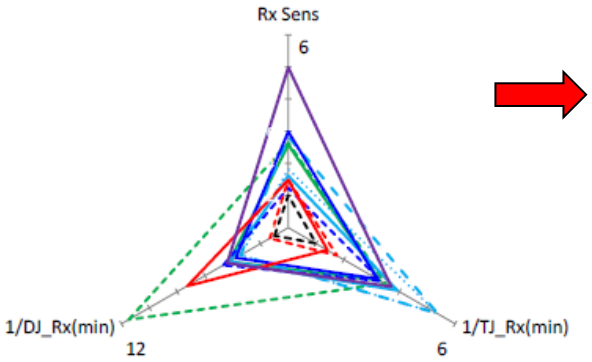


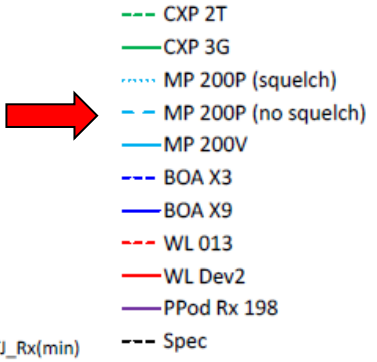
Measurement	Norm
OMA	-1.6 dBm*
Ext. Ratio	3.0 dB
Tx. Eye Opening	60% of OMA
Tx Rise Time	70 ps
Tx Fall Time	70 ps
Tx Total Jitter	0.25 of UI
Tx Deterministic Jitter	0.12 of UI

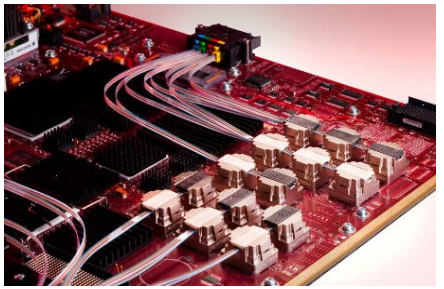
*Tracker Grade Spec

Fig. 15: Tx Channel Average Radar Plot (@5 Gbps)

Parallel Optics Receiver Radar Plot







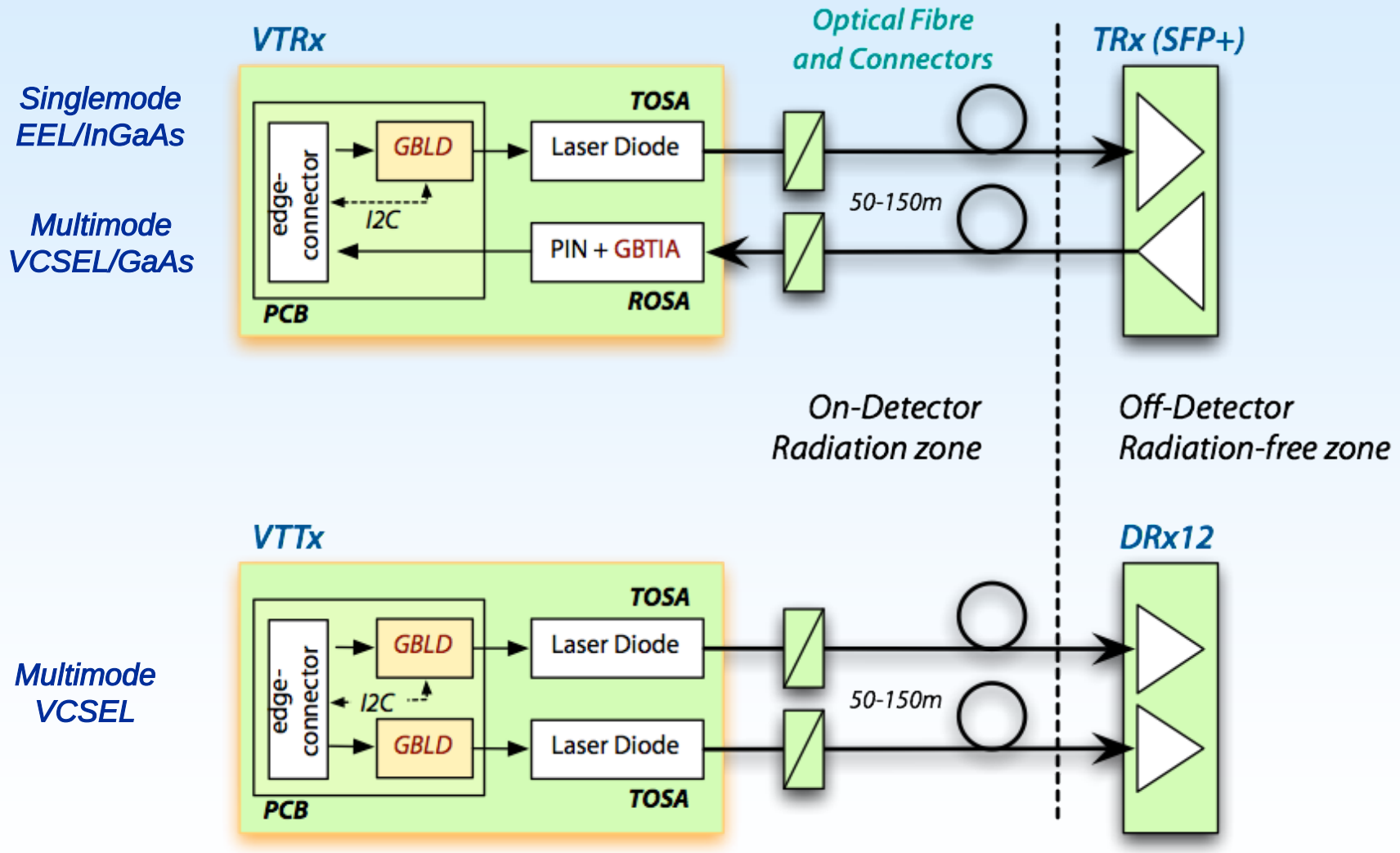
Measurement	Norm
Rx Sensitivity	-11.1 dBm*
Rx Total Jitter	0.34 of UI
Rx Deterministic Jitter	0.14 of UI

*Multimode Fiber System Spec

Fig. 16: Rx Channel Average Radar Plot (@5 Gbps)

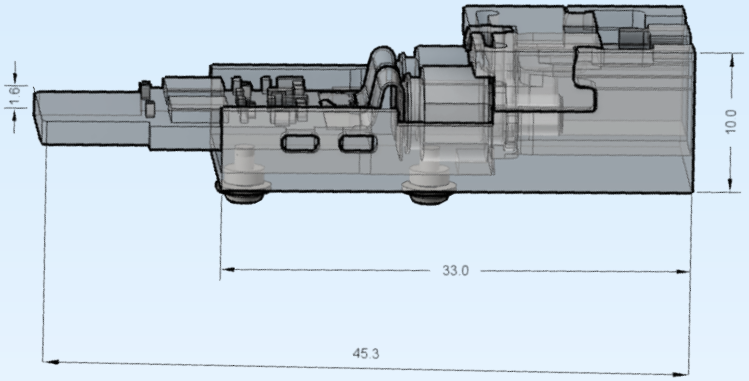
Read section 5.2 of application note !

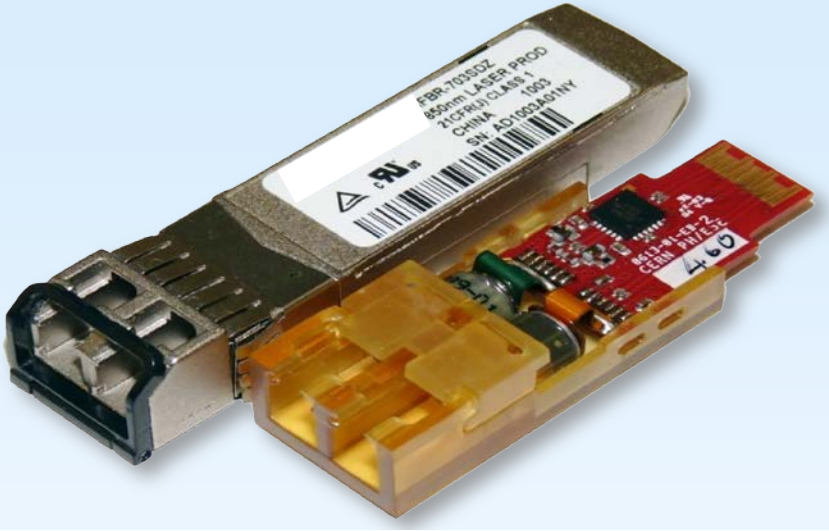
VL Front-End: VTRx or VTTx

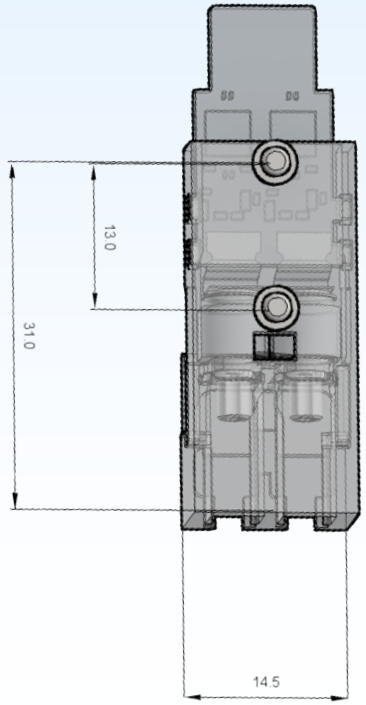


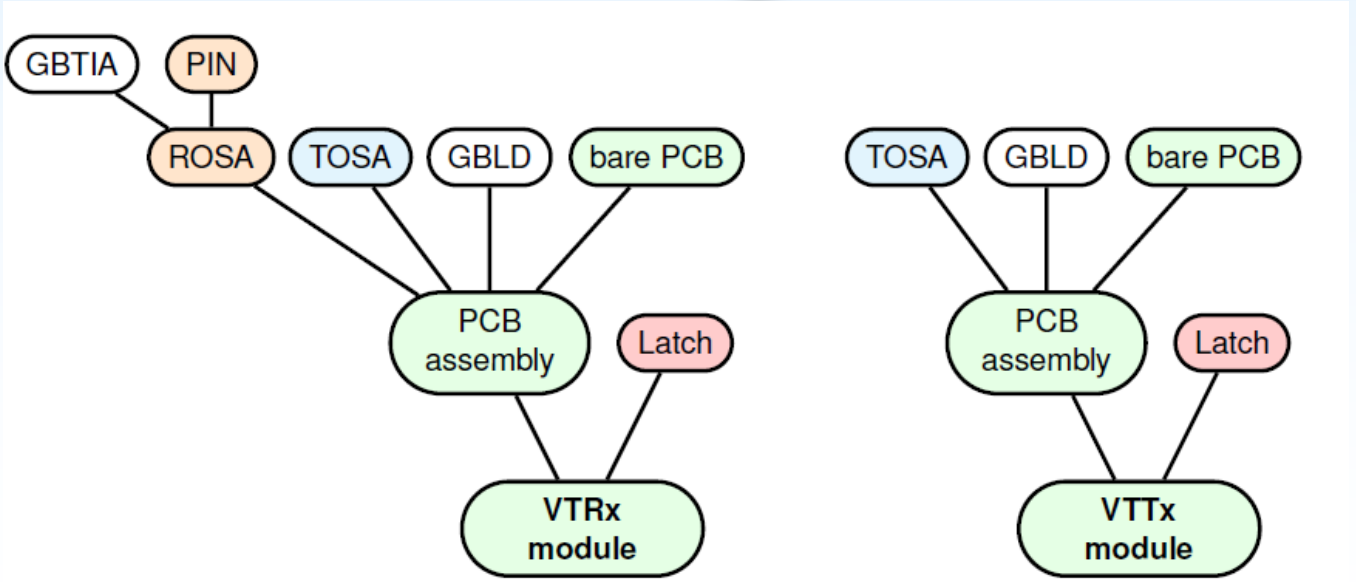
VL only hardware deliverable

Versatile Link

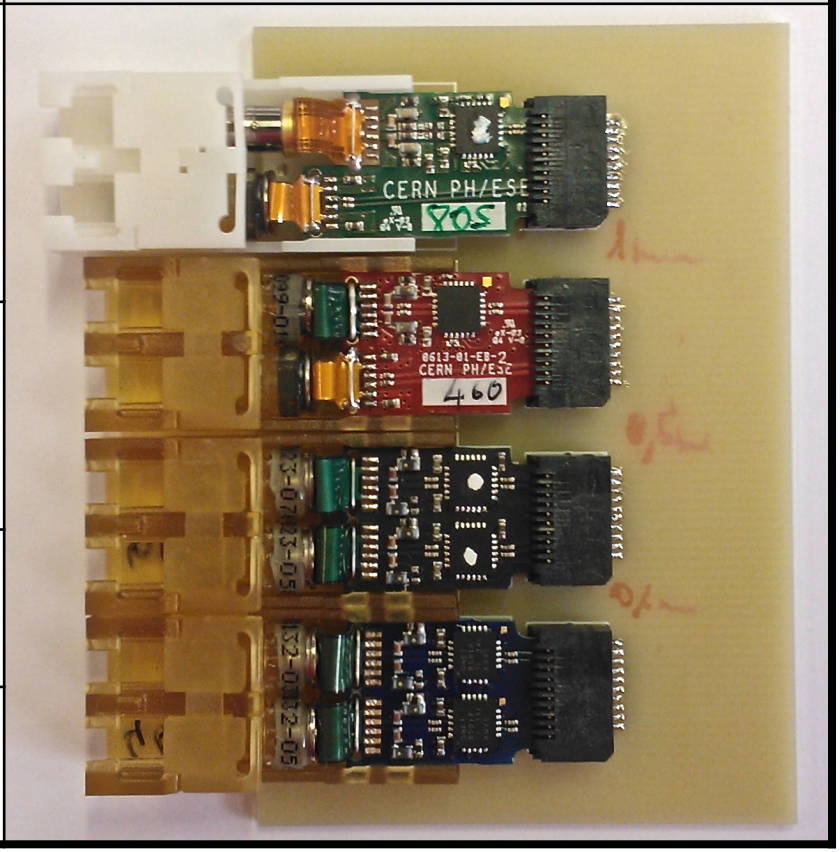






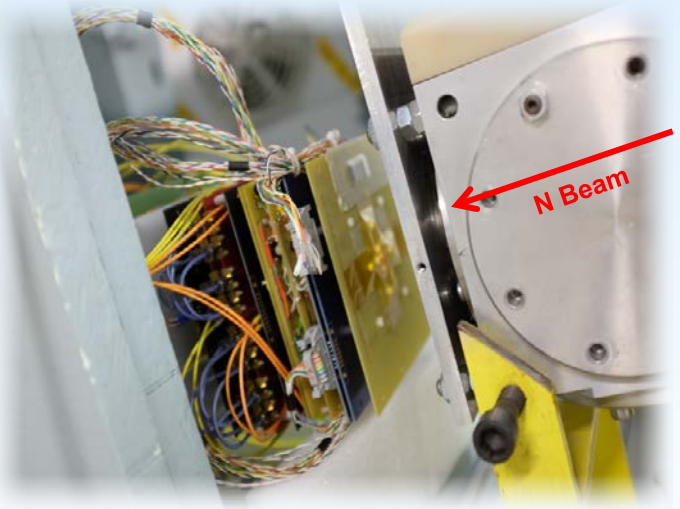


VTXx Variants

Variant	Laser Driver	TOSA	ROSA	Picture
Single-mode VTRx	GBLD v4.1	Edge Emitter Laser	InGaAs GBTIA v2	
Multi-mode VTRx	GBLD v4.1	850 nm VCSEL	GaAs GBTIA v2	
Multi-mode VTTx	GBLD v4.1	850 nm VCSEL	-	
Rad-soft VTTx	ONET8501V	850 nm VCSEL		

VTRx in n-beam

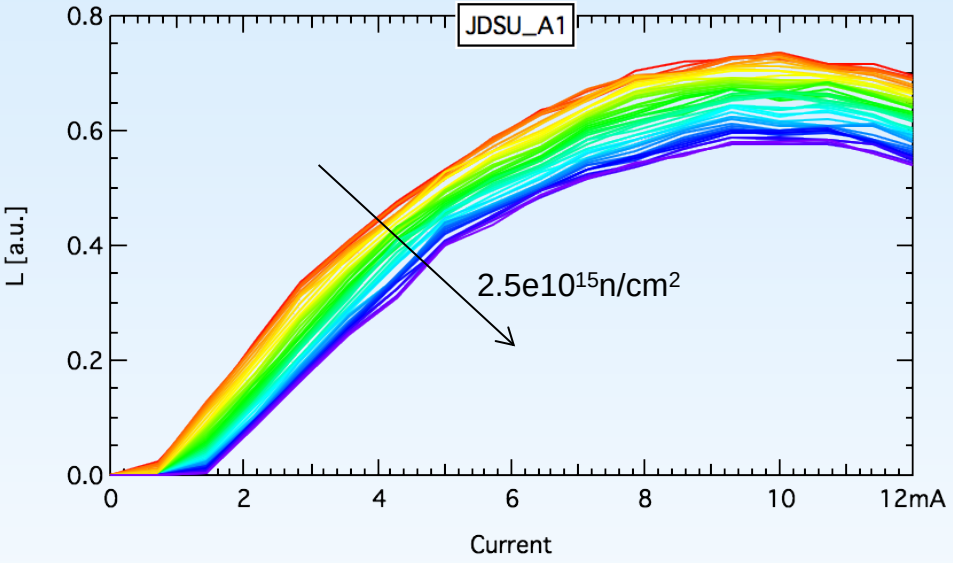
- Final prototype VTRx (SM & MM) exposed to neutron beam at UC Louvain cyclotron facility in Nov. 2013
  - Complex test
  - VTRx in addition to lasers/pins
- Direct comparison between devices irradiated with DC measurements and AC measurements on VTRx
  - Large dataset still being evaluated
- Early results show devices on VTRx behave as expected from static testing



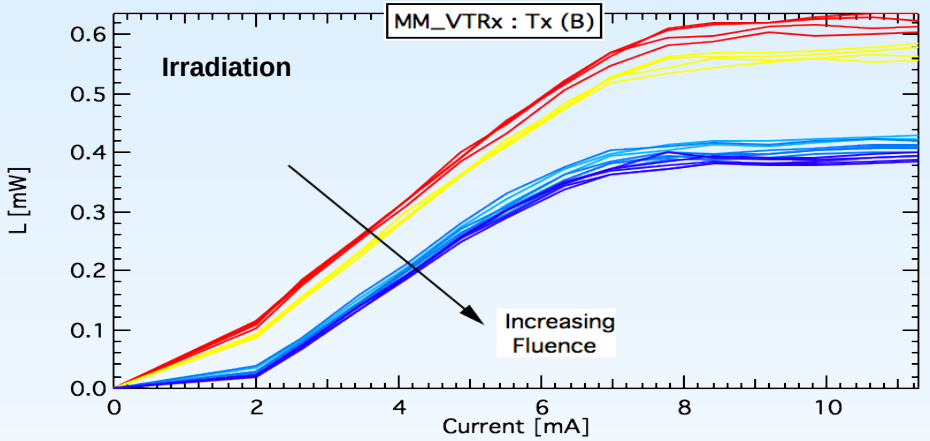
VTRx in n-beam (1: Tx static)

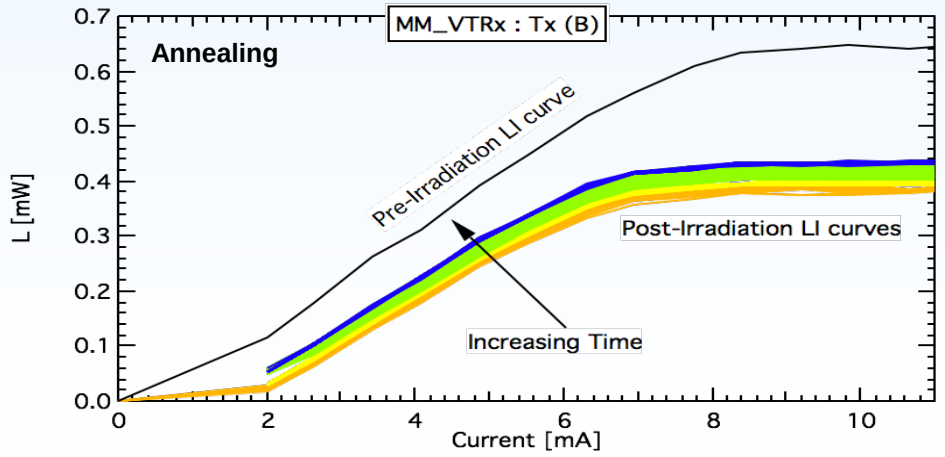
Versatile Link

VCSEL + external current source



VCSEL + GBLD **in VTRx**

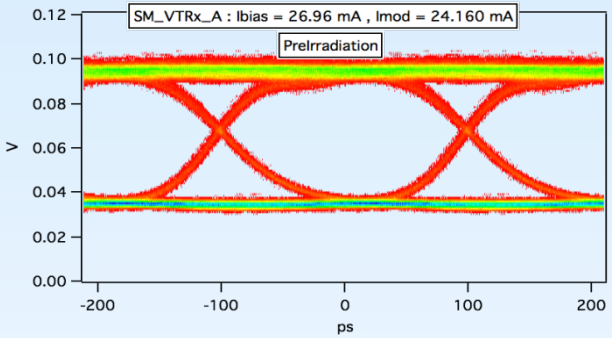


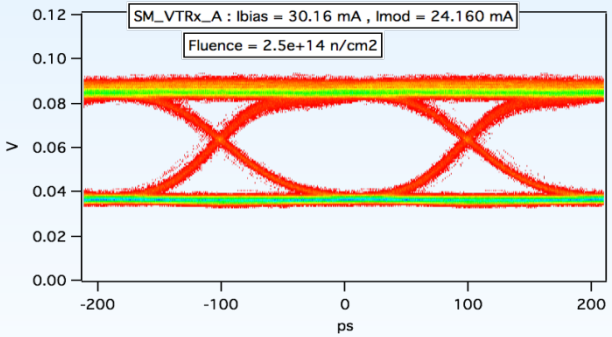


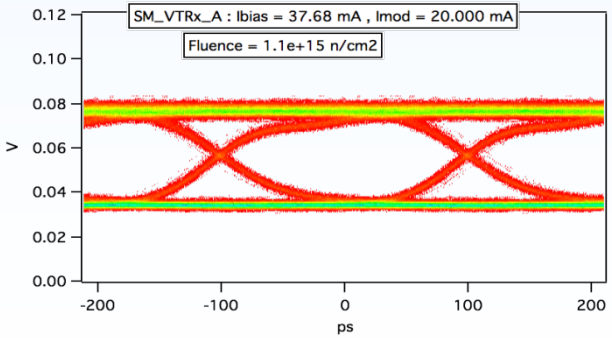
VTRx in n-beam (2: Tx dynamic)

Versatile Link

SM VTRx

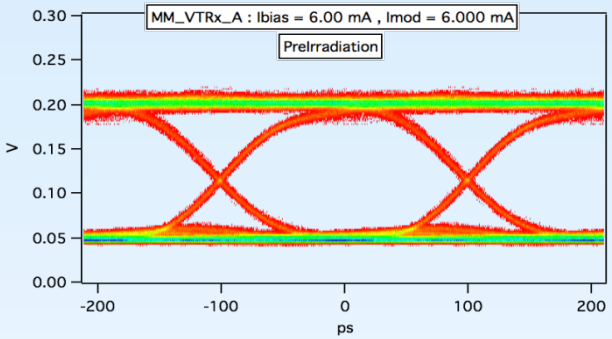


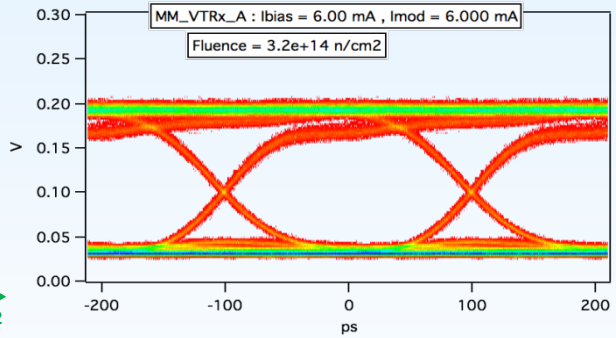


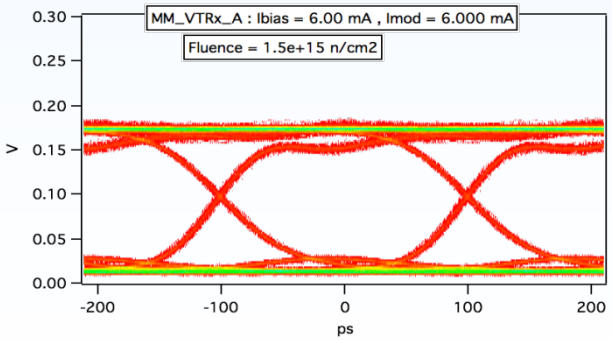


Cal grade: 5×10^{14} n/cm^2

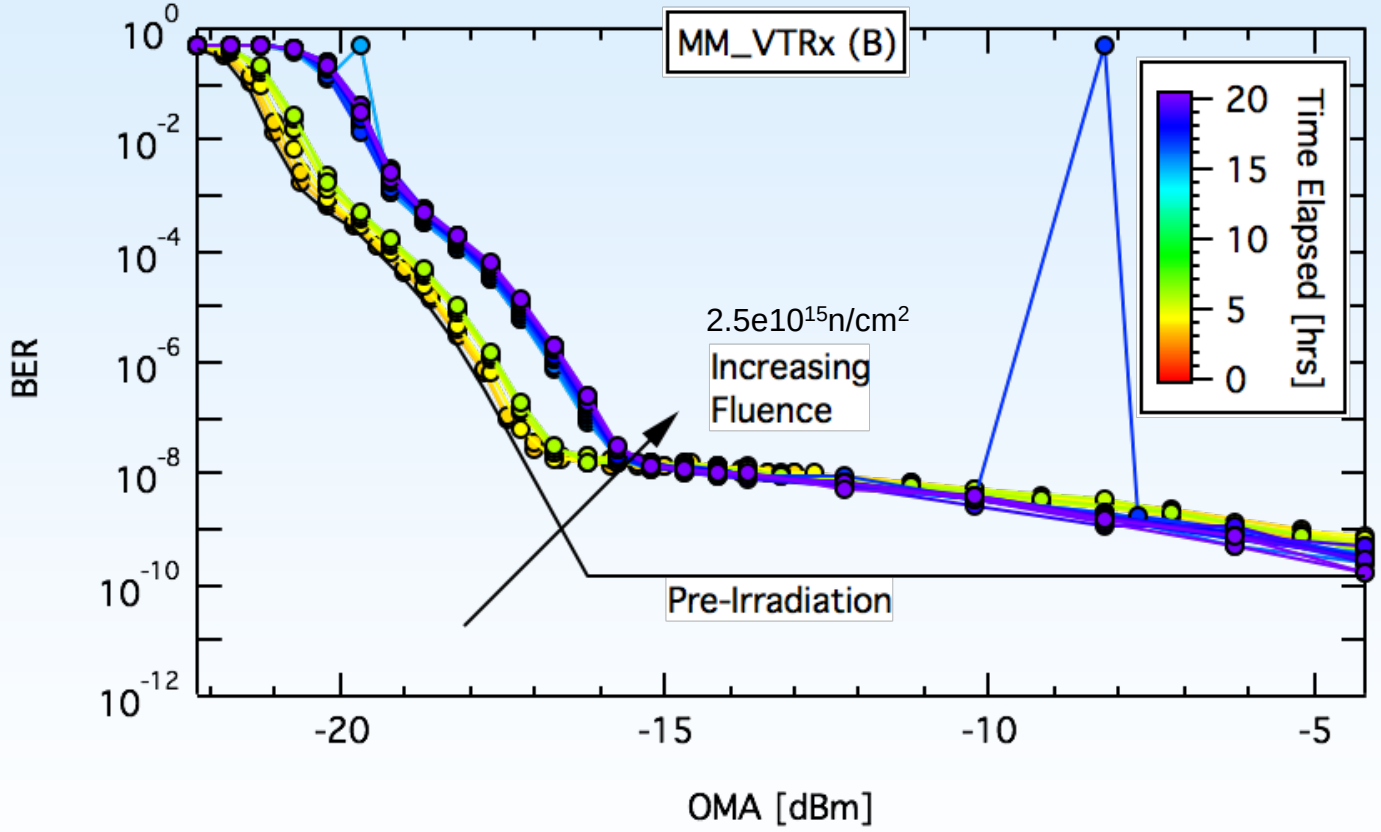
MM VTRx







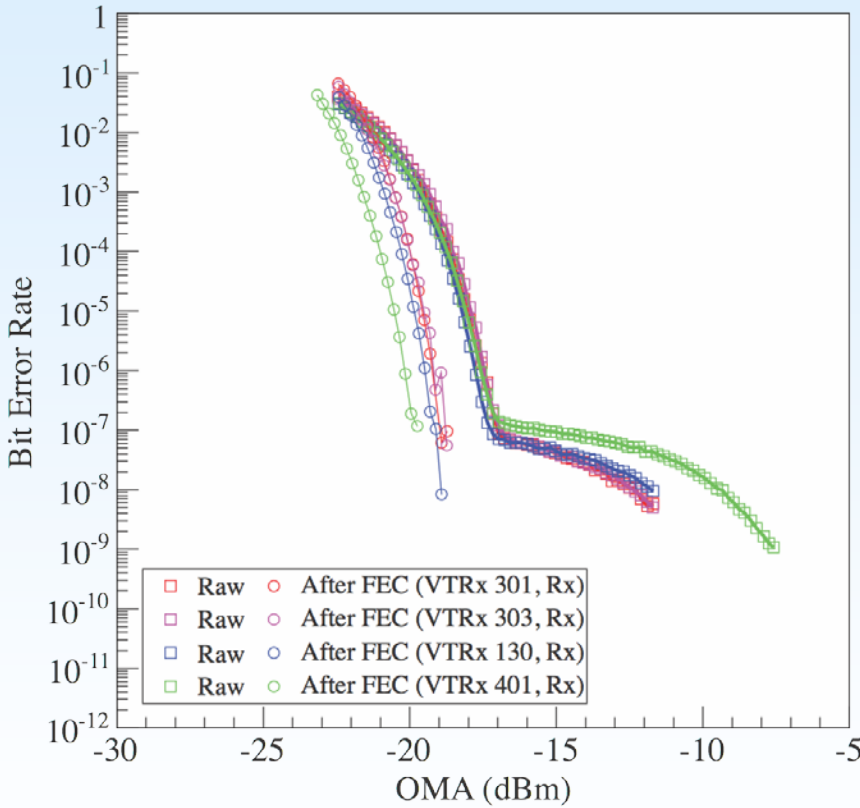
VTRx in n-beam (3: Rx)



Flux:3e10^{10}n/(cm^{2}.s)

VTRx in beam (4: SEU)

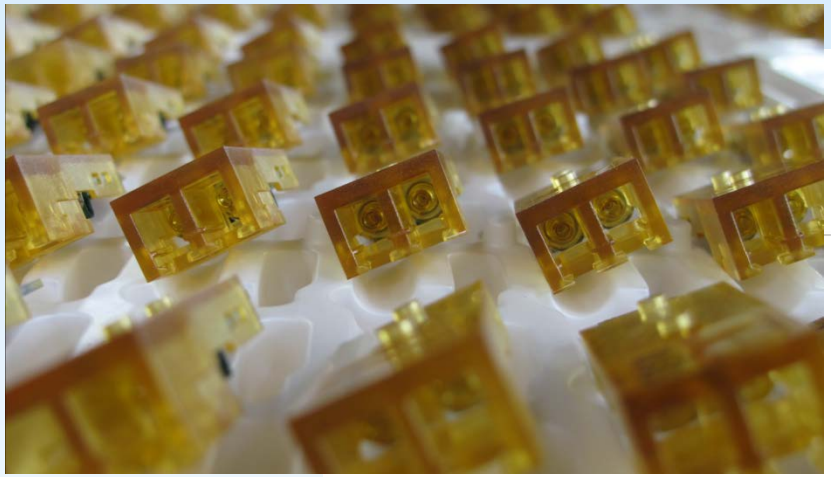
- SEUs in Pin Receiver are unavoidable
  - GBT implements an interleaved Reed-Solomon Forward Error Correction (FEC) scheme to mitigate the induced errors
- Single-event upsets observed in GBLD registers
  - Not seen previously in proton testing at PSI
  - Flux in Louvain neutron test was 3 x 10^{10} n/cm^2/s (two orders of magnitude higher than at PSI)
  - Cross-section is 1.2x10^{-14} errors/n/cm^2
- In a system of 10000 links operating at a luminosity of 10^{35}, this would be equivalent to
  - 1 register corruption every 14 minutes at the level of the Calorimeters
- Most likely due to the circuit topology of a reset line in the control registers
  - To be fixed in final submission

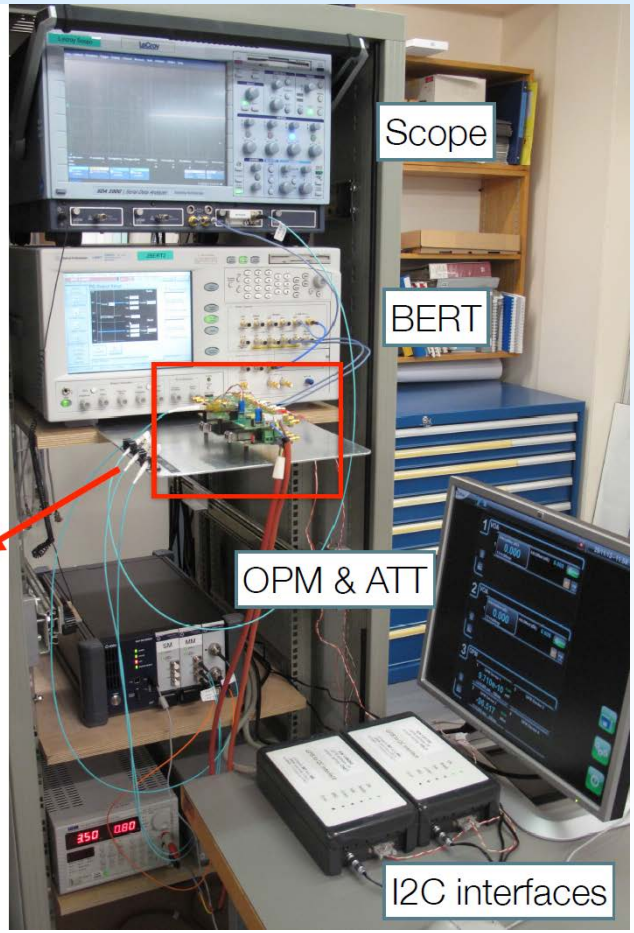


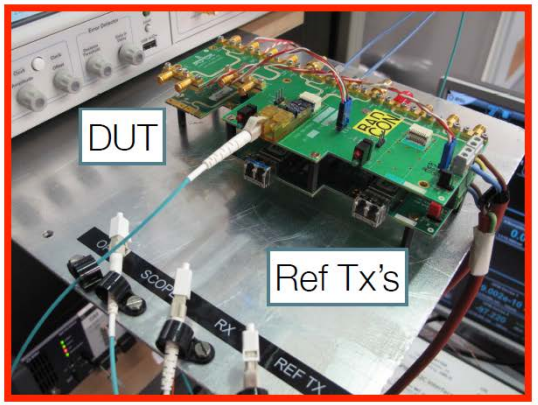
Recap: VTXx Ready for Pre-Production

- PCB and latch designed in-house
- Opto components shortlisted and shown to be radiation tolerant
  - Gamma testing also carried out for verification, no significant effects observed
  - Integration of GBTIA ASIC in ROSA with several suppliers
- Module assembled and performance verified
  - Including performance over operating temperature range 10-60 °C
  - Including magnetic field tolerance
- Final irradiation test of full module allows qualification for use in Calorimeter-level radiation fields
  - SEU sensitivity observed, to be fixed in GBLD production run
- Automated test setup developed, including database and reporting tool
  - To be replicated for module assembler
- QA documentation being prepared

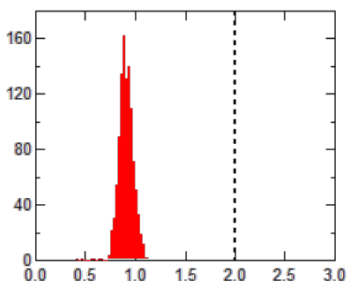
650pcs RadSoft VTTx Batch for CMS GCT

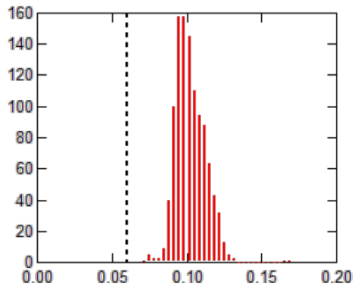






Static parameters of 514 VTTx's (1028 channels):





VTXx Procurement Quantities

Expt	TOSA		ROSA		Latch		VTRx		VTTx
& User	SM	MM	SM	MM	SM	MM	SM	MM	MM
CMS PIXph1	3000								
CMS HCAL	200	4400	200	400	200	2400	200	400	2000
ATLAS SmWh		1850		650		1250		650	600
ATLAS LArg		150		150		150		150	
LHCb		16900		2900		9900		2900	7000
Alice		9950		3550		6750		3550	3200
BE-BI-BL	500		500		500		500		
BE-BI-QP	500		500		500		500		
Totals	4300	33250	1200	7650	1200	20450	1200	7650	12800

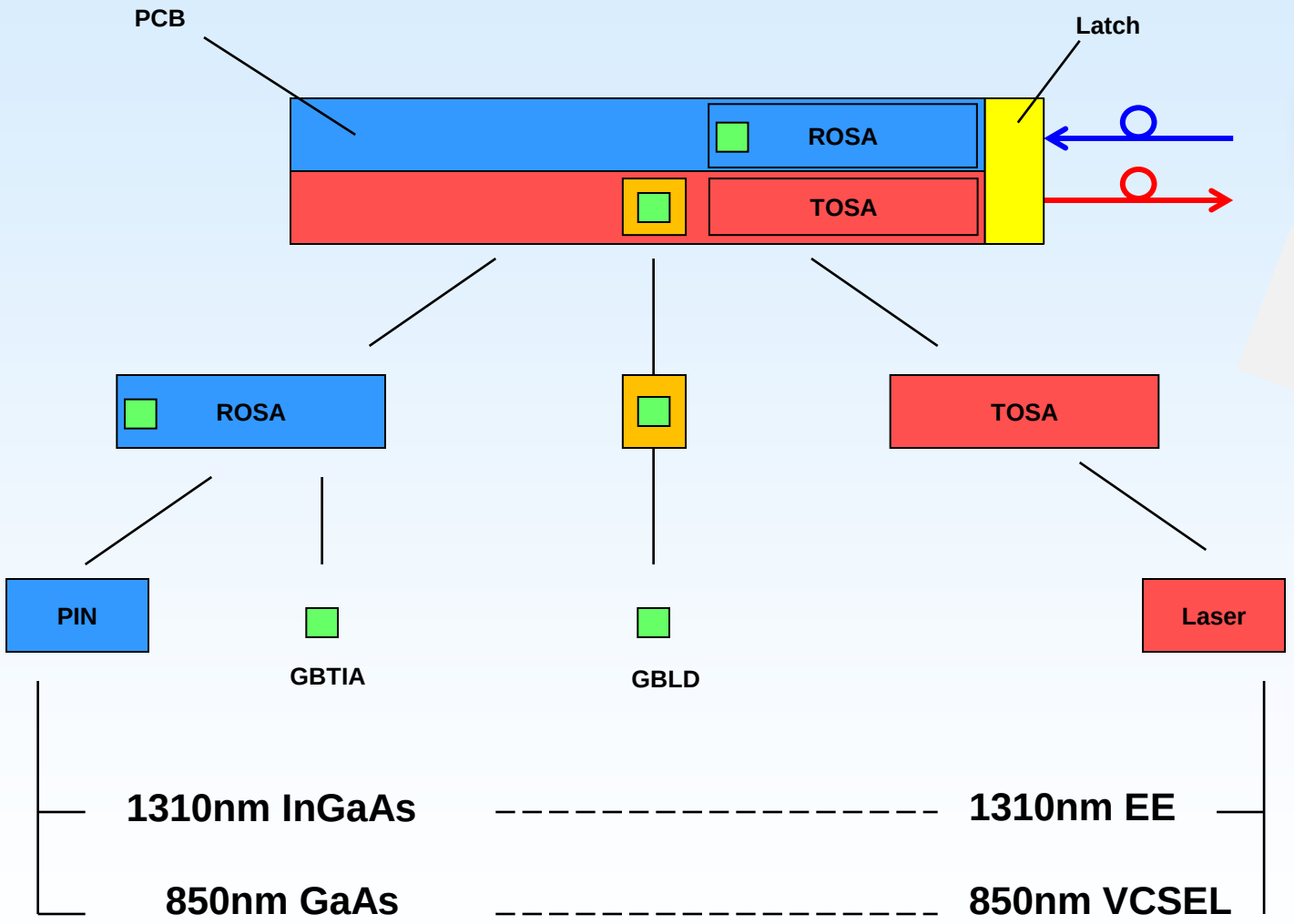
- Procurement process defined and started
  - Need to take funding into account to finalize timing of commercial actions
  - Tendering needs to be completed to know final cost
  - Contract must be placed reasonably soon after tender
  - ASICs are produced as part of the GBT project engineering run
- One year from TOSA contract placement to first delivery of VTXx
- Volume production to kick-off by the end of 2014

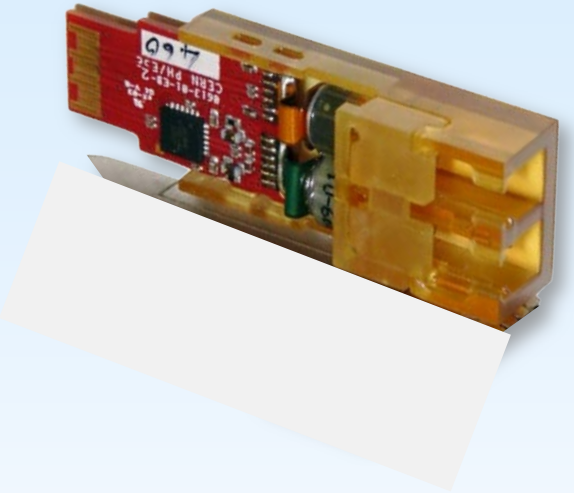
Towards Phase II upgrades: The VL+ project

The Vision:

- 5G downstream, 10G upstream
  - Driven by GBTx evolution path
  - 10G driver ASIC
- Smaller
  - Revisited optical interface
  - MM only
- Denser
  - Multi channel (not necessarily arrays)
- Versatile
  - Common multi-channel package
  - Configurable at assembly time or by turning off unused channels

Reminder 1: The VTRx Assembly Flow

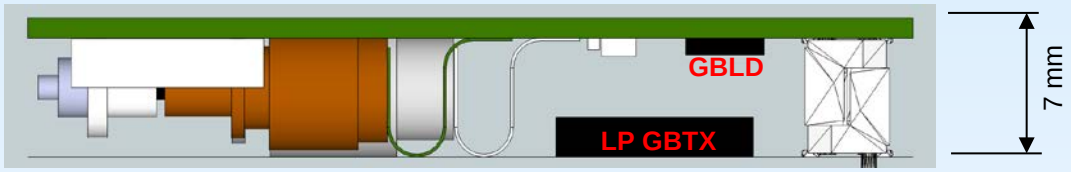


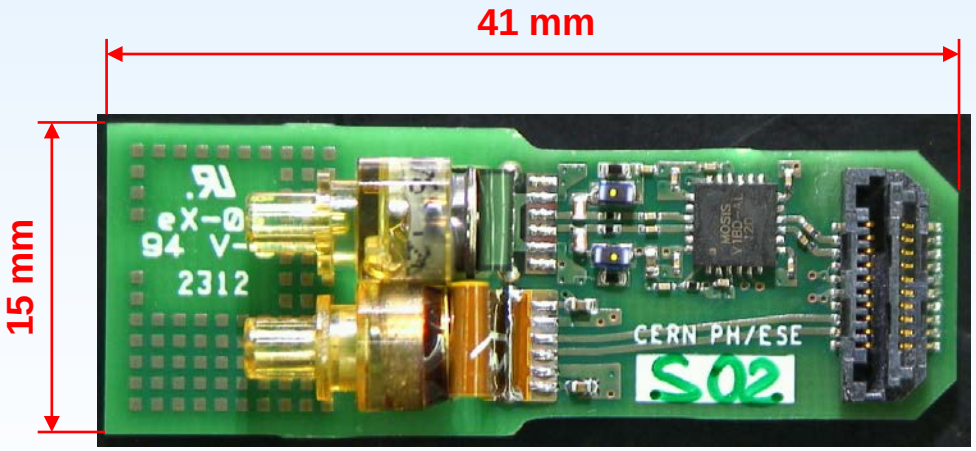


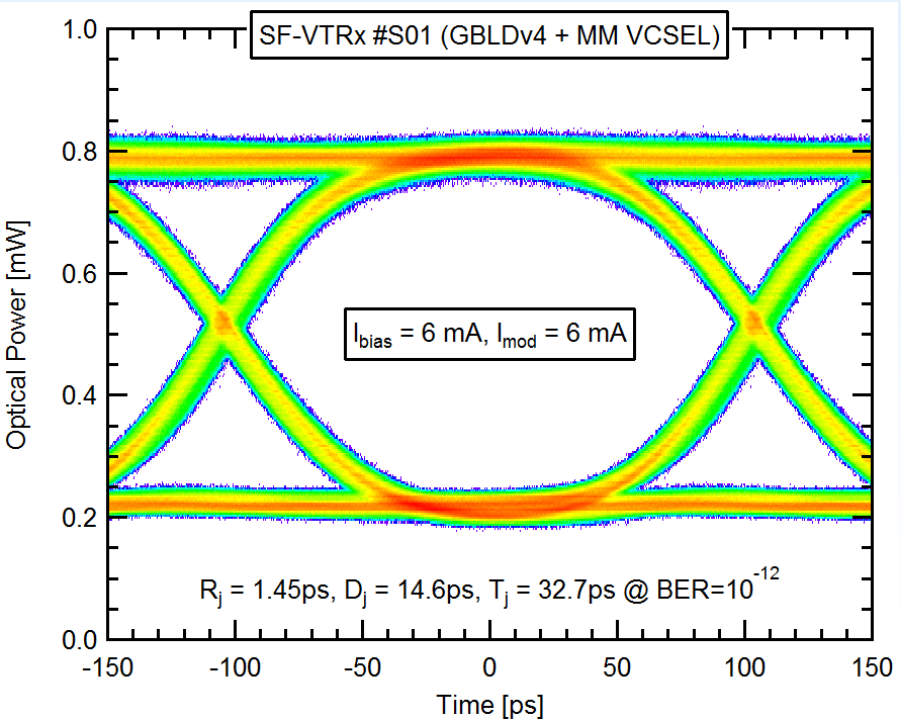
Reminder 2: The SF-VTRx Conceptual Design

Versatile Link

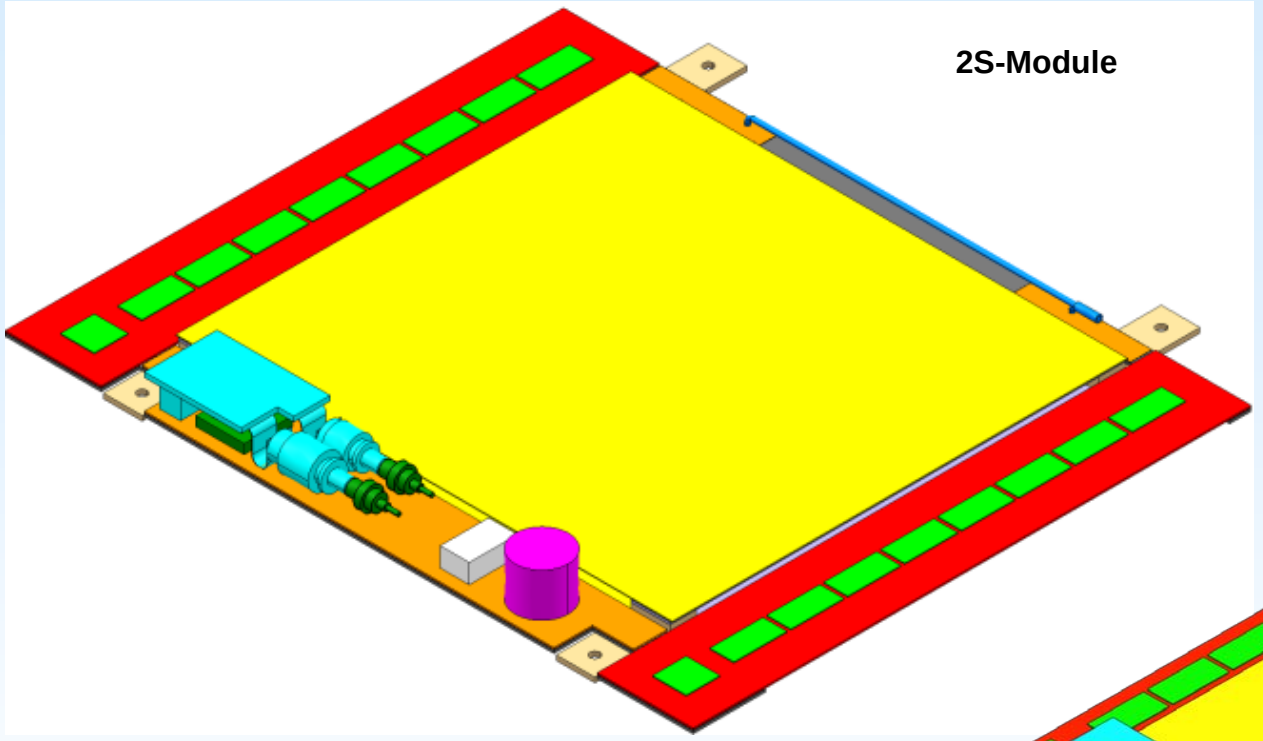
Small Formfactor -VTRx prototype: the densest possible TOSA/ROSA-based assembly

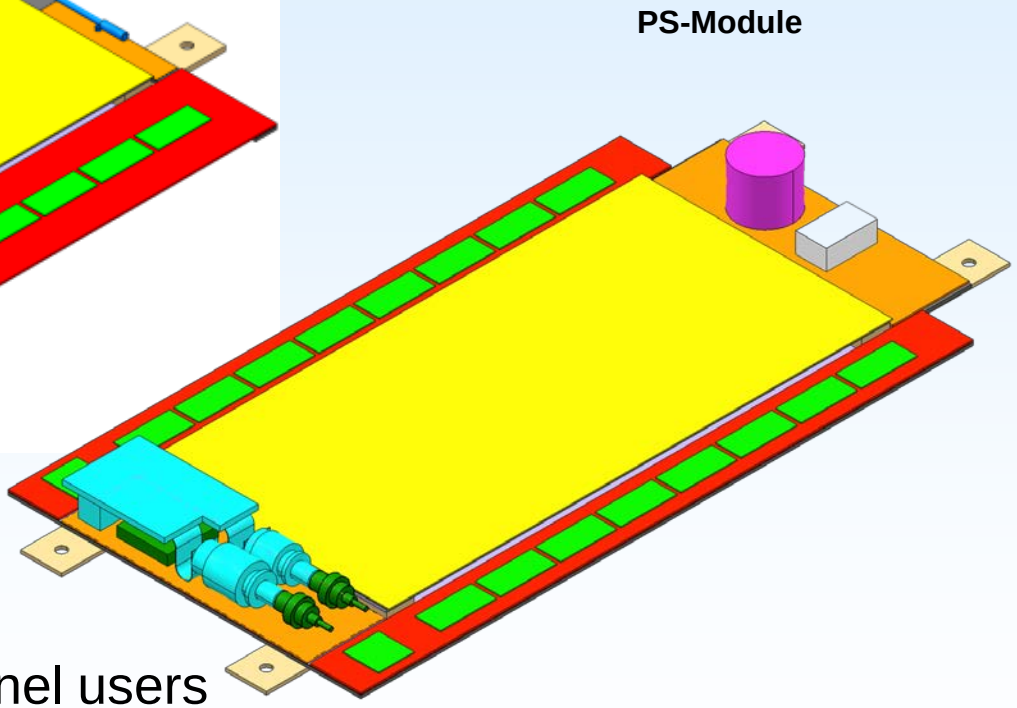






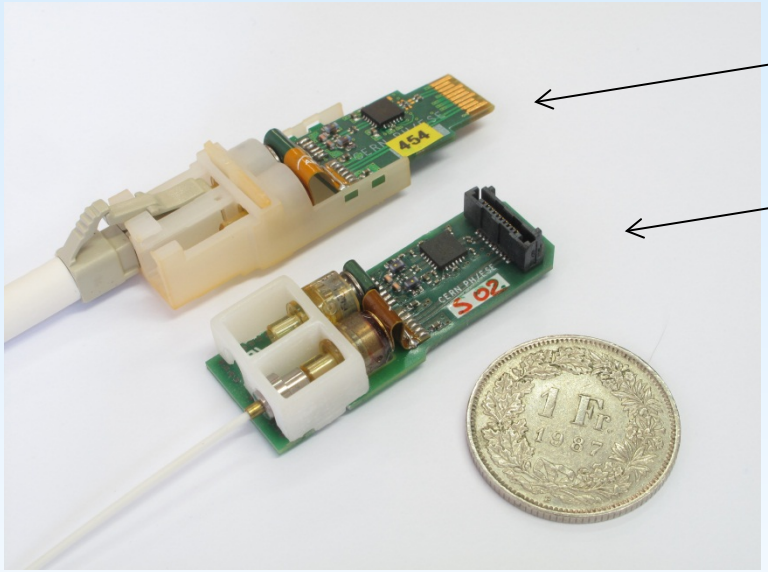
SF-VTRx Integration on CMS Tk Sensor Modules





- SF-VTRx
  - Still too bulky
  - Lacks scalability for multi-channel users

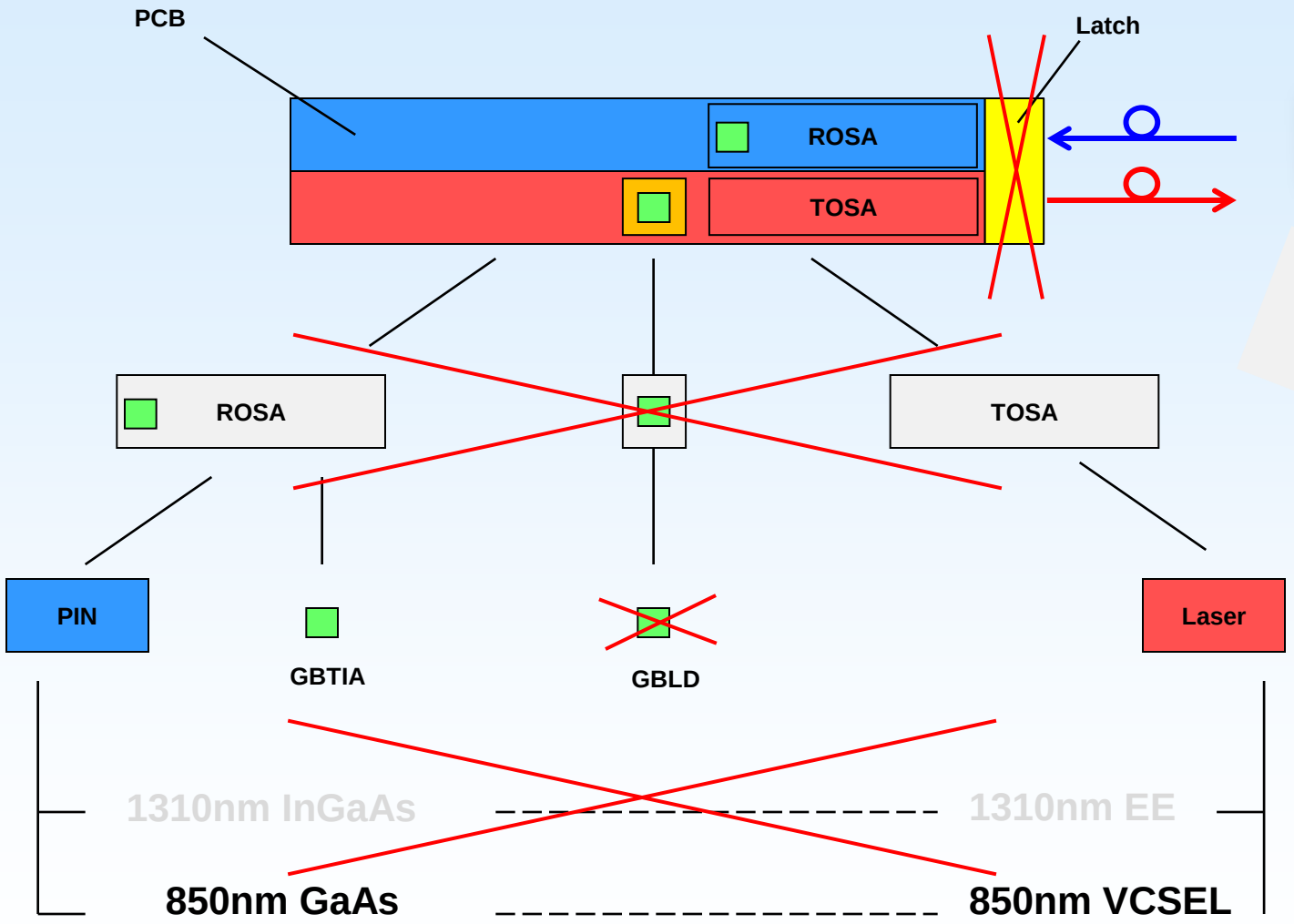
Towards Phase II

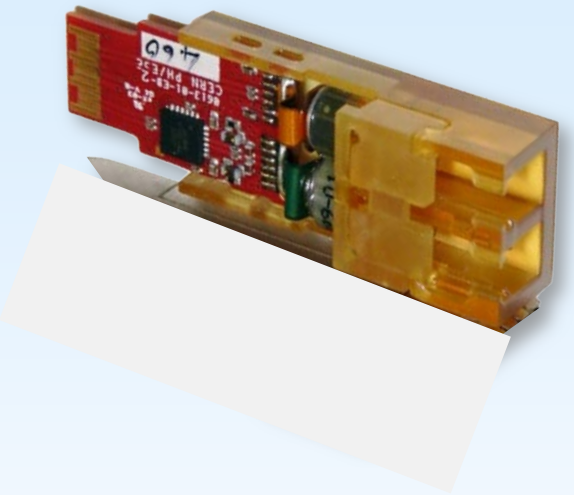


SF-VTRx versus Multi-mode VTRx

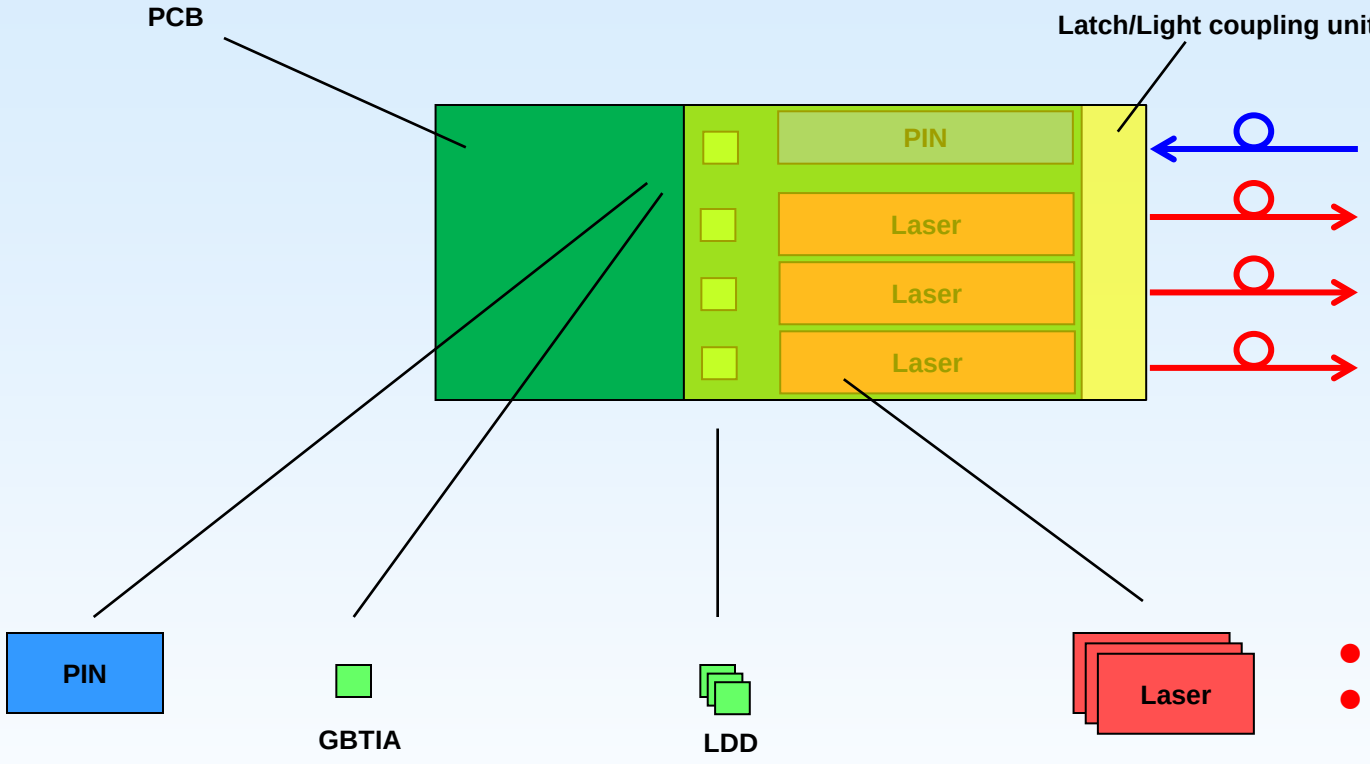
Phase II : VTRx+

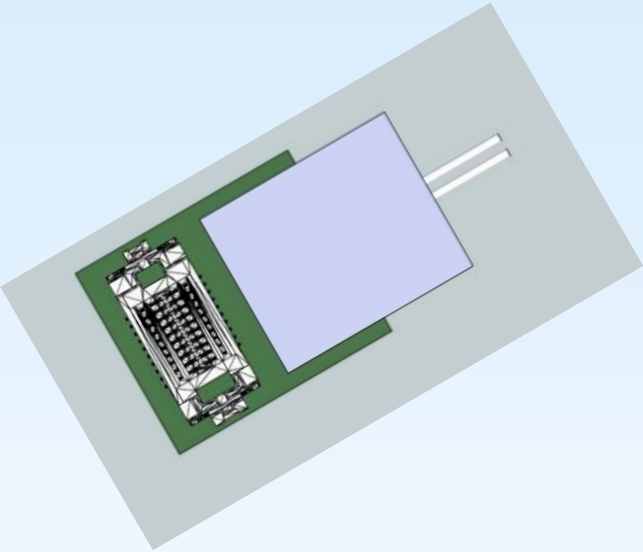
VTRx+ : what needs to be changed





VTRx+ : the concept

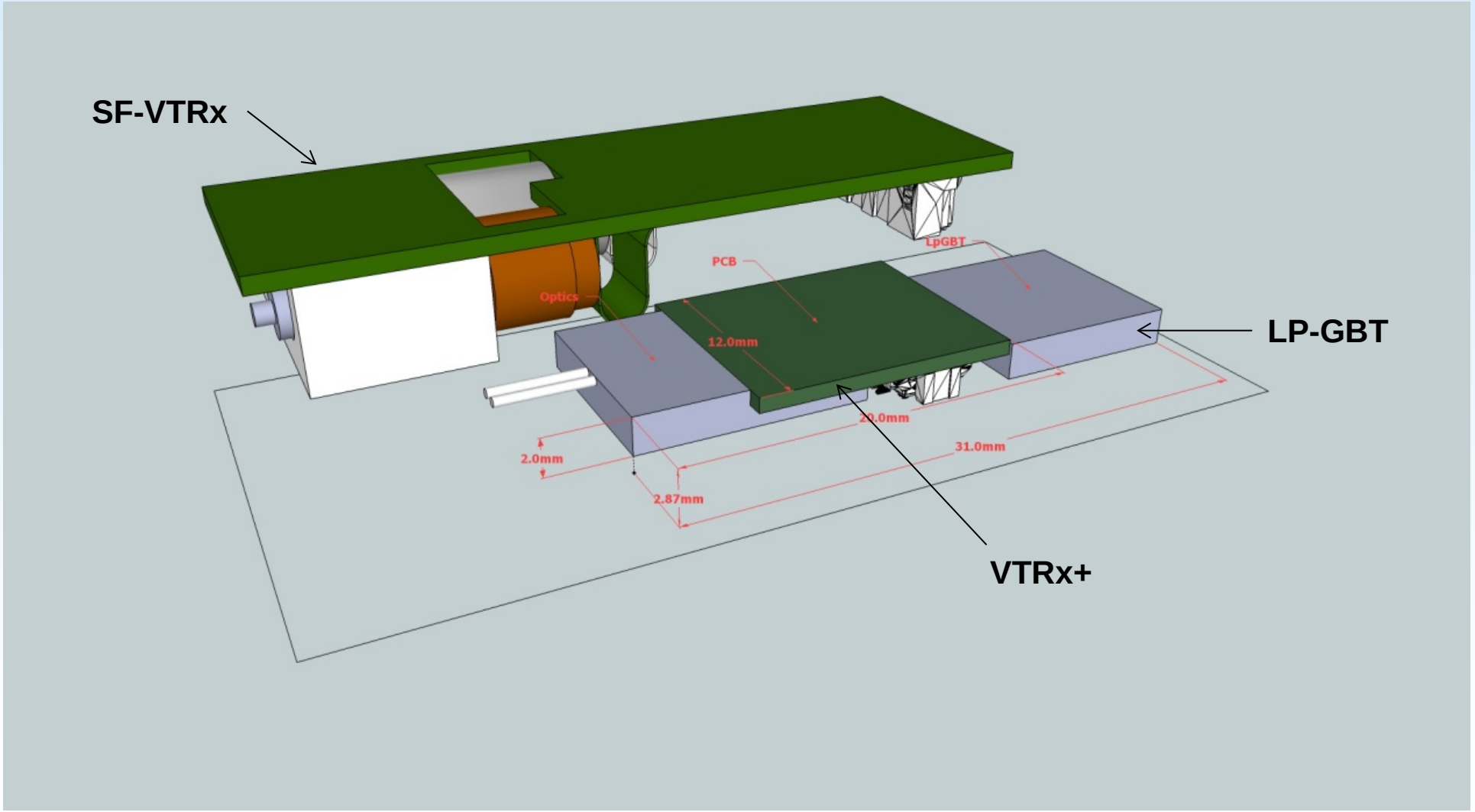




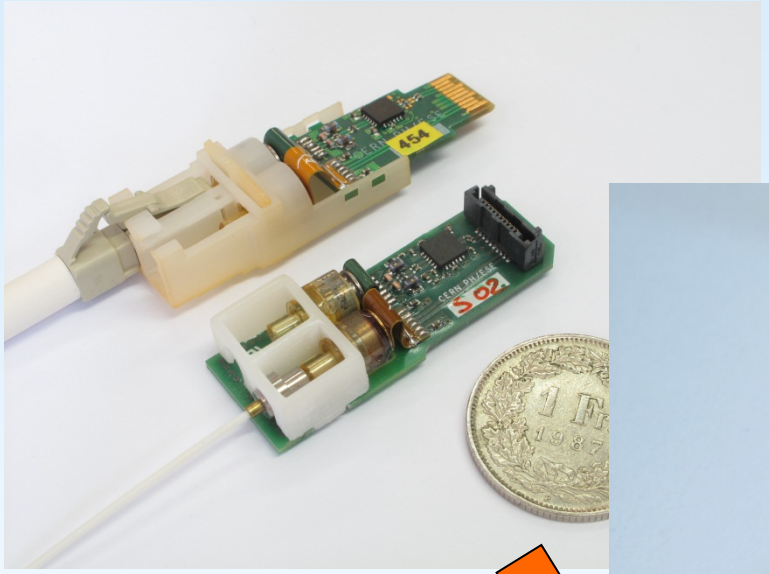
- 5G downstream, 10G upstream
- Smaller
  - Revised optical interface
  - MM only
- Denser
  - Up to 4 channels
- Versatile
  - Common package
  - Configurable at assembly time or by turning off unused channels

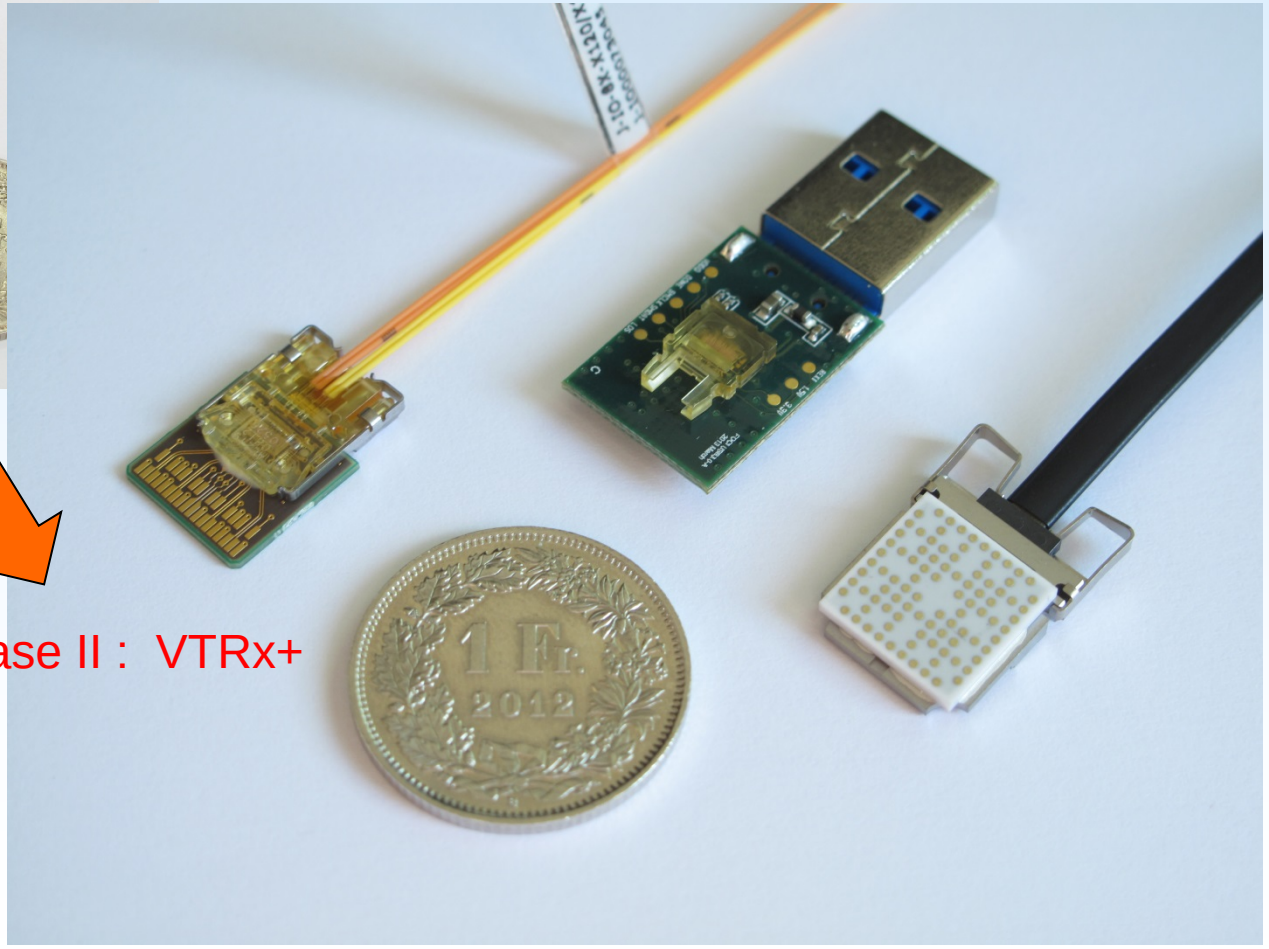
SF-VTRx vs VTRx+: An Artist View

Versatile Link



VTRx+ Samples under Evaluation





Phase II : VTRx+

VL+ project

- We have
  - 10G qualified opto-die (in TOSA/ROSA form)
  - 5G GBTIA (already fitting ROSA cavity dimensions)
  - Qualified fibre and connectors (2012)
  - Recommended Backend (2012)

- We need
  - 10G rad hard Laser Driver
    - Tiny, fitting the package cavity dimensions
    - Single channel, or Quad array, single-ended drive
  - 4 channel package
    - Configurable from single TRx to quad Tx
  - Fresh recommendations for fibre, connectors and backend

VL+ Timeline

- Feasibility Study, 18 months
  - WP1 > 10G LDD
  - WP2 > Access to 10G opto-die (not TOSA/ROSA)
  - WP3 > 4ch opto-package prototypes, possibly integrating LDD, several concepts (single channel-based, array-based, …)
  - WP4 > On-going reliability test on prototypes
  - WP5-6 > On-going evaluation of emerging passive and backend components
  - WP7 > System-level demonstrator(s)

- VL+ kick-off meeting on Friday 21st March, after the mini-opto workshop

VL+ WP-Breakdown (1)

- WP1: 10G LDD (single/quad)
  - Common specification and review-process
  - Design and test
- WP2: Opto-Die (PIN$_{GaAs\&InGaAs}$, VCSEL)
  - Test die from different suppliers
  - Survey market for emerging components
- WP3: 4ch Opto-package (configurable)
  - Design, prototype and test with different suppliers
  - Survey market for emerging packages and opto interfaces
- WP4: Opto-Module reliability
  - Accelerated ageing, 85/85, ESD, stress tests

CERN, SMU

CERN

CERN

Oxford

VL+ WP-Breakdown (2)

- WP5: Passives
  - Survey market for emerging components
  - Test and qualify
    - Fibre: OM3 vs OM4, bend insensitive, 80μm, …
    - Cable: ribbon, micro-tubes, …
    - Connectors: MPOnx12, MXL, …
- WP6: Backend
  - Survey market for emerging engines
  - Test and qualify
- WP7:System
  - Update specifications
  - Develop test framework
  - In-system tests

CERN EN-EL

FNAL

CERN, FNAL Others?, …

VL Documentation

- https://espace.cern.ch/project-versatile-link/public/default.aspx