GBT Project: Present & Future

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On Behalf of the GBT Project Collaboration
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CERN, Switzerland
Outline

• Radiation Hard Optical Link Architecture
• The GBT System
• GBT Chipset:
  – Status
  – Schedule
• GBT-FPGA Status
• GBT Building Blocks Status
• LpGBTX:
  – Architecture
  – SerDes (Resources optimization)
  – Power Consumption
  – Footprint
  – Project effort
Radiation Hard Optical Link Architecture

On-Detector
Radiation Hard Electronics

Off-Detector
Commercial Off-The-Shelf (COTS)

Custom ASICs

Timing & Trigger
DAQ
Slow Control

Timing & Trigger
DAQ
Slow Control

GBTX

GBTIA

GBLD

PD

LD

FPGA
The GBT System

- FE Module
- GBTX
- Phase - Shifter
- CLK Reference/xPLL
- ePLLx
- DEC/SCR
- SCR/ENC
- SER
- CDR
- CLK Manager
- ePLLtx
- CDR
- JTAG
- I2C Slave
- I2C Master
- Control Logic
- Configuration (e-Fuses + reg-Bank)
- JTAG Port
- I2C Port

External clock reference

Clock[7:0]

80, 160 and 320 Mb/s ports

One 80 Mb/s port

data-down

data-up

clock

http://cern.ch/proj-gbt

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GBLD Status

GBLD V4.1

• Main Specs
  – Bit rate 5 Gb/s (min)
  – Modulation:
    • Current sink
    • Single-ended/differential
  – Laser modulation current: 2 to 24 mA
  – Laser bias: 2 to 43 mA
  – Equalization:
    • Pre-emphasis/de-emphasis
    • Independently programmable for rising/falling edges
  – Supply voltage: 2.5 V
  – Die size: 2 mm × 2 mm
  – I2C programming interface

• Status
  – Available in small quantities
    • Integrated in the VTRx and VTTx
  – Fully functional
  – Excellent performance
  – Radiation hardness proved (total dose)
  – Heavy Ion and Neutron SEU tests:
    • Revealed “some sensitivity” of the configuration registers
    • Proton tests shown no upsets
    • Majority of the errors related with reset function (not triplicated) can be easily improved.
  – Technology: 130 nm DM metal stack
  – Device is production ready

4.8 Gb/s, pre-emphasis on

Total jitter: ≈ 25 ps

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GBTIA V2.0 / V2.1

• **Main specs:**
  - Bit rate 5 Gb/s (min)
  - Sensitivity: 20 μA P-P (10^{-12} BER)
  - Total jitter: < 40 ps P-P
  - Input overload: 1.6 mA (max)
  - Dark current: 0 to 1 mA
  - Supply voltage: 2.5 V
  - Power consumption: 250 mW
  - Die size: 0.75 mm × 1.25 mm

• **Status:**
  - Fully functional
  - Integrated in the VTRx
  - Excellent performance
  - Radiation hardness proved
    • Tested up to 200 Mrad (SiO₂)
  - Device is production ready
    • LM metal stack

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GBTX Status

• **Main specs:**
  - 4.8 Gb/s transceiver
  - User bandwidth:
    - 3.28 Gb/s up/down-links, GBT mode
    - 3.52 Gb/s up-link, 8B/10B mode
    - 4.48 Gb/s up-link, wide-bus mode

• **Status:**
  - Chip is fully functional
  - A few modifications will be introduced in the production version:
    - XPLL will be adapted for a higher value of the motional resistance of the quartz crystal
    - Tolerance to SEUs of the e-link programing register will be improved
    - Startup state machine expanded
  - Prototypes availability:
    - 22 + 32 (drilled) GBTX available
    - Additional 240 will be available in August

Total height including solder balls: ~3 mm

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GBT Slow Control Adapter:
• ASIC dedicated to slow control functions.
• System Upgrades for SLHC detectors.
• “Replacement” for the CCU & DCU ASICs
• Flexible enough to match the needs of different Front-End systems.

Key Features:
• Dual redundant e-Ports for GBTX e-links.
• 16 I2C master controllers @ 100k/s or 1 Mb/s.
• 1 SPI master controller
• 1 JTAG master controller
• 32 multiplexed ADC channels:
  – 12-bit dual slope integrating ADC @ 3.5KHz
• 4 DAC channels
• 32 Digital I/O lines individually programmable.
• 8-bit memory bus
• 4 Interrupt inputs
• Technology: CMOS 130nm using radiation tolerant techniques.

Status:
• Chip ready for prototyping:
  – Tapout May 2014

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GBT Chipset Schedule

“Scenario 1” – MPW followed by production

- 19 May 2014 – MOSIS MPW
  - GBTX
  - GBT - SCA
  - GBLD
- Q3 – 2014
  - Chips available from the foundry
  - ASIC Packaging
- Q4 – 2014
  - Prototypes medium quantities: ~200
  - Samples distributed to the users
- Q1 – 2015:
  - Launch the production
- Q3 – 2015:
  - Production quantities available

“Scenario 2” – Production only

- Q2 – 2014 (May)
  - Split Engineering Run to produce in quantities:
    - GBTX
    - GBTIA
    - GBLD V4
    - GBT - SCA
- Q3 – 2014
  - Chips available from the foundry
  - ASIC Packaging
- Q4 – 2014
  - ASIC production testing
  - First production ASICs distributed to the users
GBT – FPGA Status

• **Aim:**
  - Implement the GBT serial link in all its flavours as an IP core for most of the current FPGAs used on Back-End boards for upgrades

• **Firmware versions**
  - Serial link encoding schemes
    - Reed-Solomon (aka “GBT frame”),
    - 8b/10b (to be done)
    - Wide-bus
  - Standard and Fixed latency versions

• **Targeted FPGA and reference design**
  - **Altera:**
    - Cyclone V GT
      - Eval kit & GBTx-SAT board
    - Stratix V
      - AMC 40
  - **Xilinx:**
    - Virtex 6
      - ML605 & GLIB
    - Kintex 7
      - KC705
    - Virtex 7
      - VC705

• **Project Resources**
  - 50% of one Fellow since last summer
  - More than 85 users registered
  - A sharepoint site: [https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx](https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx)

• **A SVN repository:**
  - [https://svnweb.cern.ch/cern/wsvn/phys/ese/be/gbt_fpga](https://svnweb.cern.ch/cern/wsvn/phys/ese/be/gbt_fpga)

• **Contact us:**
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  - Manoel.Barros.Marin@cern.ch

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See poster by Manoel Barros for further information on the GBT – FPGA
Available “IP” to facilitate the implementation of e-Link transceivers in the frontend ASICs:

- **SLVS Receiver**
  - Wire-bond, DM metal stack
  - C4, LM metal stack
- **SLVS Driver**
  - Wire-bond, DM metal stack
  - C4, LM metal stack
- **SLVS Bi-directional**
  - C4, LM metal stack
- **HDLC transceiver**
  - Synthesizable Verilog
- **7B/8B CODEC**
  - Synthesizable Verilog
- **ePLL-FM**
  - Frequency Multiplier PLL
  - Radiation Hard
  - 130 nm CMOS technology with the DM metal stack (3-2-3).
  - Input frequencies: 40/80/160 MHz
  - Output frequencies: 160/320 MHz regardless the input frequency
  - Programmable phase of the output clocks with a resolution of 11.25° for the 160 MHz clock and 22.5° for the 320 MHz clock
  - Programmable charge pump current, loop filter resistance and capacitance to optimize the loop dynamics
  - Supply voltage: 1.2 V - 1.5 V
  - Nominal power consumption: 20 mW @ 1.2 V - 30 mW @1.5 V
  - Operating temperature range: -30°C to 100°C
- **ePLL-CDR (currently under testing)**
  - Data rate: 40/80/160/320 Mbit/s
  - Output clocks: data clock + 40/80/160/320 MHz with programmable phase
  - Internal or external calibration of the VCO frequency
  - Possibility to use it as a frequency multiplier PLL without applying input data
  - Programmable charge pump current, loop filter resistance and capacitance to optimize the loop dynamics
  - Supply voltage: 1.2 V - 1.5 V
  - Operating temperature range: -30°C to 100°C
  - Prototype fabrication: May 2013
The LpGBTX

- **Low Power Dissipation and Small Footprint:**
  - Critical for pixel detectors
  - Critical for tracker/triggering detectors

- **Bandwidth:**
  - Low-Power mode
    - 4.8 Gb/s for Up and Down links
  - High-Speed mode:
    - 9.8 Gb/s for the Up-link
    - 4.8 Gb/s for the Down-link

- **e-Links:**
  - 80, 160 and 320 Mb/s for down-links
  - Low-Power Mode:
    - 80, 160 and 320 Mb/s for up-links
  - High-Speed Mode:
    - 160, 320 and 640 Mb/s for up-links
  - Programmable: Single-ended / differential

- **Functionality:**
  - “Replica” of the GBTX
  - Small subset of the GBT-SAC functionality will be included
LpGBTX Architecture

- **Downlink**: 4.8 Gb/s
  - GBT mode
- **Uplink**: 4.8/9.6 Gb/s
  - GBT / Wide-Bus / 8B/10B
- **EC link**: 80 Mb/s
- **SCA functionality added**
- **Output e-Links**:
  - 80/160/320 Mb/s → 40 e-Links (max)
- **Phase programmable clocks**:
  - 40/80/160/320/640 MHz → 8 Clocks (max)
- **Output e-Clocks**:
  - 40/80/160/320 Mb/s → 40 e-Clocks (max)
- **Input-Links**:
  - 80/160/320 Mb/s @ 4.8 Gb/s
  - 160/320/640 Mb/s @ 9.6 Gb/s
  - GBT mode → 40 e-Links (max)
  - Wide-bus mode → 56 e-Links (max)

“Idle & data headers” could be used to distinguish between the “odd and even frames” when operating at 9.6 Gb/s!
SerDes Optimization

For efficiency the SER and DES have to be co-designed

- 1 high frequency PLL drives the CDR and SER:
  - Half Rate CDR (same architecture as GBTX)
  - Serializer:
    - Full rate @ 4.8 Gb/s
    - Half rate @ 9.6 Gb/s
- PLL can work as:
  - CDR
  - Frequency Multiplier
  - This enables: TX, RX and TRANS

Clock Divider
- For the e-Links the clock frequencies are:
  - 40/80/160/320/640 MHz
- Half rate CDR requires:
  - 2.4 GHz
  - I and Q phases
  - Differential for CML
- Serializer: Half rate 9.8 Gbps / Full rate 4.8 Gbps
  - 4.8 GHz

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## LpGBTX: Power (1/2)

### LpGBTX power estimate

<table>
<thead>
<tr>
<th>Component</th>
<th>Power [mW]</th>
<th>Fraction</th>
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<tbody>
<tr>
<td>I/O</td>
<td>548</td>
<td>54%</td>
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<tr>
<td>SERDES</td>
<td>157</td>
<td>15%</td>
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<tr>
<td>CORE</td>
<td>121</td>
<td>12%</td>
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<tr>
<td>Phase-Shifter</td>
<td>120</td>
<td>12%</td>
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<tr>
<td>Clock Manager</td>
<td>73</td>
<td>7%</td>
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<tr>
<td><strong>Total (max)</strong></td>
<td><strong>1019</strong></td>
<td></td>
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</table>

- **Assumes:**
  - 65 nm CMOS technology
  - Supply voltage: 1.2V
  - Merged SerDes architecture
  - 4.8 Gb/s on both up and down links
  - e-Links with 200 mV signaling
  - “SCA” functionality not taken into account in this preliminary study

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Preliminary & Non-Binding!
Case study:

- **Hypothetical** configuration:
  - **E-Links:**
    - 20 × Data-In @ 160 Mb/s
    - 1 × Clock @ 160 MHz
    - 2 × Data-Out @ 160 Mb/s
  - **Phase-Adjustable clocks:**
    - 2 × Clock @ 40 MHz
    - 2 × Clock @ 160 MHz

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<th>Mode:</th>
<th>TRANSCEIVER</th>
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<td>E-Links:</td>
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<td>Data rate [Mb/s]:</td>
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<td># Data outputs:</td>
<td>2</td>
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<tr>
<td># Clock outputs:</td>
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<td># Data inputs:</td>
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<td>EC-Channel:</td>
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<tr>
<td>State:</td>
<td>Disabled</td>
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<tr>
<td>Phase-Shifter:</td>
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<tr>
<td>State:</td>
<td>Enabled</td>
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<td># Channels</td>
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<td>Power [mW]</td>
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<td>SERDES:</td>
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<td>XPLL:</td>
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<td>Channel:</td>
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<td>SLVS-TX:</td>
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<td>Total:</td>
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<td>CLK SLVS-Tx:</td>
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<td>Data SLVS-Rx:</td>
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<td>Total:</td>
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<td>CORE:</td>
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<td>Standard Cells:</td>
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<td>Phase-Aligners:</td>
<td>6</td>
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<tr>
<td>Total:</td>
<td>115</td>
</tr>
<tr>
<td>Total Power [mW]:</td>
<td>439</td>
</tr>
</tbody>
</table>
LpGBTX: Footprint

Tracker Specific Development (Single-ended I/O only)

General Purpose LpGBTX with programmable I/O (Single-ended /Differential)

Two ASICs:
• LpGBT-SerDes (tracker specific)!
• LpGBTX (general purpose)
Although many functions are the same in the two ASICs, these are effectively two projects!
• Almost doubles the budget and the manpower needs!

Preliminary & Non-Binding!

• Pin-count: ≈ 150 (to be confirmed)
• BGA pitch: 0.65 mm
• Package Size: ≈ 10 mm × 10 mm

• Pin-count: = 500
• BGA pitch: 0.65 mm
• Package Size: ≈ 16 mm × 16 mm
LpGBTX: 2014 – and beyond, Activities / Manpower / Budget

2014
• Q3: First draft of LpGBTX specifications
• Q3: Discussions with the Experiments
• Q4: LpGBTX final specifications

2015 and beyond
• LpGBTIA
  – (The GBTIA is already relatively low power. Perhaps the LpGBTIA is not a strictly necessary development...)
  – Technology: 65 nm CMOS
  – Manpower: 2 MY (design and testing)
• LpGBLD10
  – (Some work already going on)
  – Technology: 130 nm CMOS
  – Manpower: 2 MY (design, packaging and testing)
• LpGBTX
  – Technology: 65 nm CMOS
  – Two packaging flavours:
    • “Tracker” & “General Purpose”
  – Manpower:
    • Design: 8 MY
    • Packaging: 1 MY
    • Testing: 2 MY
  – We have to seriously consider “building” a stable LpGBT team if a LpGBT chipset is to be a reality in useful time!
  – The move to 65 nm and Low Power is not just a “copy-paste exercise”!!!
• The LpGBT has not yet been defined as an approved “project” or “common project”:
  – Effort going on to secure budget and manpower for the project!

Total manpower: 15 MY
Extra Slides
EportRx: phase-aligner (set to maximum and minimum; FE position dependant)
EportTx: no phase align necessary on GBTx

Flags are latched with e-link's clock and triggered by the e-links data
E-LINK SERDES

GBT-FPGA

GLIB

CLOCK

29 ns

21 ns

GBT-FPGA

TX

MGT TX

SFP

GBTx SAT board

Cyclone V

PLL

4 ns

29 ns

30.6 ns

51.2 ns

18/03/2014

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## UPSTREAM LATENCY

<table>
<thead>
<tr>
<th>Encoding</th>
<th>E-link speed</th>
<th>All</th>
<th>All - passive</th>
<th>All - passive - GBT_FPGA*</th>
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<tbody>
<tr>
<td>GBT Frame</td>
<td>80MHz</td>
<td>224 ns</td>
<td>214 ns</td>
<td>~9 BC</td>
</tr>
<tr>
<td></td>
<td>237 ns</td>
<td>227 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>160MHz</td>
<td>190 ns</td>
<td>180 ns</td>
<td>~8 BC</td>
</tr>
<tr>
<td></td>
<td>202 ns</td>
<td>192 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wide Bus Frame</td>
<td>80MHz</td>
<td>224 ns</td>
<td>214 ns</td>
<td>~9 BC</td>
</tr>
<tr>
<td></td>
<td>237 ns</td>
<td>227 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>160MHz</td>
<td>190 ns</td>
<td>180 ns</td>
<td>~8 BC</td>
</tr>
<tr>
<td></td>
<td>202 ns</td>
<td>192 ns</td>
<td></td>
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</tr>
</tbody>
</table>

Remaining: MGT, SFPs, GBTx
### Downstream Latency

<table>
<thead>
<tr>
<th>Encoding</th>
<th>E-link speed</th>
<th>All</th>
<th>All - passive</th>
<th>All – passive - GBT_FPGA*</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBT Frame</td>
<td>80MHz</td>
<td>174 ns</td>
<td>164 ns</td>
<td>~7 BC</td>
</tr>
<tr>
<td></td>
<td>160MHz</td>
<td>173 ns</td>
<td>163 ns</td>
<td>~7 BC</td>
</tr>
</tbody>
</table>

Remaining: MGT, SFPs, GBTx