Front-End ASIC for the ATLAS New Small Wheels

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ASIC for ATLAS Muon Spectrometer Upgrade

New Small Wheels
- sTGC
  Small Strip Thin Gap Chamber
- MM
  MicroMegas
  (MICROMEsh GAseous Structure)

Front-end Electronics (ASIC)
- more than 2.3 million channels total
- operate with both charge polarities
- sensing element capacitance 10-200 pF
- charge meas. up to 2 pC @ < 1 fC rms
- time meas. ~ 100 ns @ < 1 ns rms
- trigger primitives, neighbor logic
- low power, programmable
VMM Front-end ASIC

VMM is a 64-channel front-end ASIC for the read out the sTGC and MM sensors in the New Small Wheels

**version 1**

VMM1, year 2012
size 5.9 × 8.4 mm²
500k transistors (8k/ch.)
a complex mixed-signal ASIC
- extensively tested -

**version 2**

VMM2, year 2014
size 13.5 × 8.4 mm²
> 5M transistors (> 80k/ch.)
a considerable step-up in complexity
- being fabricated -
VMM2 Architecture - Analog Front-End

- **input transistor**: PMOS 180 nm x 20 mm, 2 mA
- **input capacitance**: optimized for 200 pF, can operate from sub-pF to nF
- **polarity**: adjustable positive or negative
- **gain**: adjustable 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (max charge 2 to 0.06 pC)
- **peaking time**: adjustable 25, 50, 100, 200 ns
- **leakage-adaptive**, DDF shaper, BGR-stabilized baseline, test capacitor, mask
• adjustable **discrimination** threshold per channel
• trimming range: 15 mV in 1m increments
• comparator hysteresis: ~ 20 mV
• **sub-hysteresis** discrimination: effective discrimination ~ 2 mV
• **neighbor** logic: processing of sub-threshold neighbor channels
• **inter-chip communication**: neighbor channel logic includes neighbor chips
VMM2 Architecture - Direct Timing Measurements

- **direct digital output** per channel: LVDS 600 mV +/- 150 mV
- **selectable measurements:**
  - time-over-threshold (ToT)
  - threshold-to-peak (TtP)
  - peak-to-threshold (PtP)
  - pulse at peak (PtP)
- **continuous self-reset operation**
VMM2 Architecture - Peak and Time Detectors

- **peak detection**: measurement of peak amplitude and storage in analog memory
- **time detection**: measurement of peak time and storage in analog memory
  - sub-mV resolution on amplitude measurement
  - sub-ns resolution, low time-walk on peak time measurement
- multi-phase offset-free measurement circuits
- adjustable time-to-amplitude converter (TAC): 125, 250, 500, 1000 ns
- optional current output for current-mode ADCs
• charge resolution $\text{ENC} < 5,000 \text{ e}^{-}$ at 25 ns, 200 pF

• analog dynamic range $Q_{\text{max}} / \text{ENC} > 12,000 \rightarrow \text{DDF}$

• timing resolution $< 1 \text{ ns}$ (at peak-detect)

\[ \sigma_t \approx \frac{\text{ENC} \tau_p}{Q} \frac{\lambda_p}{\rho_p} \approx 0.3-0.8 \]

G. De Geronimo, in “Medical Imaging” by Iniewski
VMM2 Architecture - 6-bit ADC

- **lower-resolution ADC:** 6-bit, sub-mW, adjustable conversion time and offset
  - clock-less single-stage current-mode domino architecture
  - at threshold-crossing, completes in 25 ns from peak time

- at direct output: flag at peak followed by serialized address
- clock frequency: up to 200 MHz
- selectable serialized mode: either at each clock cycle or at each clock edge
- continuous self-reset operation
Direct Output with 6-bit ADC

- conversion completes within ~25 ns from peak
- dead time from charge event < 100 ns
- 6-bit amplitude $D5-D0$ shifted at each clock cycle or edge
- up to 200 MHz readout
VMM2 Architecture - 10-bit and 8-bit ADCs

- mixed-signal channel (x 64)
- 80,000 MOSFETs
- ~ 4-8mW

- higher-resolution ADCs: 10-bit, 200 ns, sub-mW, for peak amplitude conversion
- 8-bit, 100 ns, sub-mW for timing conversion
- adjustable conversion time and offset
- clock-less dual-stage current-mode domino architecture

- continuous self-reset operation
VMM2 Architecture - Timestamp and FIFO

- **12-bit timestamp**: from *shared 12-bit Gray-code counter*, external BC clock
  - stops TAC and latches coarse timing
- **complete timing information**: 20-bit, ~100 μs with sub-ns resolution
- **4-deep FIFO**: threshold-crossing indicator, 10-bit ADC, 8-bit ADC, 12-bit BC
- address memory
64 channels

- Gray count
- Shaper
- Logic
- Peak
- Time
- Addr.
- Trim

6-b ADC
10-b ADC
8-b ADC
12-b BC

4X FIFO

TGC clock

TGC out (ToT, TtP, PtT, PtP, 6bADC)

BC clock

vmm2 architecture

- Complete Channel

- 64 independent channels
- Neighbor communication
- 4-8 mW / channel depending on configuration

Layout size: 12 mm x 100 µm = 1 mm²
80,000 MOSFETs
sparse readout of amplitude/timing with token passing

readout options:
  • mixed-signal 2-phase: peak and time at analog outputs analog1,2
    address serialized at digital output data1
  • fully digital continuous: 38-bit event data at digital outputs data1,2
    data1 also serves as empty flag
    data shift at each clock cycle or at each clock edge up to 200 MHz
• **address of first event (ART):** - available at dedicated output ART
  - first event flag followed by serialized event address
  - shifted at each clock cycle or at each clock edge
  - up to 200 MHz, self-reset
ART (Address in Real Time)

- Charge event
- Analog pulse
- Peak-found
- Reset
- Flag and address serialized
- 6-bit address $D5-D0$ shifted at each clock cycle or edge
- Up to 200 MHz readout
VMM2 Architecture - Additional Functions

- Coarse time counter: 12-bit Gray-code
- Test pulser generator: 10-bit adjustable
- Coarse threshold generator: 10-bit adjustable
- Analog monitor: analog signal, trimmed threshold, DACs, temperature
- Temperature sensor: ~ 725 mV - 1.85 mV/°C
- Configuration registers: 80-bit + 24-bit / channel
- PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit
VMM2 Architecture - Complete ASIC

- coarse time counter: 12-bit Gray-code
- test pulse generator: 10-bit adjustable
- coarse threshold generator: 10-bit adjustable
- temperature sensor: ~725 mV - 1.85 mV/°C
- configuration registers: 80-bit + 24-bit / channel
- PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit

- technology: IBM CMOS 130nm
- power dissipation: 4-8+ mV/ch.
- transistor count: > 5 million
analog, mixed-signal, digital supplies (1.2V) – neigh.t – digital IOs (14) - TGC outs 0-6

392 bonding pads

all by hand (no automation)
A Few Notes

• VMM2 is an extremely complex and ambitious ASIC
  - *a planned redesign of VMM1 to bring us closer to the final VMM* -

• Main **risks** from **design complexity** and **layout parasitics**
  • resolution may be affected by mixed-signal cross-talk
  • locking conditions may occur from complex control logic
  • 200 MHz operation may be affected by parasitics
  • performance (INL, DNL, ..) of novel ADCs to be verified

  - *extensive simulations done to mitigate these risks* -

• To be included in **VMM3**
  • simultaneous direct- and multiplexed-operation
  • DSP for Level 1 handling and additional shared FIFO
  • test patterns and clock output
  • SEU mitigation circuits
  • any fixes on VMM2
Packaging

custom BGA package

21 x 21 mm², 400-pin, 1 mm pitch
## Schedule

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<td>ASIC design</td>
<td>complete</td>
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<tr>
<td>ASIC layout</td>
<td>complete</td>
</tr>
<tr>
<td>ASIC fabrication</td>
<td>in progress, expected by May 2014</td>
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<tr>
<td>BGA package</td>
<td>in progress, expected by May 2014</td>
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<tr>
<td>PCB (AZ)</td>
<td>in progress, expected by May 2014</td>
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