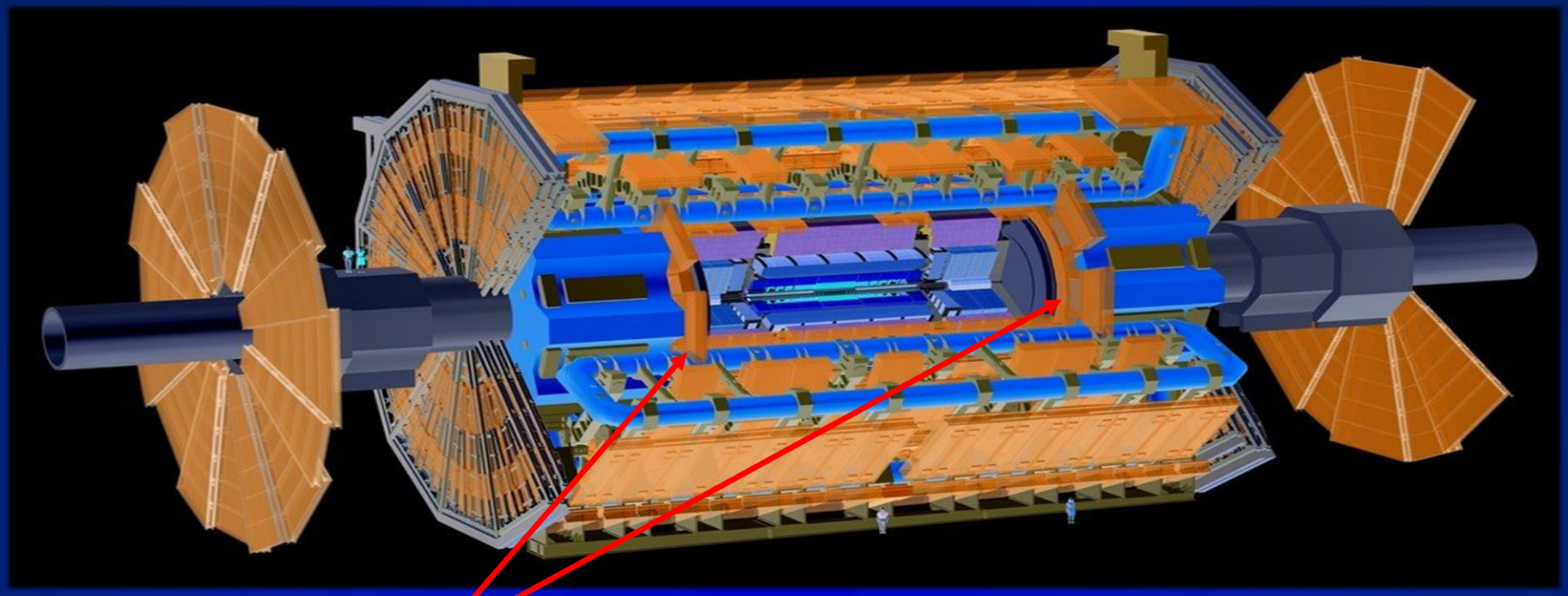
Front-End ASIC for the ATLAS New Small Wheels

Gianluigi De Geronimo, Alessio D'Andragora, Jack Fried,
Neena Nambiar, Emerson Vernon, and Venetios Polychronakos

Brookhaven National Laboratory

ACES 2014 - CERN March 2014

ASIC for ATLAS Muon Spectrometer Upgrade



New Small Wheels

- sTGC
  Small Strip Thin Gap Chamber
- MM
  MicroMegas
  (MICROMEsh GAseous Structure)

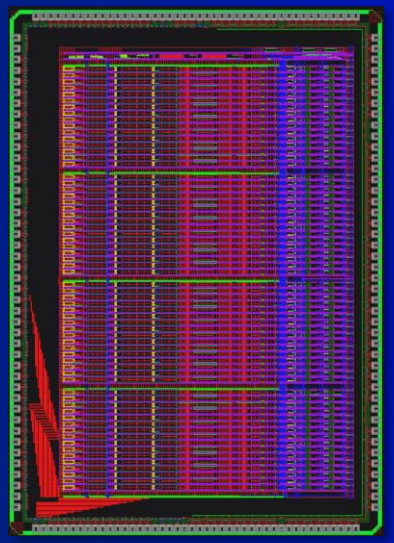
Front-end Electronics (ASIC)

- more than 2.3 million channels total
- operate with both charge polarities
- sensing element capacitance 10-200 pF
- charge meas. up to 2 pC @ < 1 fC rms
- time meas. ~ 100 ns @ < 1 ns rms
- trigger primitives, neighbor logic
- low power, programmable

VMM Front-end ASIC

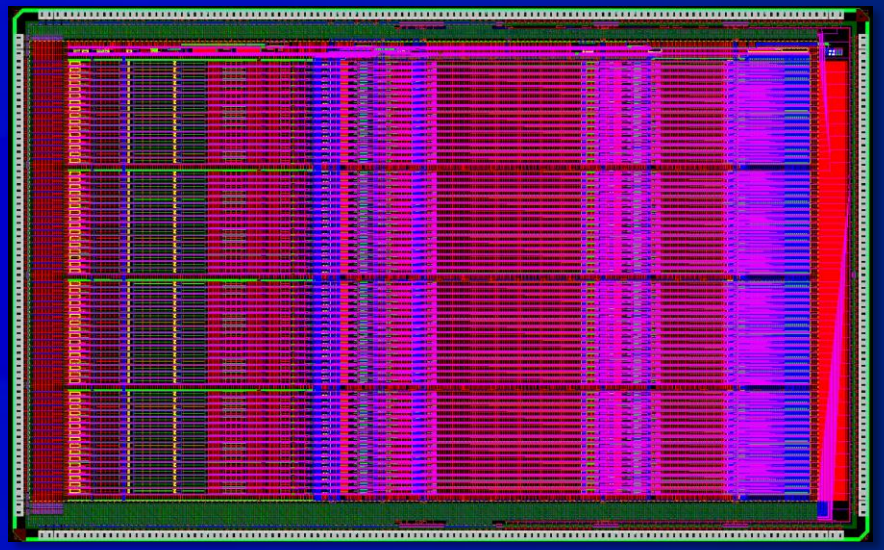
VMM is a 64-channel front-end ASIC for the read out the sTGC and MM sensors in the New Small Wheels

version 1



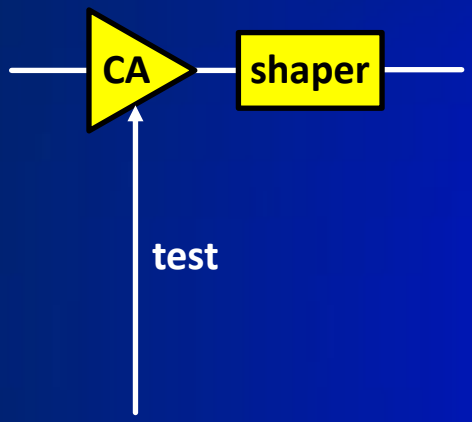
VMM1, year 2012
size 5.9 × 8.4 mm²
500k transistors (8k/ch.)
a complex mixed-signal ASIC
- extensively tested -

version 2



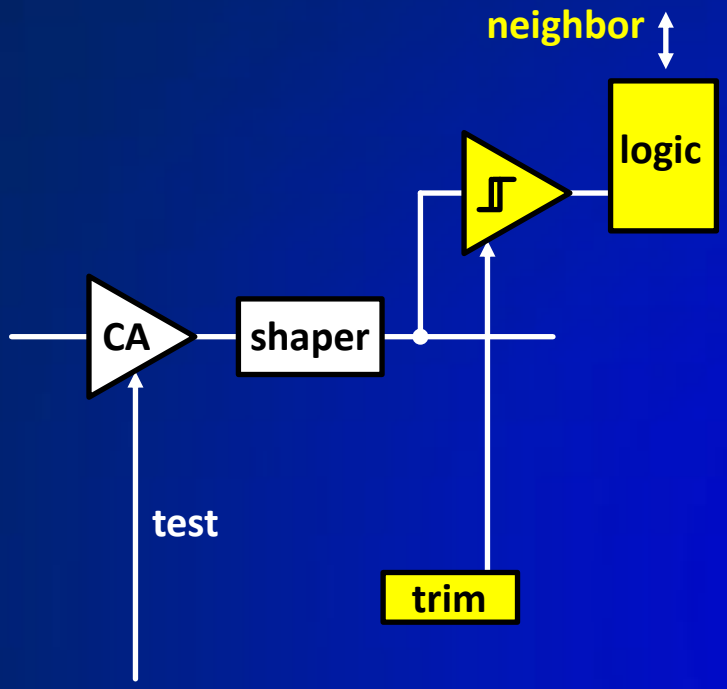
VMM2, year 2014
size 13.5 × 8.4 mm²
> 5M transistors (> 80k/ch.)
a considerable step-up in complexity
- being fabricated -

VMM2 Architecture - Analog Front-End



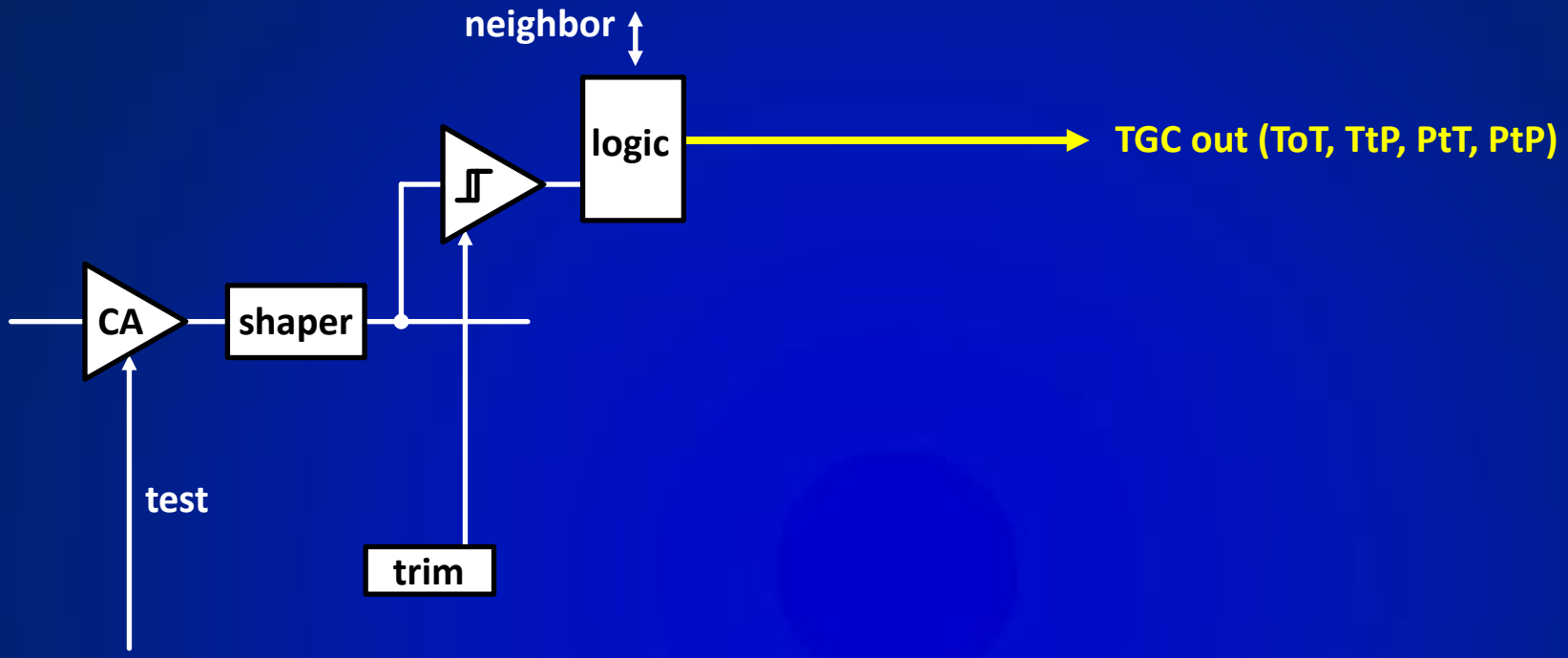
- input transistor: PMOS 180 nm x 20 mm, 2 mA
- input capacitance: optimized for 200 pF, can operate from sub-pF to nF
- polarity: adjustable positive or negative
- gain: adjustable 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (max charge 2 to 0.06 pC)
- peaking time: adjustable 25, 50, 100, 200 ns
- leakage-adaptive, DDF shaper, BGR-stabilized baseline, test capacitor, mask

VMM2 Architecture - Discriminator, Neighbor Logic



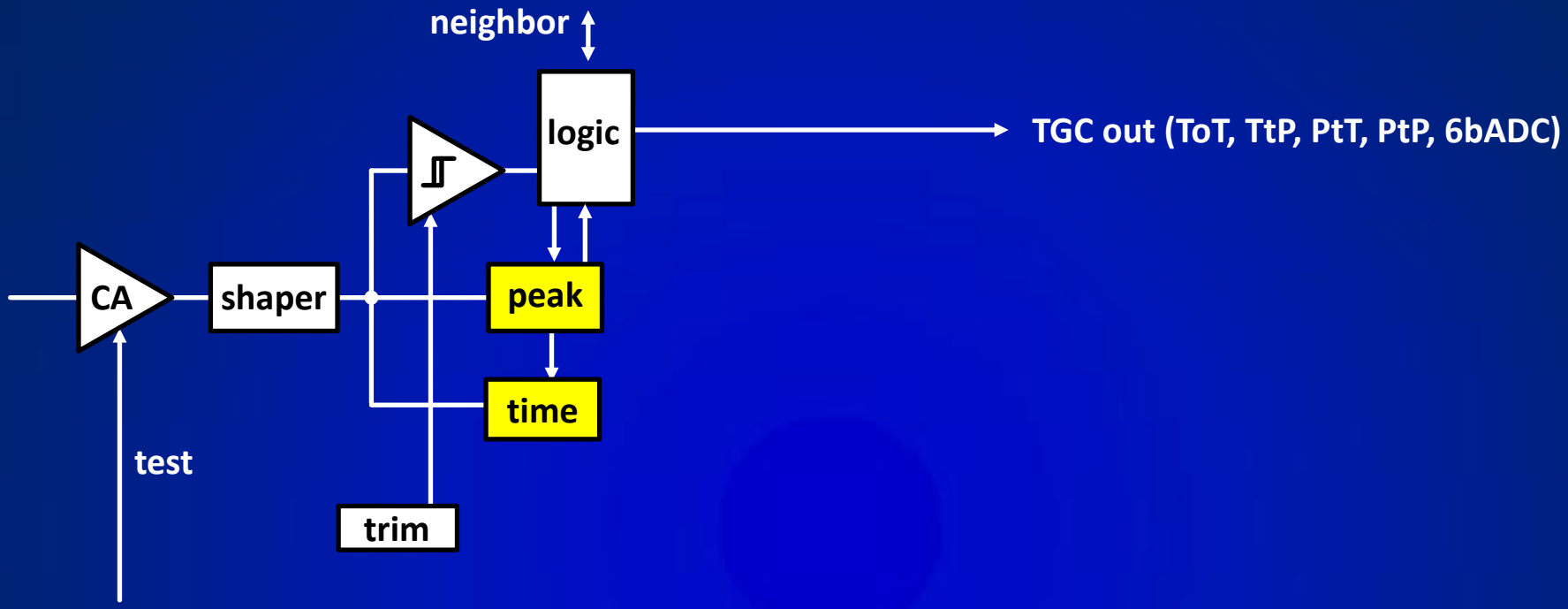
- adjustable discrimination threshold per channel
- trimming range: 15 mV in 1m increments
- comparator hysteresis: ~ 20 mV
- sub-hysteresis discrimination: effective discrimination ~ 2 mV
- neighbor logic: processing of sub-threshold neighbor channels
- inter-chip communication: neighbor channel logic includes neighbor chips

VMM2 Architecture - Direct Timing Measurements



- direct digital output per channel: LVDS 600 mV +/- 150 mV
- selectable measurements: - time-over-threshold (ToT)
  - threshold-to-peak (TtP)
  - peak-to-threshold (PtP)
  - pulse at peak (PtP)
- continuous self-reset operation

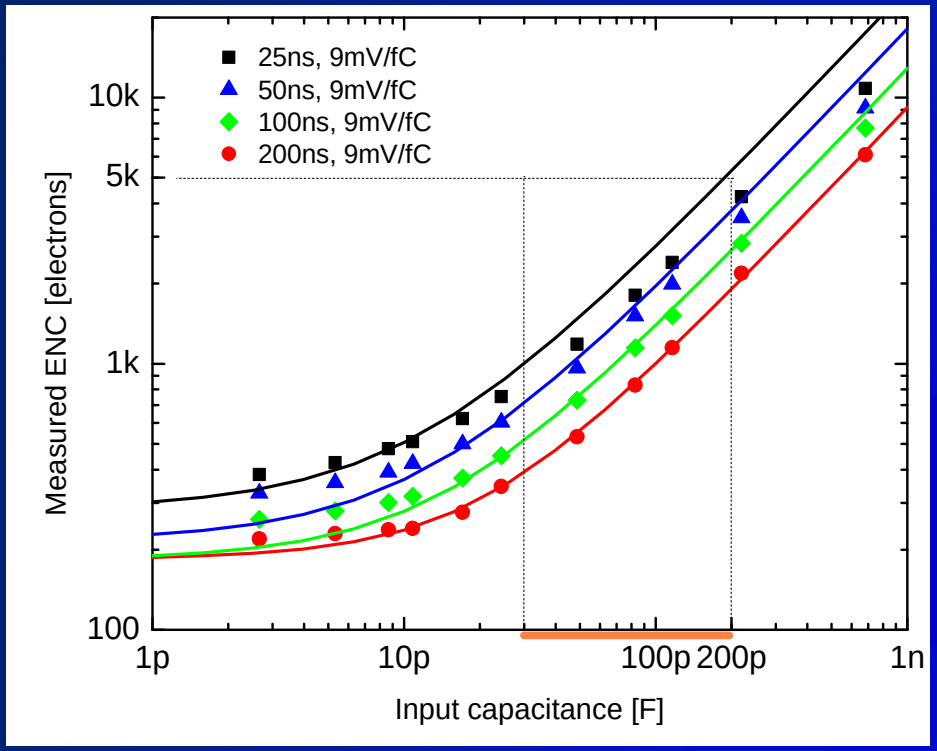
VMM2 Architecture - Peak and Time Detectors



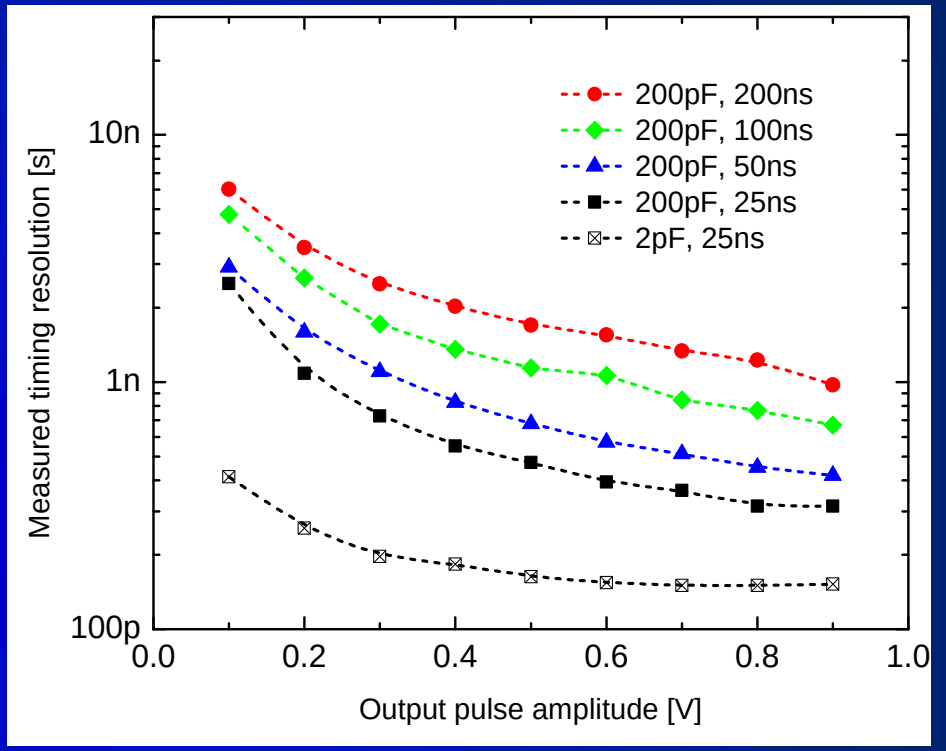
- peak detection: measurement of peak amplitude and storage in analog memory
- time detection: measurement of peak time and storage in analog memory
  - sub-mV resolution on amplitude measurement
  - sub-ns resolution, low time-walk on peak time measurement
- multi-phase offset-free measurement circuits
- adjustable time-to-amplitude converter (TAC): 125, 250, 500, 1000 ns
- optional current output for current-mode ADCs

Resolution Measurements (VMM1)

charge resolution



timing resolution



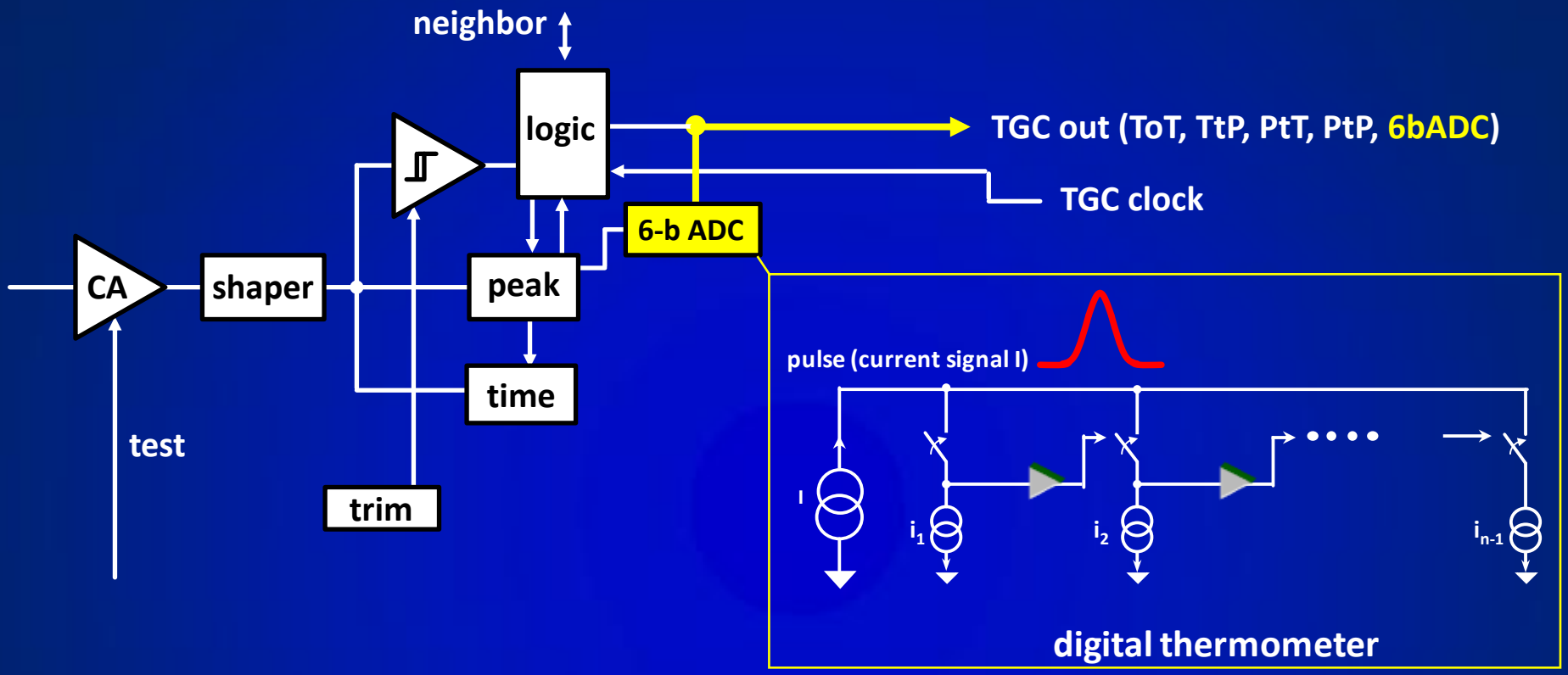
- charge resolution ENC < 5,000 e^- at 25 ns, 200 pF
- analog dynamic range Q_{max} / ENC > 12,000 → DDF
- timing resolution < 1 ns (at peak-detect)

$$\sigma_t \approx \frac{ENC\,\tau_P}{Q}\,\frac{\lambda_P}{\rho_P}$$

≈ 0.3-0.8

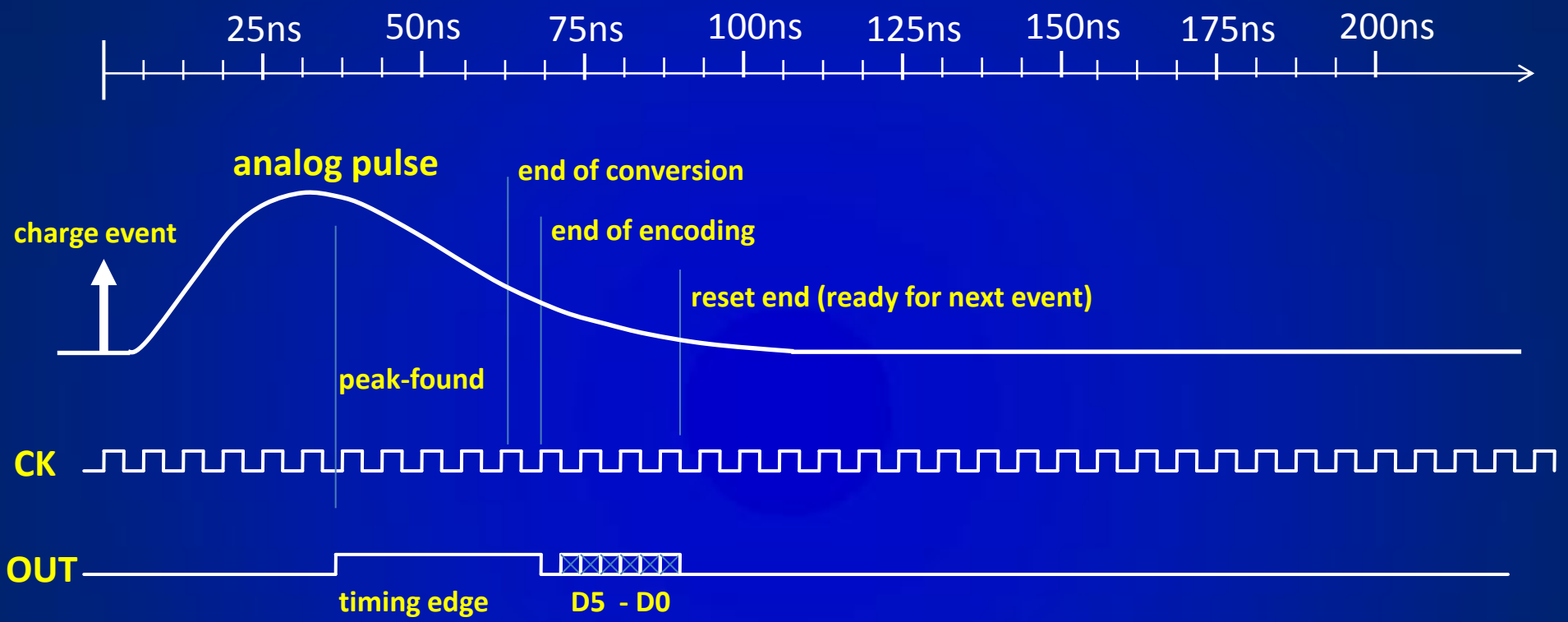
G. De Geronimo, in "Medical Imaging" by Iniewski

VMM2 Architecture - 6-bit ADC



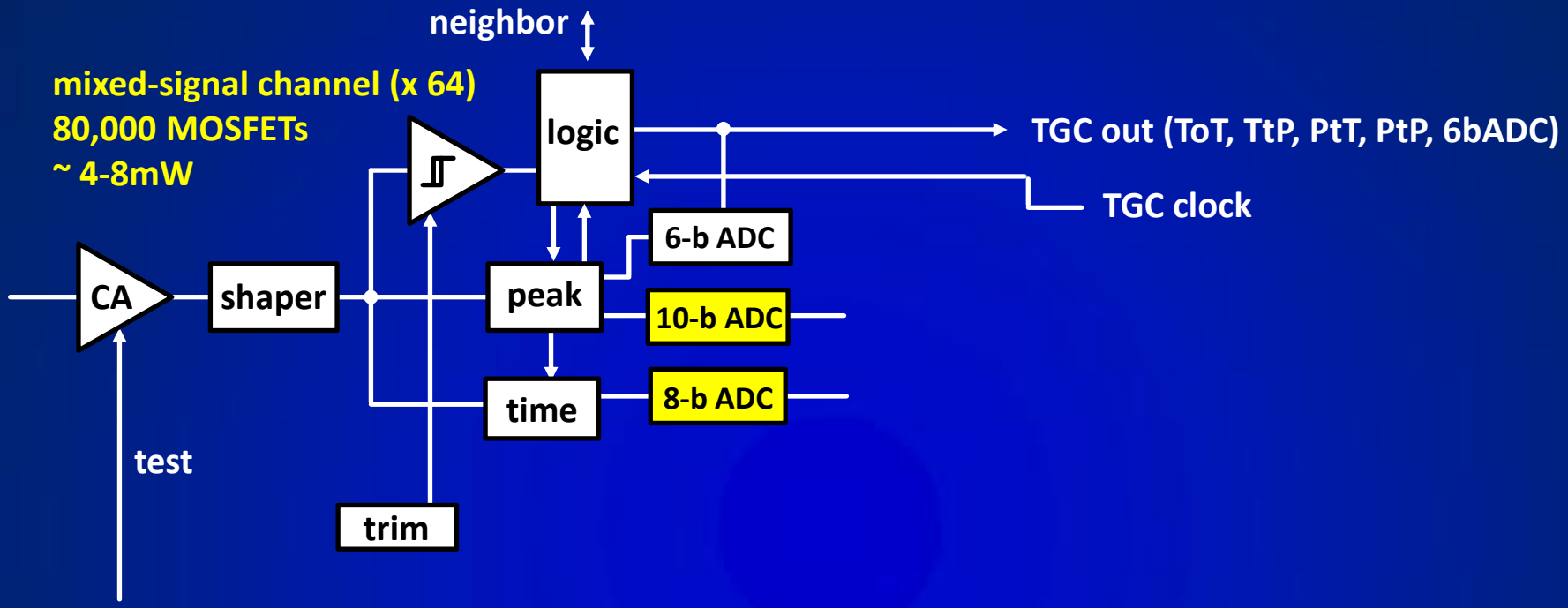
- lower-resolution ADC: - 6-bit, sub-mW, adjustable conversion time and offset
  - clock-less single-stage current-mode domino architecture
  - at threshold-crossing, completes in 25 ns from peaktime
- at direct output: flag at peak followed by serialized address
- clock frequency: up to 200 MHz
- selectable serialized mode: either at each clock cycle or at each clock edge
- continuous self-reset operation

Direct Output with 6-bit ADC



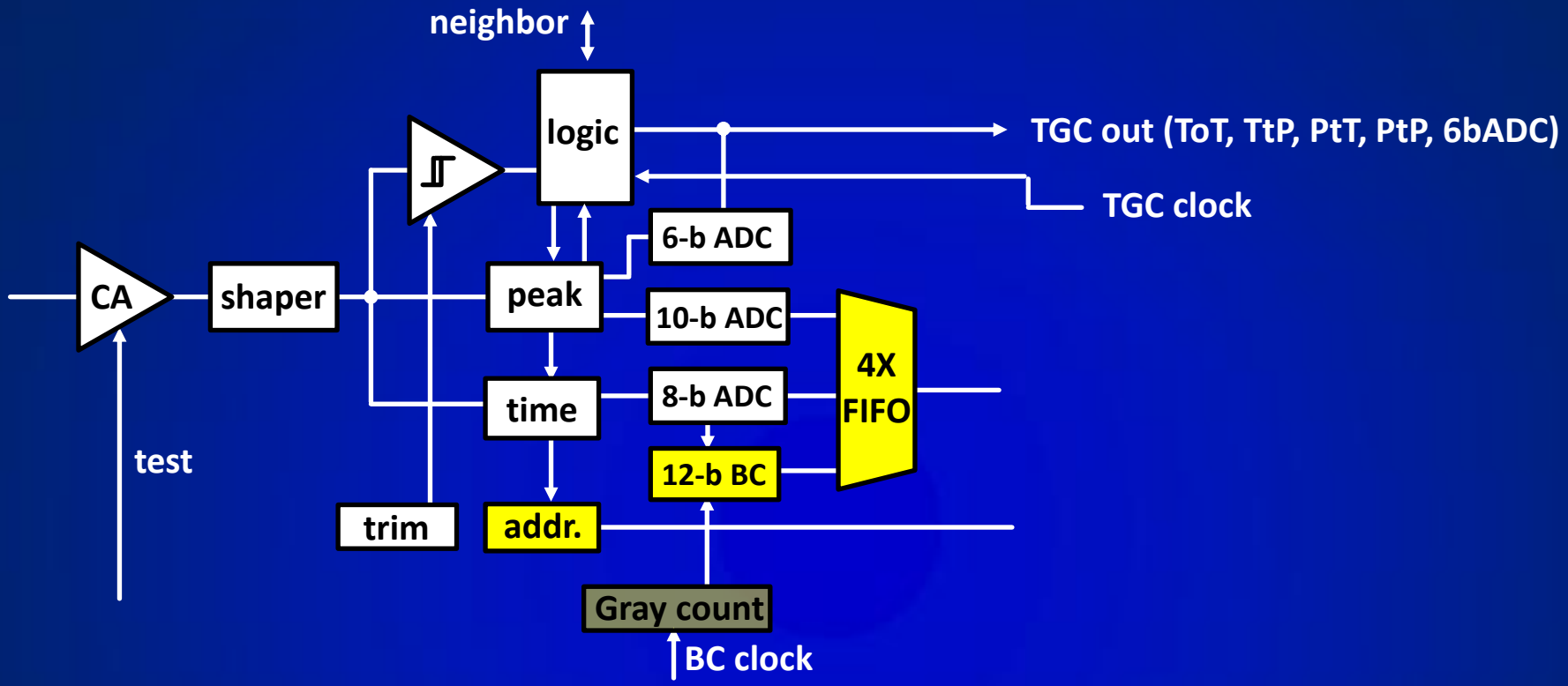
- conversion completes within ~25 ns from peak
- dead time from charge event < 100 ns
- 6-bit amplitude *D5-D0* shifted at each clock cycle or edge
- up to 200 MHz readout

VMM2 Architecture - 10-bit and 8-bit ADCs



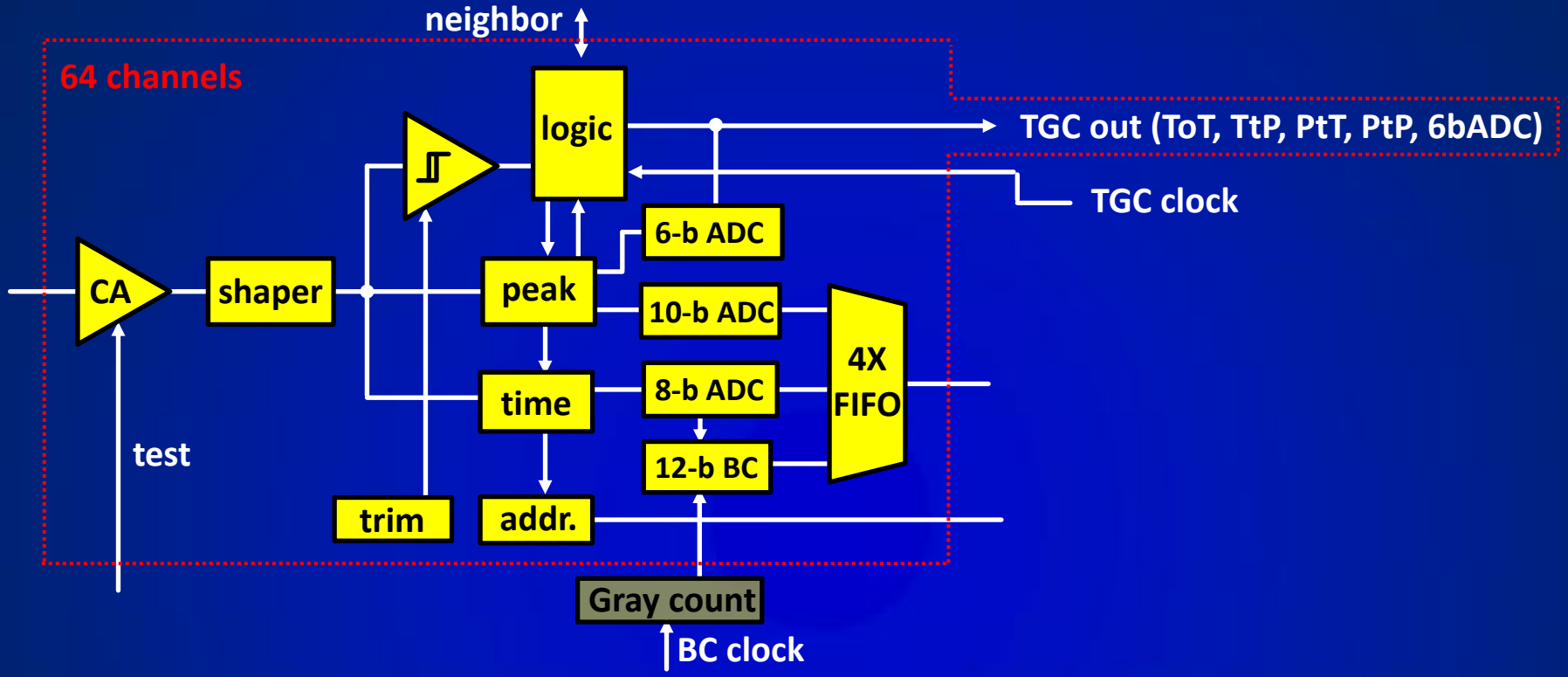
- higher-resolution ADCs: - 10-bit , 200 ns , sub-mW, for peak amplitude conversion
  - 8-bit , 100 ns , sub-mW for timing conversion
  - adjustable conversion time and offset
  - clock-less dual-stage current-mode domino architecture
- continuous self-reset operation

VMM2 Architecture - Timestamp and FIFO

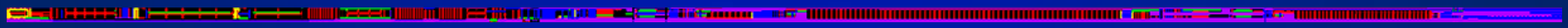


- 12-bit timestamp: - from *shared 12-bit Gray-code counter*, external BC clock
  - stops TAC and latches coarse timing
- complete timing information: 20-bit, ~100 µs with sub-ns resolution
- 4-deep FIFO: threshold-crossing indicator, 10-bit ADC, 8-bit ADC, 12-bit BC
- address memory

VMM2 Architecture - Complete Channel

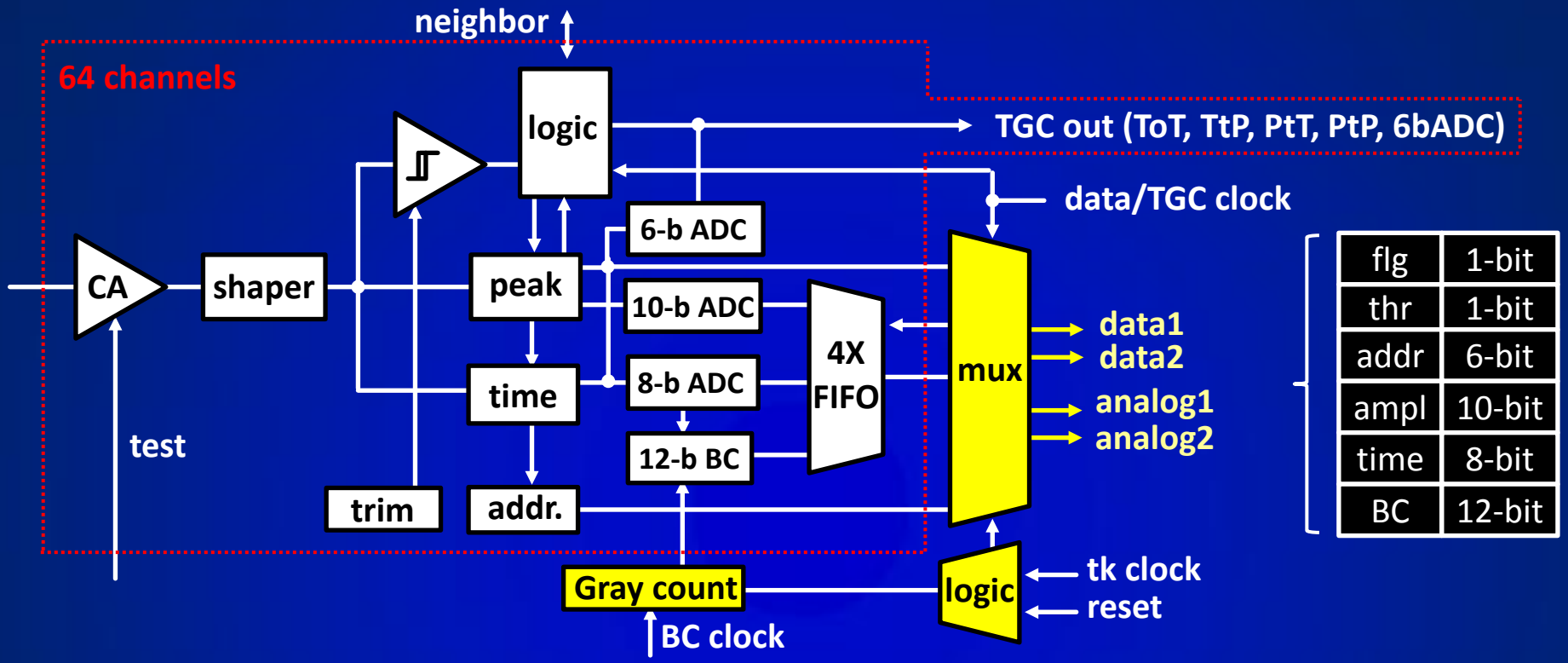


- 64 independent channels
- neighbor communication
- 4-8 mW / channel depending on configuration



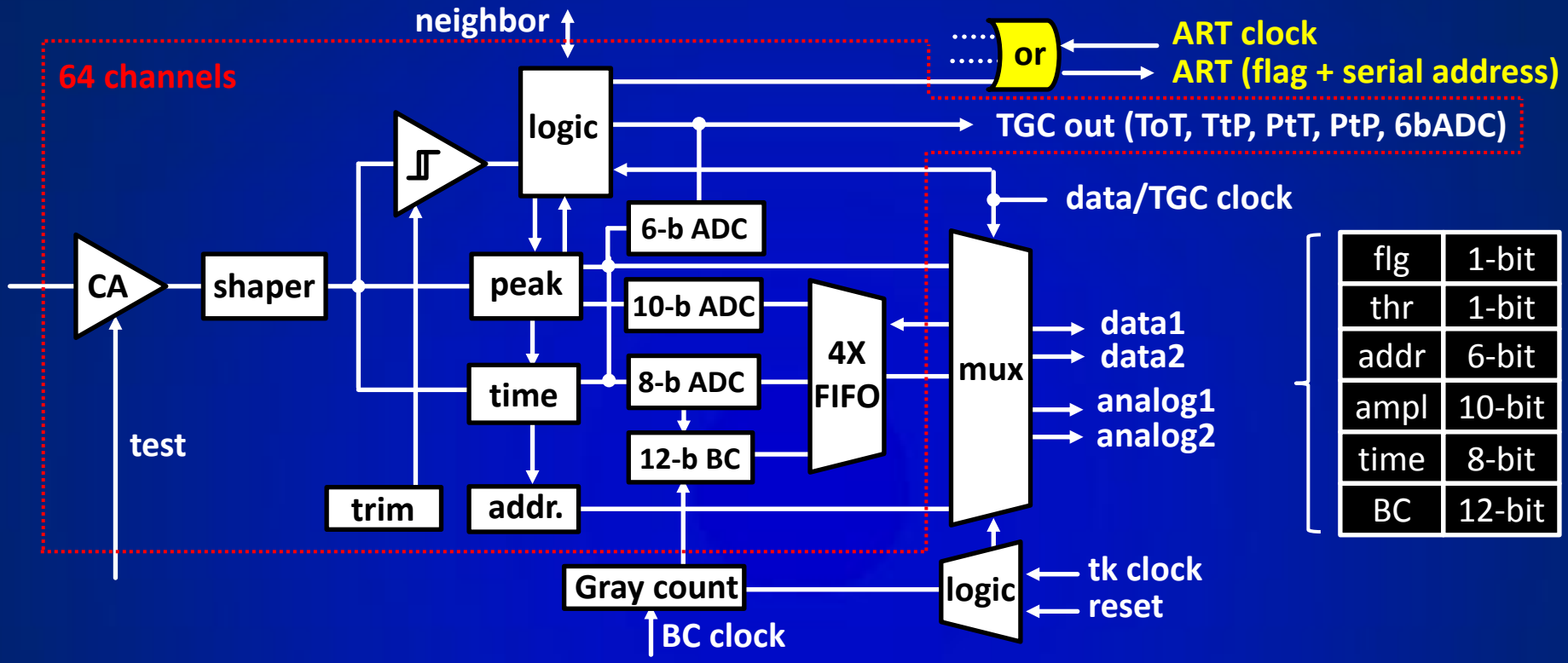
layout size: 12 mm x 100 µm = 1 mm²
80,000 MOSFETs

VMM2 Architecture - Multiplexing and Readout



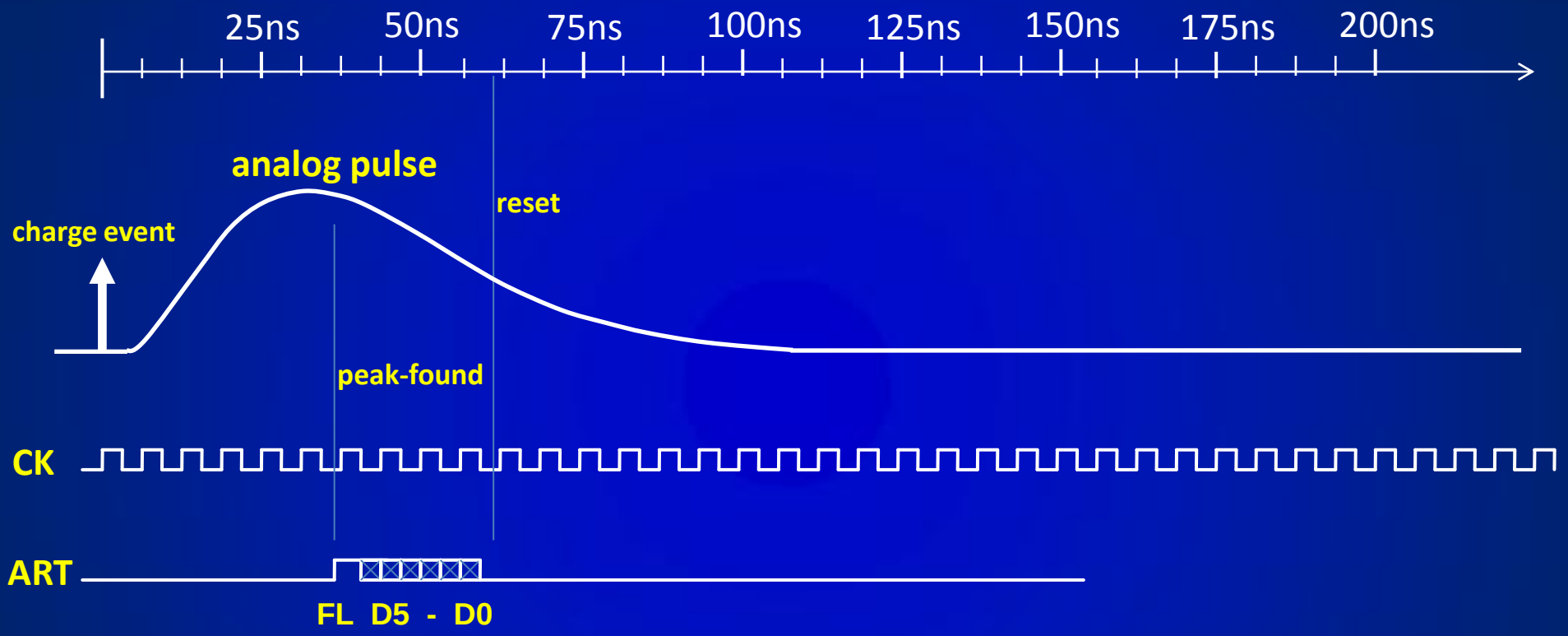
- sparse readout of amplitude/timing with token passing
- readout options:
  - mixed-signal 2-phase: peak and time at analog outputs analog1,2
    address serialized at digital output data1
  - fully digital continuous: 38-bit event data at digital outputs data1,2
    data1 also serves as empty flag
    data shift at each clock cycle or at each clock edge
    up to 200 MHz

VMM2 Architecture - Address in Real Time (ART)



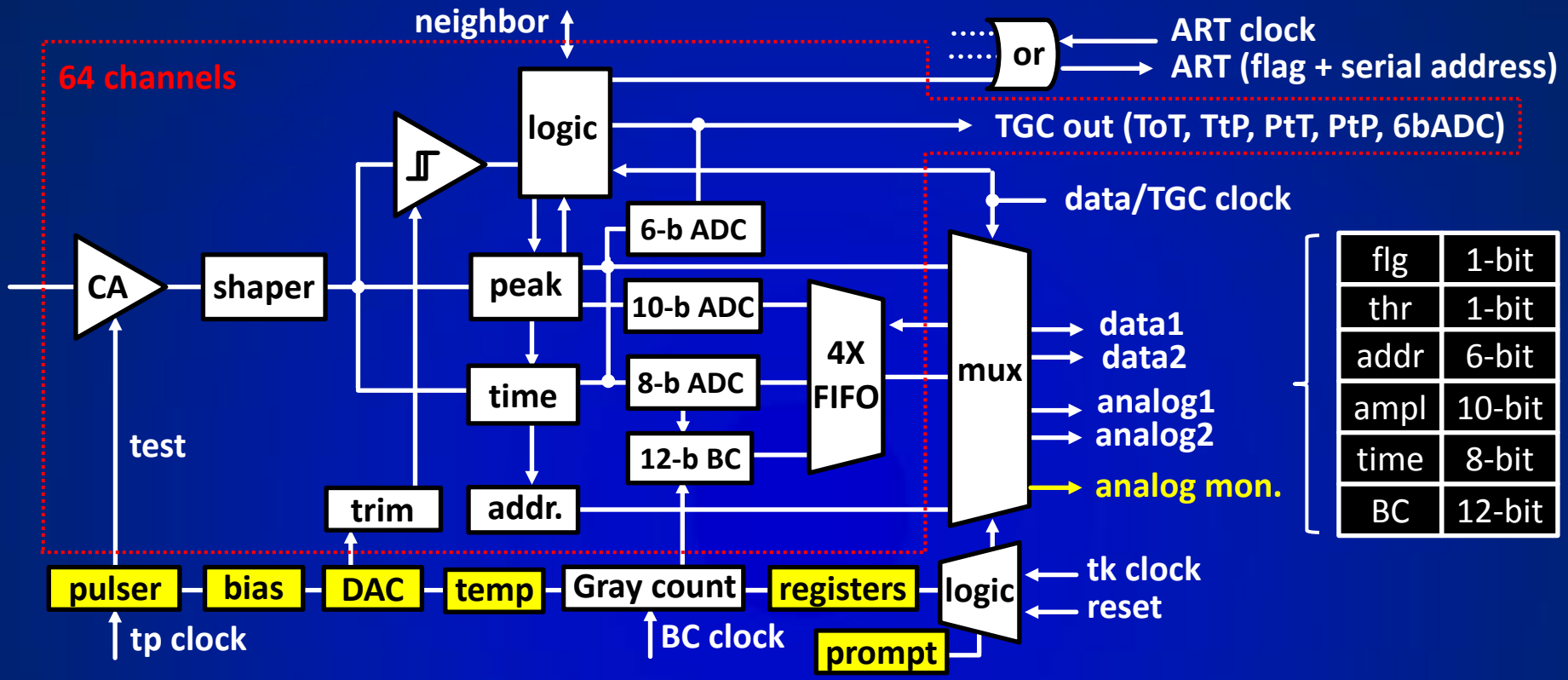
- address of first event (ART): - available at dedicated output ART
  - first event flag followed by serialized event address
  - shifted at each clock cycle or at each clock edge
  - up to 200 MHz, self-reset

ART (Address in Real Time)



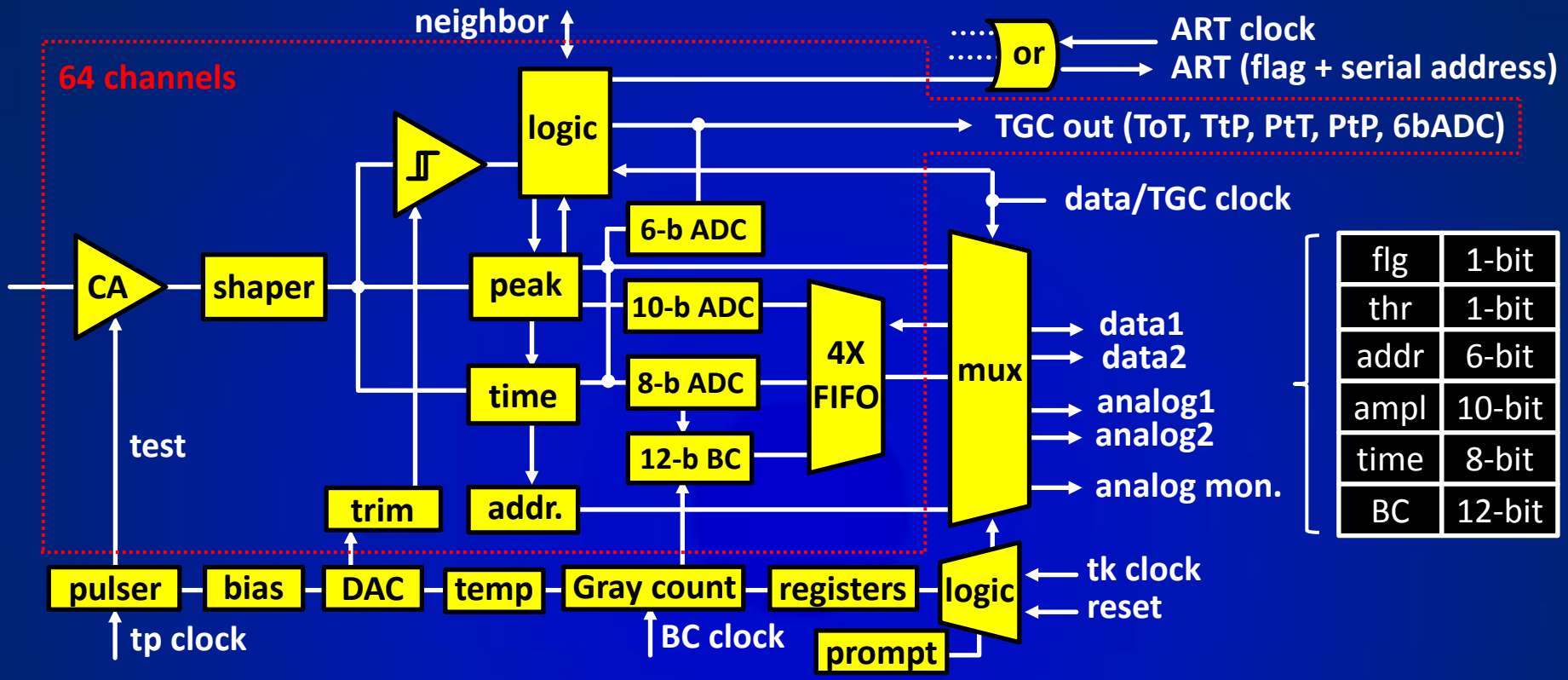
- flag and address serialized
- 6-bit address *D5-D0* shifted at each clock cycle or edge
- up to 200 MHz readout

VMM2 Architecture - Additional Functions



- coarse time counter: 12-bit Gray-code
- test pulse generator: 10-bit adjustable
- coarse threshold generator: 10-bit adjustable
- analog monitor: analog signal, trimmed threshold, DACs, temperature
- temperature sensor: ~ 725 mV - 1.85 mV/°C
- configuration registers: 80-bit + 24-bit / channel
- PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit

VMM2 Architecture - Complete ASIC

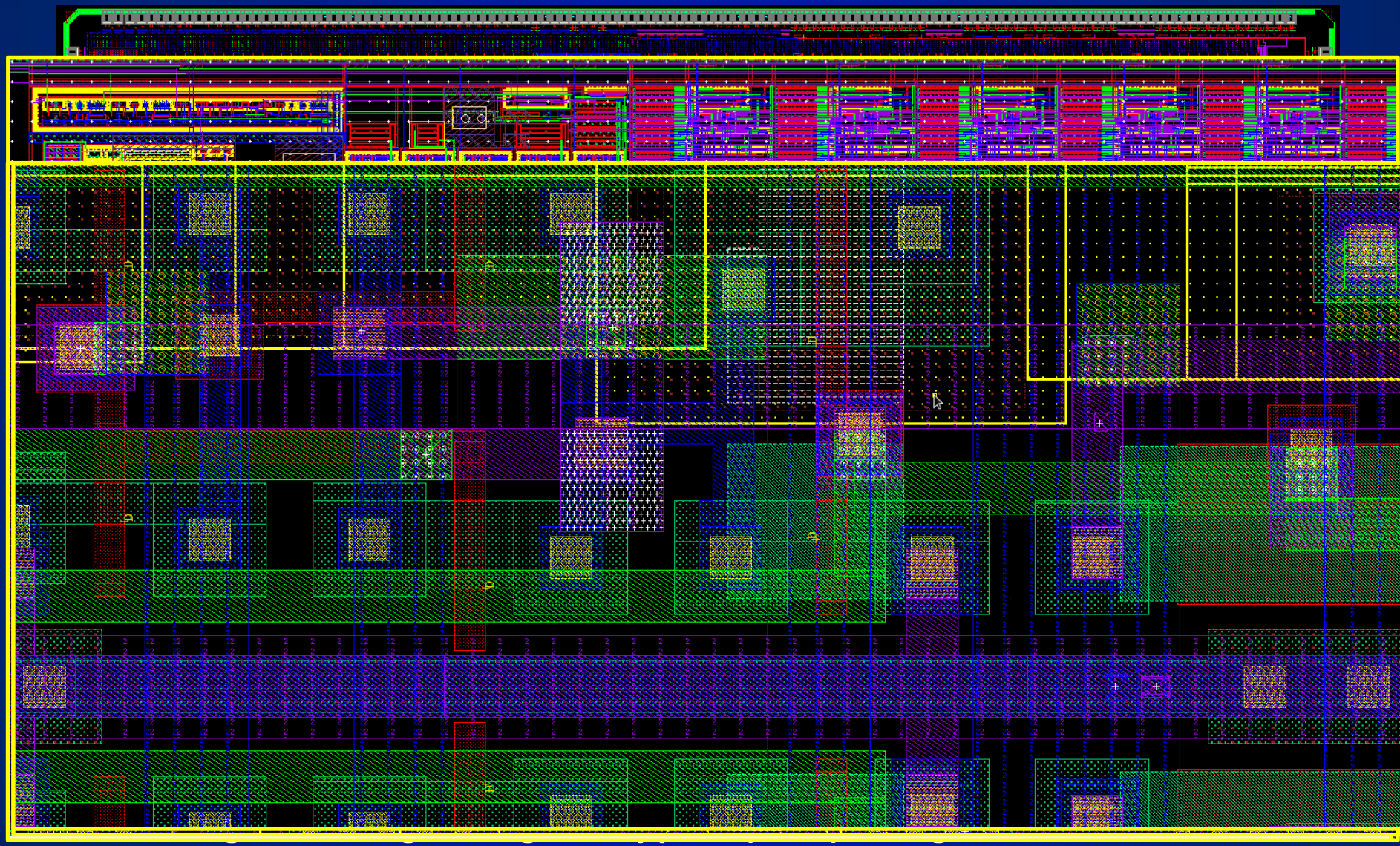


- coarse time counter: 12-bit Gray-code
- test pulse generator: 10-bit adjustable
- coarse threshold generator: 10-bit adjustable
- temperature sensor: ~ 725 mV - 1.85 mV/°C
- configuration registers: 80-bit + 24-bit / channel
- PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit

- technology: IBM CMOS 130nm
- power dissipation: 4-8^{+} mV/ch.
- transistor count: > 5 million

Layout

analog, mixed-signal, digital supplies (1.2V) – neigh.t – digital IOs (14) - TGC outs 0-6



1315 µm

392 bonding pads

all by hand (no automation)

A Few Notes

- VMM2 is an extremely complex and ambitious ASIC

  - a planned redesign of VMM1 to bring us closer to the final VMM -

- Main risks from design complexity and layout parasitics
  - resolution may be affected by mixed-signal cross-talk
  - locking conditions may occur from complex control logic
  - 200 MHz operation may be affected by parasitics
  - performance (INL, DNL, ..) of novel ADCs to be verified

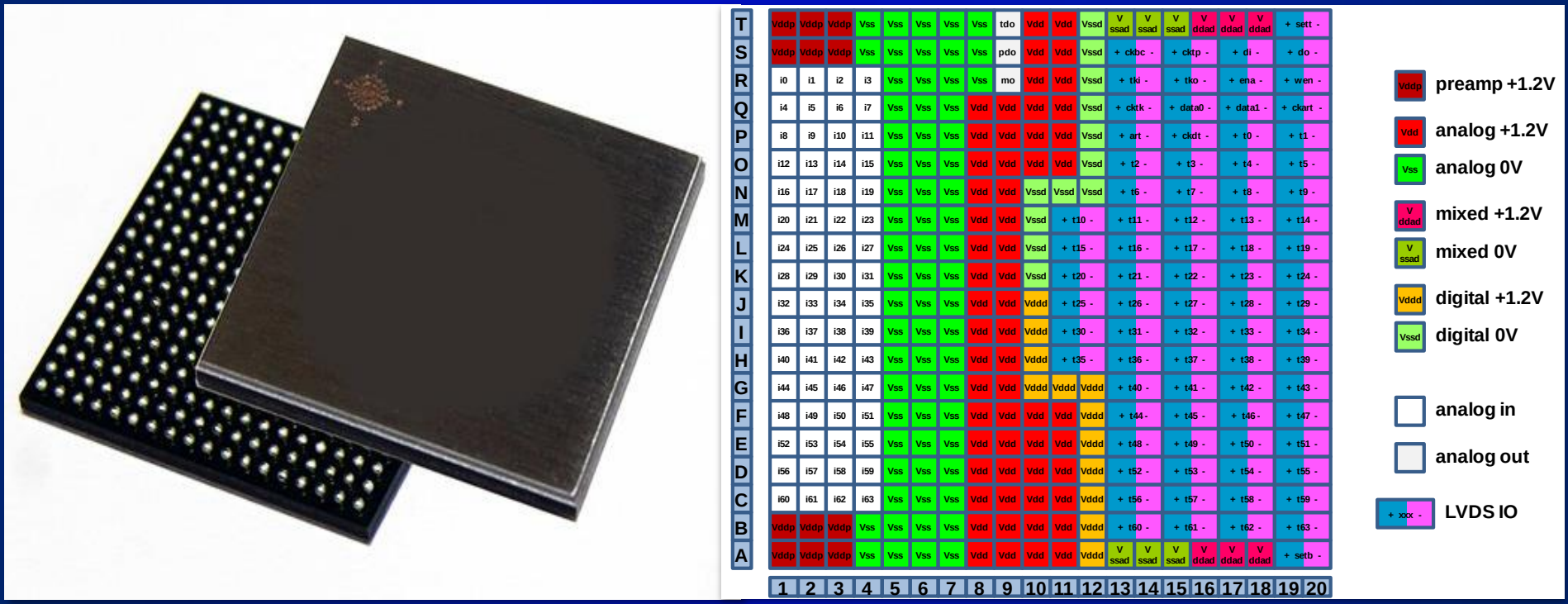
  - extensive simulations done to mitigate these risks -

- To be included in VMM3
  - simultaneous direct- and multiplexed-operation
  - DSP for Level 1 handling and additional shared FIFO
  - test patterns and clock output
  - SEU mitigation circuits
  - any fixes on VMM2

Packaging

custom BGA package

21 x 21 mm², 400-pin, 1 mm pitch



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
T	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vss	tdo	Vdd	Vdd	Vssd	V ssad	V ssad	V ssad	V ddad	V ddad	V ddad	+ sett -	
S	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vss	pdo	Vdd	Vdd	Vssd	+ ckbc -		+ cktp -		+ di -		+ do -	
R	i0	i1	i2	i3	Vss	Vss	Vss	Vss	mo	Vdd	Vdd	Vssd	+ tki -		+ tko -		+ ena -		+ wen -	
Q	i4	i5	i6	i7	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ cktk -		+ data0 -		+ data1 -		+ ckart -	
P	i8	i9	i10	i11	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ art -		+ ckdt -		+ t0 -		+ t1 -	
O	i12	i13	i14	i15	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ t2 -		+ t3 -		+ t4 -		+ t5 -	
N	i16	i17	i18	i19	Vss	Vss	Vss	Vdd	Vdd	Vssd	Vssd	Vssd	+ t6 -		+ t7 -		+ t8 -		+ t9 -	
M	i20	i21	i22	i23	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t10 -		+ t11 -		+ t12 -		+ t13 -		+ t14 -	
L	i24	i25	i26	i27	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t15 -		+ t16 -		+ t17 -		+ t18 -		+ t19 -	
K	i28	i29	i30	i31	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t20 -		+ t21 -		+ t22 -		+ t23 -		+ t24 -	
J	i32	i33	i34	i35	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t25 -		+ t26 -		+ t27 -		+ t28 -		+ t29 -	
I	i36	i37	i38	i39	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t30 -		+ t31 -		+ t32 -		+ t33 -		+ t34 -	
H	i40	i41	i42	i43	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t35 -		+ t36 -		+ t37 -		+ t38 -		+ t39 -	
G	i44	i45	i46	i47	Vss	Vss	Vss	Vdd	Vdd	Vddd	Vddd	Vddd	+ t40 -		+ t41 -		+ t42 -		+ t43 -	
F	i48	i49	i50	i51	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t44 -		+ t45 -		+ t46 -		+ t47 -	
E	i52	i53	i54	i55	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t48 -		+ t49 -		+ t50 -		+ t51 -	
D	i56	i57	i58	i59	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t52 -		+ t53 -		+ t54 -		+ t55 -	
C	i60	i61	i62	i63	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t56 -		+ t57 -		+ t58 -		+ t59 -	
B	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t60 -		+ t61 -		+ t62 -		+ t63 -	
A	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	V ssad	V ssad	V ssad	V ddad	V ddad	V ddad	+ setb -	

Vddp preamp +1.2V

Vdd analog +1.2V

Vss analog 0V

V ddad mixed +1.2V

V ssad mixed 0V

Vddd digital +1.2V

Vssd digital 0V

analog in

analog out

+ xxx - LVDS IO

Schedule

task	status
ASIC design	complete
ASIC layout	complete
ASIC fabrication	in progress expected by May 2014
BGA package	in progress expected by May 2014
PCB (AZ)	in progress expected by May 2014
ASIC tests	queued start in May-June 2014

Acknowledgment

Nachman Lupu (Technion Haifa, Israel) - Lorne Levinson (Weizmann Inst., Israel)

Ken Johns , Bill Hart (Univ. Arizona, USA) - George Iakovidis (NTU Athens, Grece)

Sorin Martoiu (IFIN-HH Bucharest, Romania) - Jay Chapman (Michigan Univ., USA)

Alessandro Marchioro (CERN) - Jessica Metcalfe (BNL, USA) - John Oliver (Harvard, USA)

Veljko Radeka (BNL, USA), CERN, ATLAS Collaboration